
ATM Forum/99-0243

Title: Aggregation of MIMO Latency

Abstract: This contribution shows how to compute the MIMO latency of a network path consisting of several components from the MIMO latencies of individual components.

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1. Introduction

In this contribution we explain how the latencies of several ATM components (switches, links, subnetworks) can be aggregated

2. An Alternative Definition of MIMO

MIMO latency of a switch is defined as:

$$\text{MIMO} = \text{FILO} - \text{FILO}_0$$

Where FILO is the measured first-bit-in to last-bit-out latency and FILO_0 (or NFOT) is the FILO latency of an ideal switch for the same input pattern. Note that FILO is the sum of frame input time (first bit in to last bit in) and the LILO (last bit in to last bit out) latency (see Figure 1):

$$\text{FILO} = \text{Frame Input Time} + \text{LILO}$$

and

$$\text{FILO}_0 = \text{Frame Input Time} + \text{LILO}_0$$

Since the frame input time does not depend upon the switch, MIMO can also be expressed as:

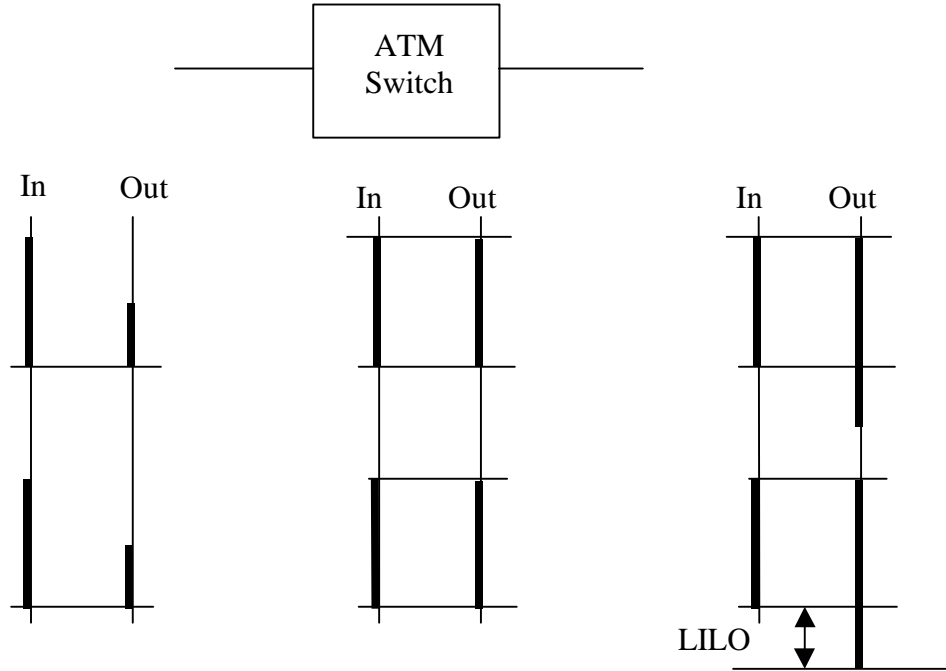
$$\text{MIMO} = \text{LILO} - \text{LILO}_0$$

Here, LILO is the measured LILO latency and LILO_0 is the LILO latency of an ideal switch for the same input pattern. Given input and output speeds, LILO_0 can be easily computed. Figure 2 shows three possible cases. The figure shows that LILO_0 is zero unless input speed is faster than the output speed.

$$\text{LILO}_0 = 0 \quad \text{if input speed} \leq \text{output speed}$$



Figure 1. Relation between MIMO and LILO



a. Input Speed < Output Speed b. Input Speed = Output Speed c. Input Speed > Output Speed

Figure 2. An ideal switch introduces a nonzero LILO latency only when input link speed is greater than the output link speed.

3. MIMO Latency of a Path:

Consider a network path consisting of n components in a series. Subscript i is used for the latency of the i^{th} component and subscript Σ for the combination. Thus,

$$\text{MIMO}_i = \text{LILO}_i - \text{LILO}_{0i}$$

Similarly for a network path:

$$\text{MIMO}_\Sigma = \text{LILO}_\Sigma - \text{LILO}_{0\Sigma}$$

Since LILO is additive:

$$\text{LILO}_\Sigma = \Sigma \text{LILO}_i$$

The above three relationships lead us to the following identity:

$$\text{MIMO}_\Sigma + \text{LILO}_{0\Sigma} = \Sigma (\text{MIMO}_i + \text{LILO}_{0i})$$

Or

$$\text{MIMO}_\Sigma = \Sigma \text{MIMO}_i + \Sigma \text{LILO}_{0i} - \text{LILO}_{0\Sigma}$$

This relationship allows us to compute MIMO of a series of components from the measured MIMO values of individual components. Note that $LILO_{0i}$ and $LILO_{0\Sigma}$ can be computed given the input pattern and the input output speeds.

We illustrate this with a few examples.

Example 1:

Consider the configuration shown in Figure 3 consisting of two switches interconnected via a wire. All links and ports are 155 Mbps (OC-3). The input frame is composed of two cells with a gap of 3 cell times. Let us suppose that each switch introduces a MIMO equal to c , where c is the cell time at OC-3. Also, for simplicity assume that the wire between the switches also introduces a MIMO of c . (Other wire lengths can be handled similarly).

Since all input/output speeds are same, an ideal switch will produce zero LILO latency. Hence,

$$\begin{aligned}
 LILO_{0i} &= 0 \\
 LILO_{0\Sigma} &= 0 \\
 MIMO_{\Sigma} &= \Sigma MIMO_i = c + c + c = 3c
 \end{aligned}$$

That is, the MIMO latency is simply the sum of individual MIMO latencies.

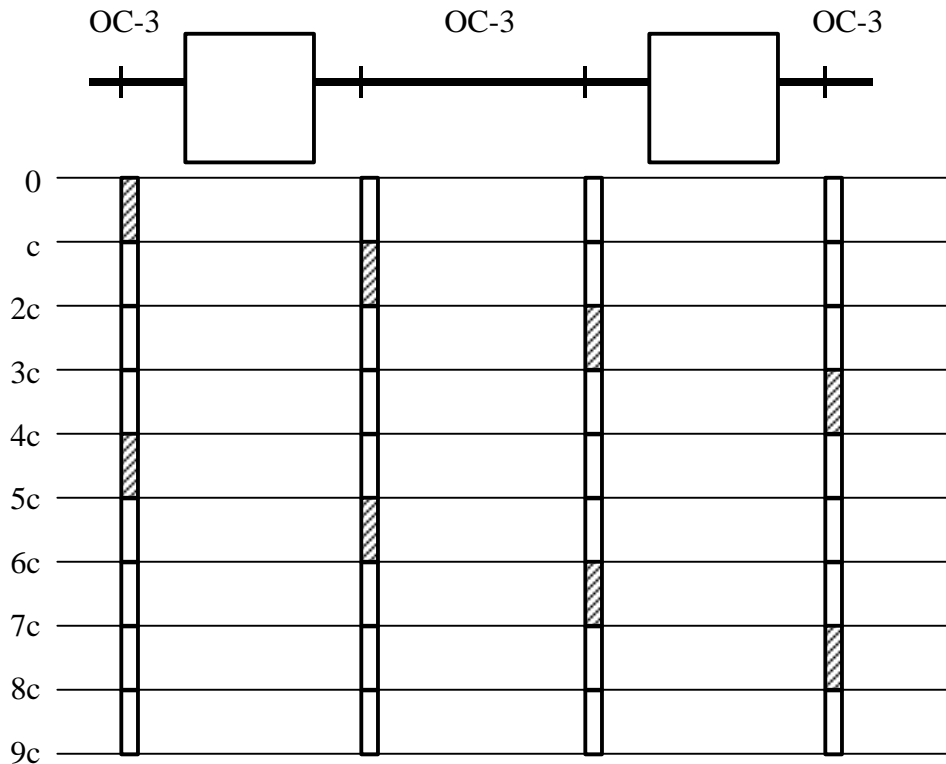


Figure 3. MIMO aggregation for Example 1.

Example 2:

Consider the configuration shown in Figure 4. This is similar to the configuration of Example 1, except that the intermediate link is 51.4 Mbps and therefore, introduces a delay of $3c$.

In this case, the first switch has an input speed of OC-3, while the output speed is OC-1. An ideal switch with these I/O speeds will produce a LILO latency of $2c$, where c is the cell time at OC-3. That is,

$$LILO_{01} = 2c$$

For the wire as well as the second switch, the input speed is equal to or less than the output speed and so the $LILO_0$ is zero:

$$LILO_{02} = 0$$

$$LILO_{03} = 0$$

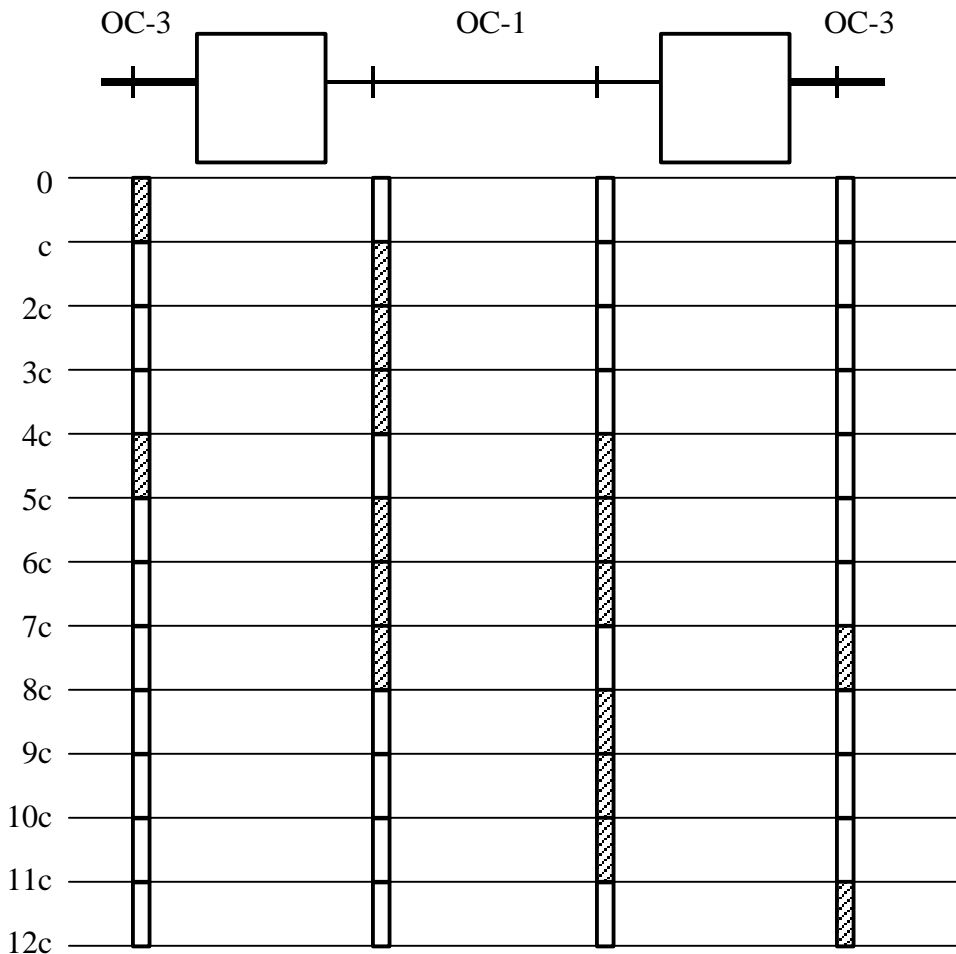


Figure 4. MIMO aggregation for Example 2.

If the whole network is replaced by a single ideal switch, that switch will have an input speed of OC-3 and an output speed of OC-3 and therefore, will have a zero LILO latency.

That is,

$$LILLO_{0\Sigma} = 0$$

Using the above values, we get:

$$MIMO_{\Sigma} = \Sigma MIMO_i + \Sigma LILLO_{0i} - LILLO_{0\Sigma} = (c+3c+c) + (2c+0+0) - 0 = 7c$$

4. Recommended Changes to the Baseline [Motion]:

- a. Add Section 2 and 3 in Appendix A of the baseline text [1] after Section A.7 (With appropriate section renumbering)
- b. Throughout the document replace "NFOT" with "FILO₀" for consistency and clarity.

Reference:

[1] ATM Forum/BTD-TEST-TM-PERF.00.11 (Draft) February 1999