

\*\*\*\*\*

ATM Forum Document Number: ATM\_Forum/97-0859

\*\*\*\*\*

**Title:** Measurement Experiences with the Revised MIMO Latency Definition

\*\*\*\*\*

**Abstract:** In this contribution, we present frame delay measurement results and calculations using the revised MIMO latency definition in the cases with different input and output link rates and discontinuous frames on input.

\*\*\*\*\*

**Source:**

Gojko Babic, Arjan Durresi, Justin Dolske, Raj Jain  
The Ohio State University

Raj Jain is now at Washington University in Saint Louis, jain@cse.wustl.edu <http://www.cse.wustl.edu/~jain/>

The presentation of this contribution at the ATM Forum is sponsored by NASA.

\*\*\*\*\*

**Date:** September 1997

\*\*\*\*\*

**Distribution:** ATM Forum Technical Working Group Members (AF-TEST, AF-TM)

\*\*\*\*\*

**Notice:**

This contribution has been prepared to assist the ATM Forum. It is offered to the Forum as a basis for discussion and is not a binding proposal on the part of any of the contributing organizations. The statements are subject to change in form and content after further study. Specifically, the contributors reserve the right to add to, amend or modify the statements contained herein.

\*\*\*\*\*

# Measurement Experiences with the Revised MIMO Latency Definition

## 1. Introduction

We presented in [1] some of our experiments from ATM switch performance testing. Among other results, we provided a number of frame latency measurements and calculations using the old MIMO latency definition as given in [2]. The test configuration used included a commercial ATM monitor and a commercial switch with an input link rate equal to the output link rate, and all tests were performed with contiguous frames on input.

In this contribution, we present frame latency measurement results and calculations using the revised MIMO latency definition [3] for the test configuration with different input and output link rates, and discontinuous frames on input.

## 2. Some Considerations About Calculations Using the Old MIMO Latency Definition

As we have indicated, we used the old MIMO latency definition for frame latency calculations in [1]. However, the results using the old MIMO latency definition and the revised MIMO latency definition are identical for cases when the input link rate is equal to or lower than the output link rate, since both definitions give:

$$\text{MIMO latency} = \text{LILO latency} \quad (1)$$

In [1], we also illustrated that the same results for MIMO latency are obtained using either Expression (1) or Expression (2), which is given as:

$$\text{MIMO latency} = \text{FILO latency} - \text{NFOT} \quad (2)$$

for cases when the input link rate is equal to the output link rate.

The revised MIMO definition defines NFOT slightly differently than the old definition did. However, it turns out that both definitions produce identical NFOT values for contiguous frames on input if the input link rate is equal to the output link rate, which was the case in our measurement tests.

In conclusion, all results and calculations for frame latency in [1] are still valid and correct, although the old MIMO latency definition was used.

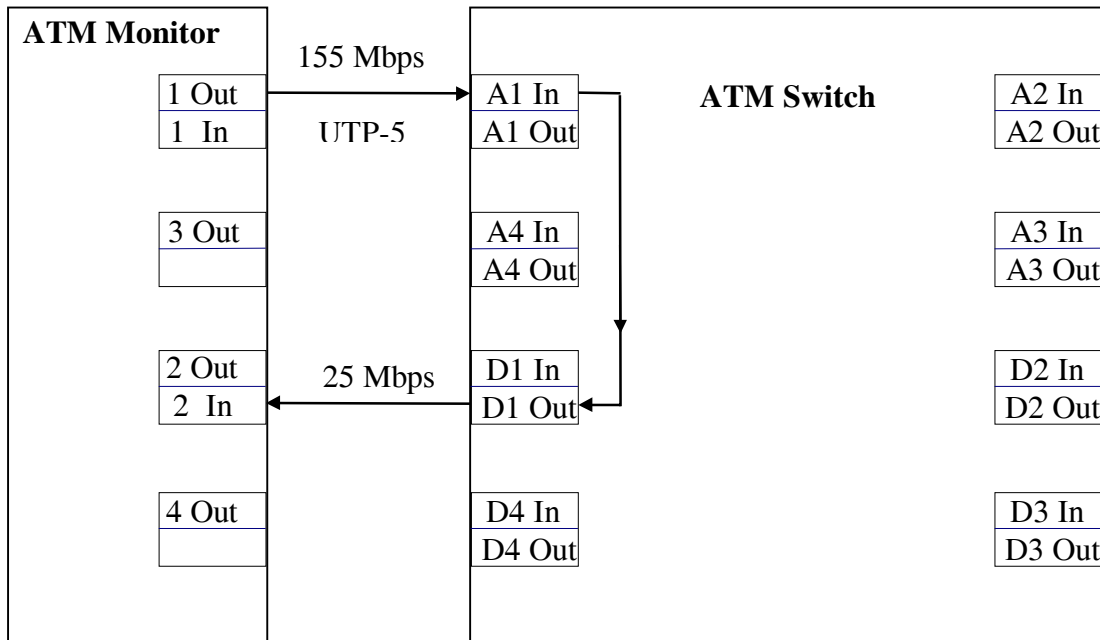
### 3. Latency Test with Input Link Rate Higher Than Output Link Rate

#### Configuration

The test configuration for the new MIMO latency measurements for the case with an input link rate higher than the output link rate is shown in Figure 1. The test configuration includes one ATM test system (monitor) and one ATM switch, with a 155 Mbps UTP-5 link between the monitor port 1 and the switch port A1 and a 25 Mbps link between the monitor port 2 and the switch port D1. A permanent virtual channel connection (VCC) is established between the monitor ports 1 and 2 via the switch ports A1 and D1. This VCC is used for transmission of frames in the latency test. These frames are referred to as “test frames.” Figure 1 also indicates the traffic flow direction. Tests are performed without background traffic.

Note that in the given test configurations with a 155Mbps UTP-5 input link and a 25Mbps output link, we have:

- CIT = cell input time =  $424[\text{bits}] / \text{Input Link Rate}$   
=  $424[\text{bits}] / 149.76 [\text{Mbps}]$   
=  $2.83 \mu\text{sec}$
- COT = cell output time =  $424[\text{bits}] / \text{Output Link Rate}$   
=  $424[\text{bits}] / 25.6 [\text{Mbps}]$   
=  $16.56 \mu\text{sec}$



**Figure 1:** Test configuration for measurements of MIMO latency

### Measurement Results and Calculations

We performed all our tests with 32-cell frames. One of the measurements used contiguous frames, i.e. cells of the test frame were transmitted back-to-back. In the rest of the tests, we introduce identical gaps (unassigned cells or cells of other frames) between cells of the test frame.

As explained in [3], when the input link rate is higher than or equal to the output link rate, MIMO latency can be obtained by measuring the transfer delay of the first cell and the inter-arrival time between the first cell and the last cell of the frame. In this case, MIMO latency is calculated as:

$$\text{MIMO latency} = \text{First cell's transfer delay} + \text{First cell to last cell inter-arrival time} - \text{NFOT} \quad (3)$$

Table 1 presents measurement results for eight test runs, from which MIMO latency is calculated. The first test uses a contiguous test frame on input. All other tests use discontinuous frames on input, with gaps between cells of the test frame, as indicated in the second column. Our tests do not show any significant difference if gaps include unassigned cells or cells of other frames, which leave the switch through output links other than the one used by the test frames.

The next two columns present measurement results for the first cell's delay and interarrival time between the first and the last cells.

**Table 1:** MIMO Latency Measurement Results and Calculated Results for 155Mbps Input and 25Mbps Output (all time are in  $\mu\text{sec}$ )

Test No.	Frame Pattern	1 <sup>st</sup> cell delay	First cell to last cell inter-arrival time	NFOT	MIMO Latency
1	No gap	36.8	526.5	530.0	33.3
2	1-cell gaps	35.8	526.0	530.0	31.8
3	2-cell gaps	36.8	526.0	530.0	32.8
4	3-cell gaps	34.8	526.5	530.0	31.3
5	4-cell gaps	40.8	519.5	530.0	30.3
6	5-cell gaps	36.8	526.5	542.9	19.9
7	6-cell gaps	36.8	616.0	630.6	22.2
8	7-cell gaps	35.3	705.0	718.4	21.9

The fifth column includes calculated values for NFOT, as explained in [3] given a frame pattern on input. Here is how we calculate those values. For the first five tests, it can be found that each cell entering a zero-delay switch has to wait for transmission of the previously received cell to finish. Thus, on output we should have back-to-back cells, i.e. a contiguous frame. Then, we can calculate NFOT for 32-cell frames in all those cases as:

$$\text{NFOT} = 32 \times \text{COT} = 32 \times 16.56 = 530 \text{ } \mu\text{sec}$$

In the last three tests, the gaps on input are large enough that no cells have to wait on a previously received cell. In the case with 5-cell gaps, the first bit of the 32<sup>nd</sup> (last) cell arrives at a zero-delay switch at time  $t$ , where

$$t = (\text{CIT} + 5\text{-cell gap}) \times 31 = 6 \text{ CIT} \times 31 = 526.4 \text{ } \mu\text{sec}$$

and then

$$\text{NFOT} = t + \text{COT} = 526.4 + 16.5 = 542.9$$

In the case with 6-cell gaps, the first bit of the 32<sup>nd</sup> (last) cell arrives at a zero-delay switch at time  $t$ , where

$$t = (\text{CIT} + 6\text{-cell gap}) \times 31 = 7 \text{ CIT} \times 31 = 614.1 \text{ } \mu\text{sec}$$

and then

$$\text{NFOT} = t + \text{COT} = 614.1 + 16.5 = 630.6 \text{ } \mu\text{sec}$$

Similarly, in the case with 7-cell gaps, the first bit of the 32<sup>nd</sup> (last) cell arrives at a zero-delay switch at time  $t$ , where

$$t = (\text{CIT} + 7\text{-cell gap}) \times 31 = 8 \text{ CIT} \times 31 = 701.9 \text{ } \mu\text{sec}$$

and then

$$\text{NFOT} = t + \text{COT} = 701.9 + 16.5 = 718.4 \text{ } \mu\text{sec}$$

In the last column of Table 1, MIMO latency values are obtained according to Expression (3) by adding terms in the third and the fourth column and subtracting the term in the fifth column.

It is interesting to note that the MIMO latency values for the last three measurements are about 30% lower than the first four measurements. Our explanation for such behavior of the switch under test is that the switch introduces additional delays when it has the overhead of processing queues of cells in its memory.

#### **4. Latency Test with Input Link Rate Lower Than Output Link Rate**

##### Configuration

We also performed different tests using the configuration in Figure 1, this time the test frames are sent in the opposite direction. In this way, we obtained a configuration for

latency testing with the input link rate lower than the output link rate. In this case, we have:

- CIT = cell input time = 16.56  $\mu$ sec
- COT = cell output time = 2.83  $\mu$ sec

Measurement Results and Calculations

We perform tests with 32-cell frames, with some idle periods between cells. According to [3], when the input link rate is lower than or equal to the output link rate MIMO latency can be calculated using Expression (3) or the following simple expression:

$$\text{MIMO Latency} = \text{LILO latency} = \text{Last cell's transfer delay} - \text{CIT} \quad (4)$$

To calculate MIMO latency according to Expression (4) it is only required that the transfer delay of the last cell of a frame be measured.

Table 2 presents measurement results for two test run, from which MIMO latency is calculated using both Expression (4) and Expression (3).

It is interesting to note that for the 25Mbps physical interface (which uses an unframed transmission system), our ATM monitor could not generate cells with accurate inter-cell idle periods (as is possible to do with unassigned cells in a framed transmission system). For example, although we attempted to generate back-to-back cells for the first test, there were still small idle periods between cells in the frame. Also, the second test had idle periods a little larger than one CIT, although we wanted to have gaps exactly one cell input time long. We had to perform off line tests to obtain the test frame pattern.

**Table 2:** MIMO Latency Measurement Results and Calculated Results for 25Mbps Input and 155Mbps Output (all times are in  $\mu$ sec)

Test No.	Last cell delay	MIMO Latency Expression (4)	1 <sup>st</sup> cell delay	First cell to last cell inter-arrival time	NFOT	MIMO Latency Expression (3)
1	32.0	15.4	31.0	535.0	550	16
2	32.5	15.9	33.0	1067.5	1082.6	17.9

The second, fourth and fifth columns present measurement results. MIMO latency values for the third column are obtained from the second column results using Expression 4. Values for NFOT are obtained by monitoring the frame pattern generated by our ATM monitor. Using Expression (3) and values in the fourth, fifth and sixth columns, the MIMO latency values in column 7 are obtained.

It can be observed that good agreement of MIMO latency values can be obtained using the two expressions for its calculation.

## References:

- [1] Gojko Babic, Arjan Durresi, Raj Jain, Justin Dolske, Shabbir Shahpurwala, "ATM Switch Performance Testing Experience," ATM\_Forum/97-0178R1, April 1997
- [2] Raj Jain, Gojko Babic, "MIMO Latency: Revised Proposed Text," ATM\_Forum/96-1762, December 1996
- [3] Gojko Babic, Arjan Durresi, Raj Jain, Justin Dolske, "Revised MIMO Definition," ATM\_Forum/97-0612, July 1997