Vivado V2017.2 Tutorial

William D. Richard, Ph.D.

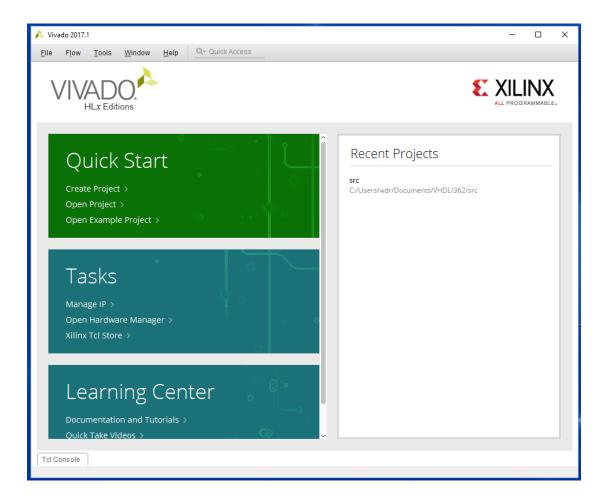
September 19, 2017

Updated Septembert 10, 2018

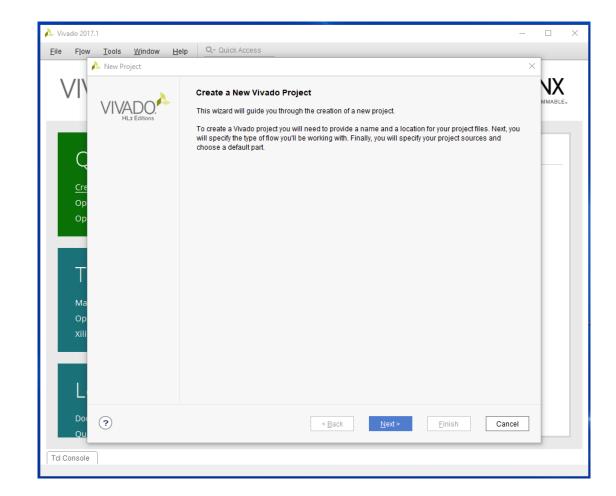
Create your source using a text editor: example.vhd

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b : IN STD_LOGIC ;
c : IN STD_LOGIC ;
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           d : IN STD LOGIC ;
          e : IN STD LOGIC ;
           output : OUT STD LOGIC) ;
END andx ;
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   SIGNAL temp1 : std logic ;
   SIGNAL temp2 : std logic ;
BEGIN
   temp1 <= a AND b AND c ;</pre>
   temp2 <= d AND e ;</pre>
   output <= temp1 AND temp2 ;</pre>
END nonsense ;
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Run Vivado and select "Create New Project"



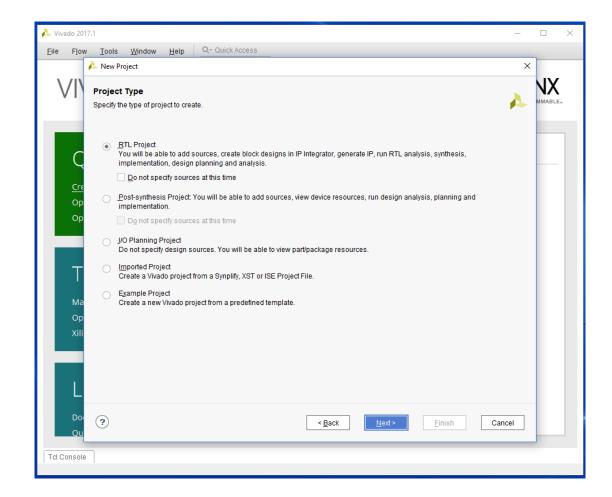
Read the info screen and click "Next"



Select the project directory and name your project

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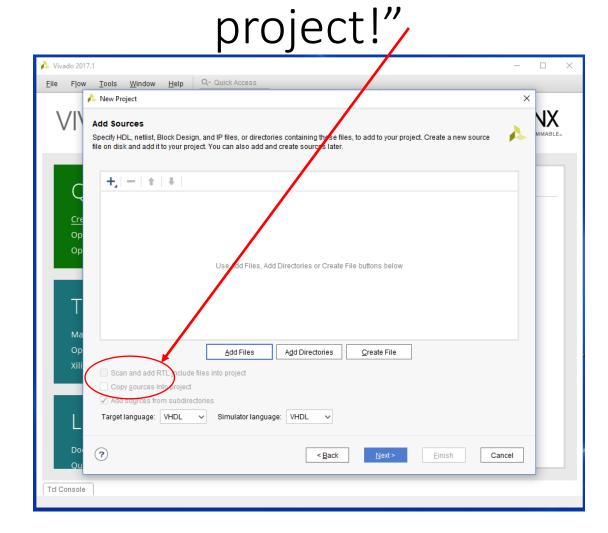
Select "RTL Project" and click "Next"



This is a very important step!

- After you create your project by clicking "next" on the last screen, your root project subdirectory is created
- Copy your source files into the root directory at this point, always keeping a copy of any work you did in case you mess up things as you start learning Vivado
- On the next screen, if you check "Copy sources into project, they will be automatically stuck in a subdirectory below the root project directory, and when you edit your sources in Vivado you will not be editing the files in the root directory – you will probably become very confused!

Select "Add Files" from the "Add Sources" GUI: Make sure you don't check "Copy sources into



Navigate to your project directory and select your source example.vhd file, then click "OK"

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Make sure the Target and Simulator Language is set to VHDL, then click "Next"

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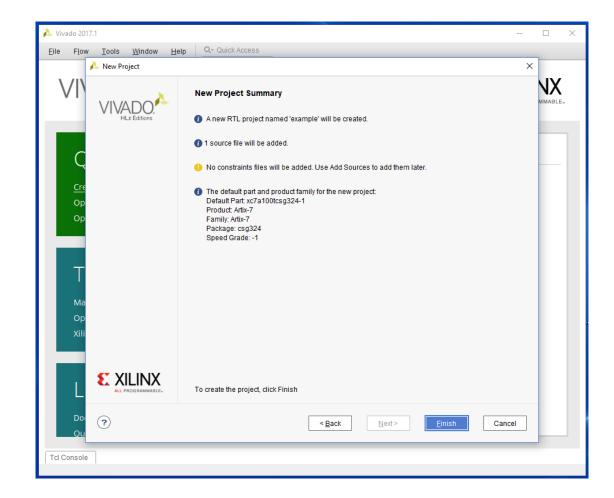
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Select the FPGA used on the CSE 260M demo board (Xilinx Artix 7 xc7a100tcsg324-1)

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Read the info screen and click "Finish"



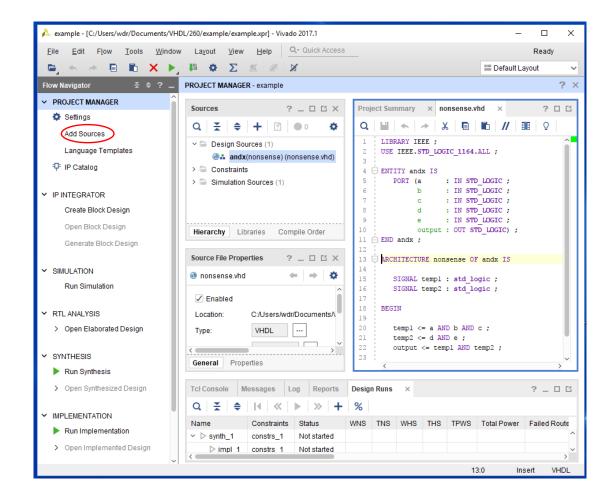
This is what you should get: A Vivado Project!

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The Vivado Project Manager allows you to view and edit your source file

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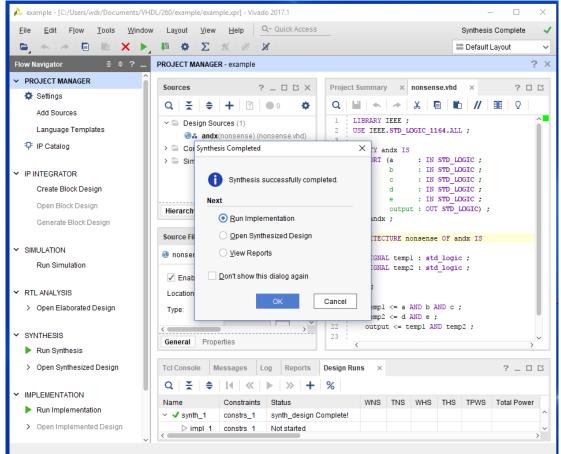
If you didn't create your VHDL source file ahead of time, you can use the GUI to create one



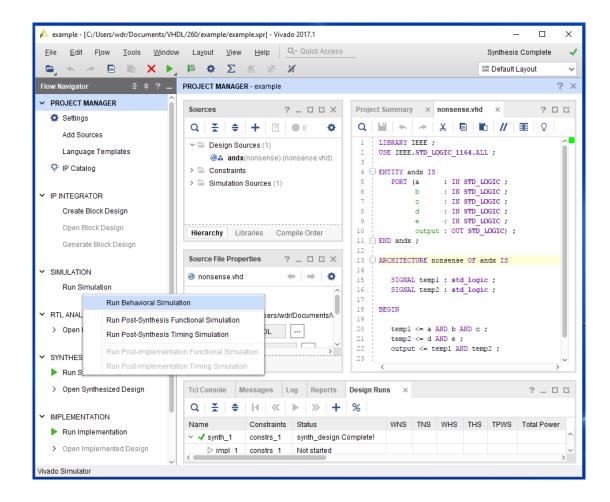
You have to synthesize your design before you can simulate it!

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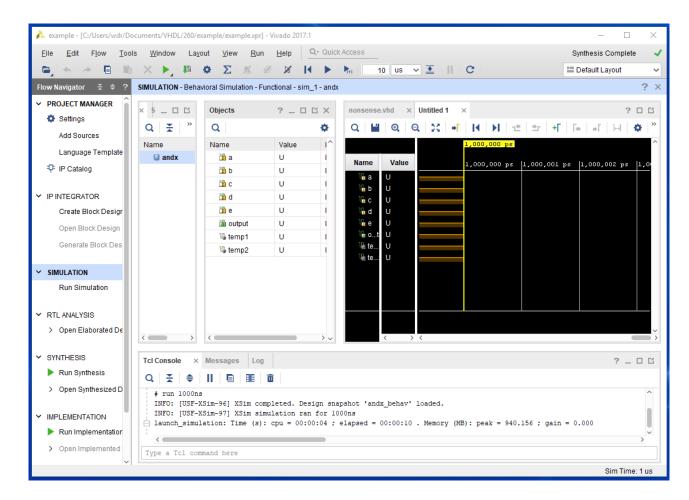
If you are just trying to simulate your design, you can select "Cancel" once you get a successful synthesis: No need to implement the design!



Run the simulator by right clicking on the "Run Simulation" menu item



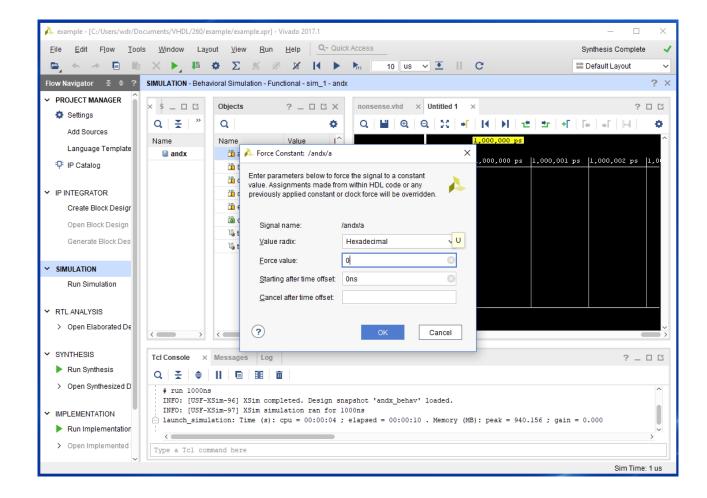
The simulator will take a few seconds to initialize (minutes for big designs)



Force the initial stimulus values by right clicking on each input in the "Objects" menu

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For this example, signal "a" is forced to logic 0



Run the simulator for 10 ns by typing "Run 10 ns" in the TCL Console

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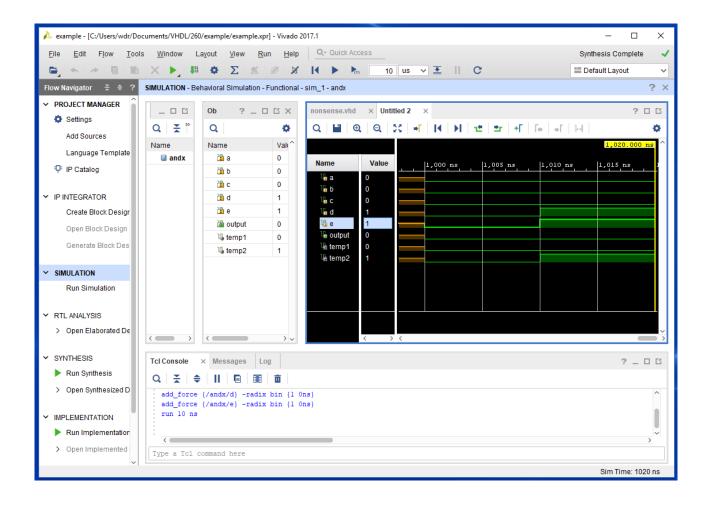
Use the zoom "magnifying glass" controls to adjust the simulation display

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Force additional stimulus values by right clicking on inputs in the "Objects" menu

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Run the simulator for an additional 10 ns after changing stimulus values using the TCL Console



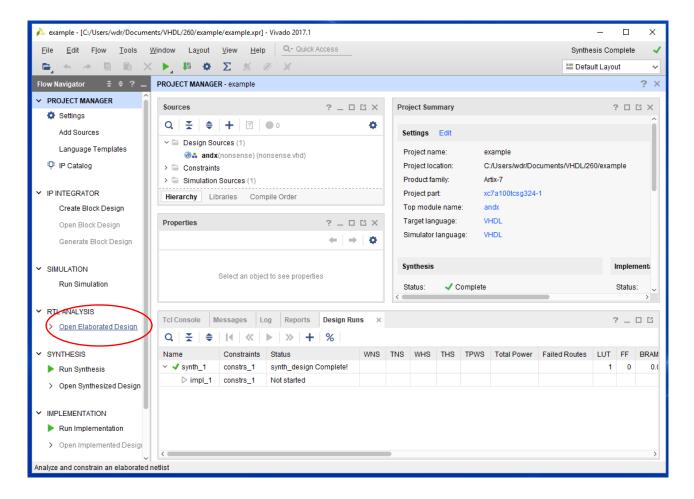
You can unlock the simulation window from the Vivado GUI

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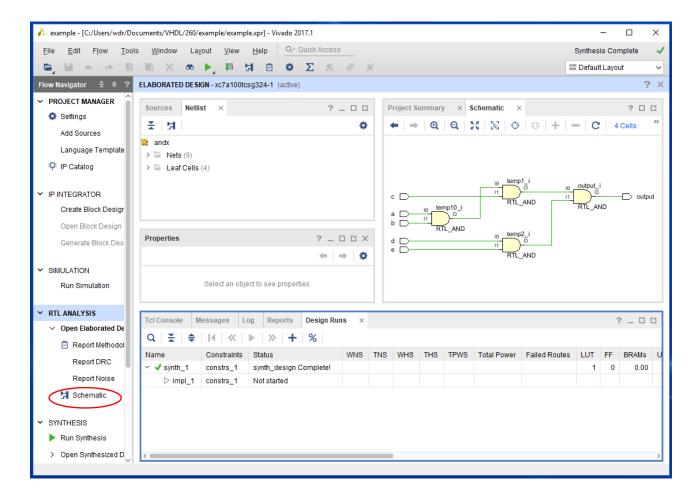
If you force all inputs to '1', the output will go high after you run an additional 10 ns!

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Open the Elaborated Design produced by the Synthesizer to see what your VHDL implied!



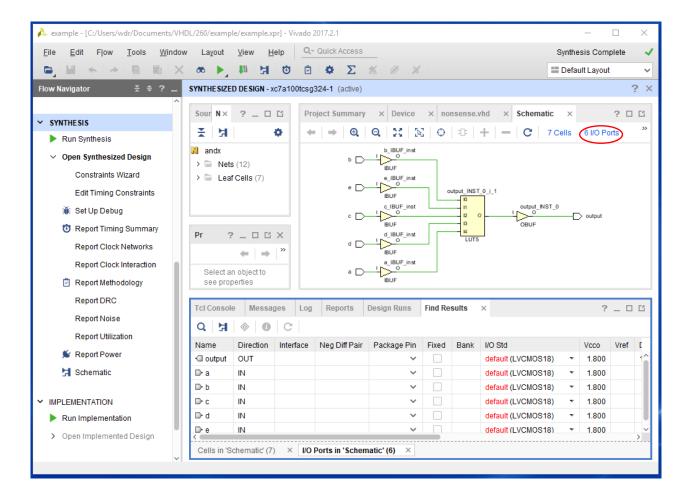
Notice that the schematic is not "optimal," but it is logically what your VHDL implied



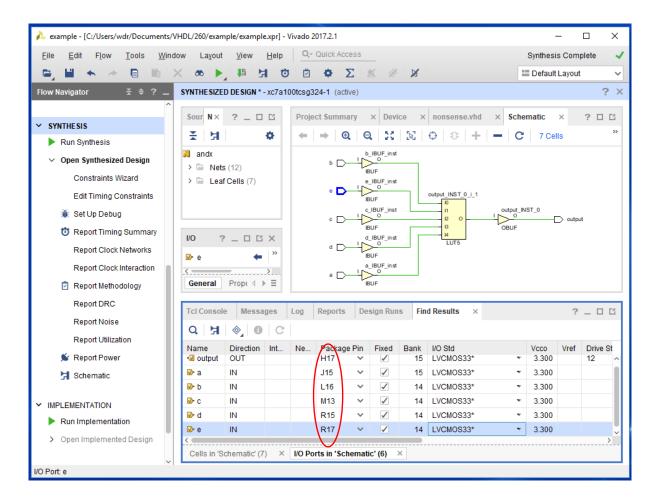
Open the Synthesized Design and view the schematic: A single LUT!

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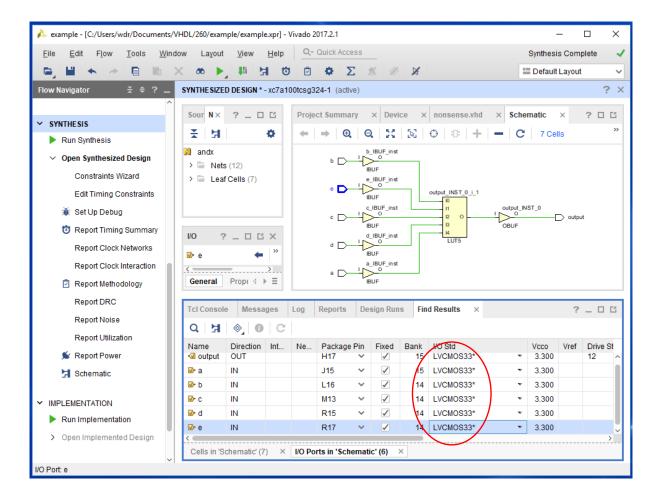
Expand the Schematic so you can see the "6 I/O Ports" option; select it to view the pins



Assign the pins to SW(4:0) and LD(0) using the documentation for the demo board



Make sure you use LVCMOS33 as discussed in class as the I/O standard!



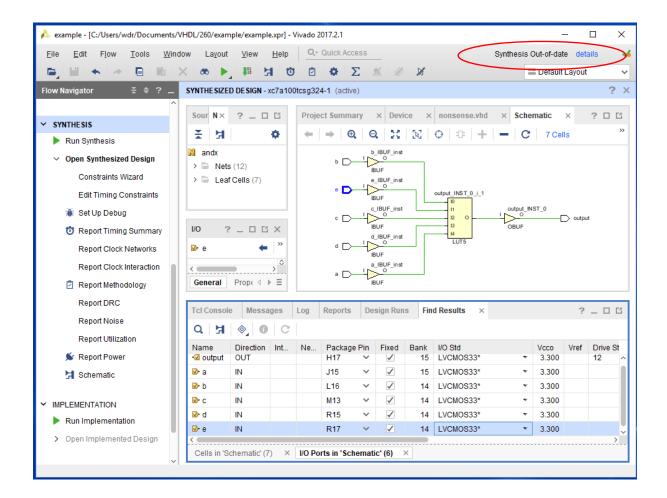
When you save the design, you will be prompted for a constraints file name

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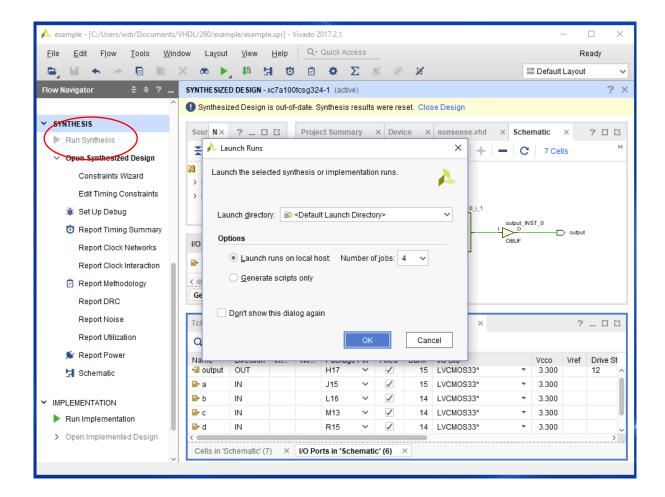
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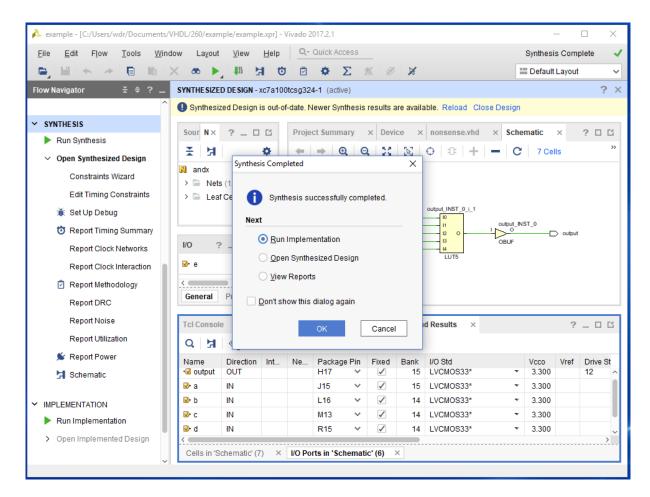
The synthesis will now be out of date because of your pin assignments and I/O standard selection



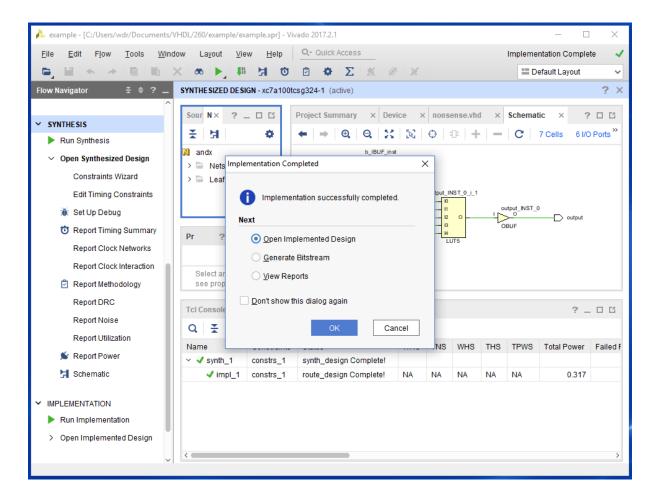
Run synthesis again...



This time, run select "Run Implemenation" by clicking "OK"



Select "Open Implemented Design" once place and route finishes



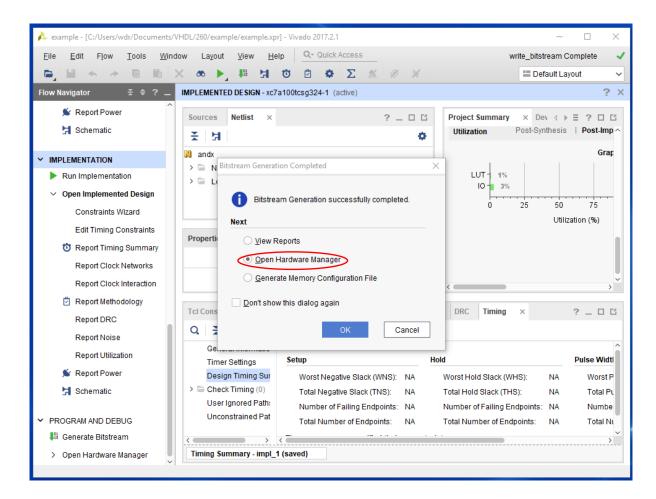
After looking at Reports, select "Generate Bitstream"

			- Vivado 2							
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Clock "OK" at the info screen...

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> Open Hardware Manager	Timing Summary - impl_1 (saved)	
Generate a programming file after imple	mentation	

When Generate Bitstream finishes, select "Open Hardware Manager"



After plugging in the Digilent FPGA board to your laptop or PC, select "Open Target"

🍌 example - [C:/Users/wdr/Documents/VH	DL/260/example/example.xpr] - Vivado 2017.2.1	– 🗆 X
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✓ Open Implemented Design	Q, 素 ♦ Ø ▶ ≯ Available Targets of	wdr/Documents/VHDL/260/example/example.sri ×
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Report Clock Interaction		6 b : IN STD_LOGIC ; 7 c : IN STD_LOGIC :
Report Methodology		7 c : IN STD_LOGIC ; 8 d : IN STD_LOGIC ;
Report DRC		9 e : IN STD_LOGIC ; 10 output : OUT STD_LOGIC) ;
	Select an object to see properties	11
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🗯 Report Power	Tcl Console × Messages Serial I/O Links Seria	IVO Scans ? _ 🗆 🖸
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Y PROGRAM AND DEBUG	INFO: [Labtools 27-2221] Launch Output:	^
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✓ Open Hardware Manager	**** Build date : Aug 9 2017-16:50:22 ** Copyright 1986-2017 Xilinx, Inc. All	Distance Descound
Open Target	copyright 1906-2017 Allinx, Inc. All	
Program Device		×
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Automatically connect to local hardware targ	et	

Select "Program device" after you see the Hardware Manager connect to the FPGA

À example - [C:/Users/wdr/Documents/VH	DL/260/example/example.xpr] - Vivado 2017.2.1	– 🗆 X
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∨ Open Hardware Manager	<pre>Fefresh hw_device -update_hw_probes false [linder INFO: [Labtools 27-1435] Device xc7al00t (JTAG of INFO: [Labtools 27-1435] Device xc7al00t</pre>	
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Program Device		~ ~ ~
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Once the FPGA is programmed, you can test your design using the switches and LEDs!

🍌 example - [C:/Users/wdr/Documents/VH	DL/260/example/example.xpr] - Vivado 2017.2.1	– 🗆 X
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Flow Navigator	HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210292746689A	? ×
IMPLEMENTATION	There are no debug cores. Program device Refresh device Hardware	nonsense.vhd ? 다 더 ×
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	Q 素 ≑ 🖻 🖩 🏛	
 ✓ PROGRAM AND DEBUG ↓^{III} Generate Bitstream ✓ Open Hardware Manager 	WARNING: [Labtools 27-3361] The debug hub core was not Resolution: 1. Make sure the clock connected to the debug hub (dbg_ 2. Make sure the BSCAN_SWITCH_USER_MASK device property	hub) core is a free running clock and 7 in Vivado Hardware Manager reflects t
Open Target Program Device	For more details on setting the scan chain property, co	Insult the vivado Debug and Frogramming
Add Configuration Memory D 🧅	Type a Tcl command here	