Vivado V2017.2 Tutorial

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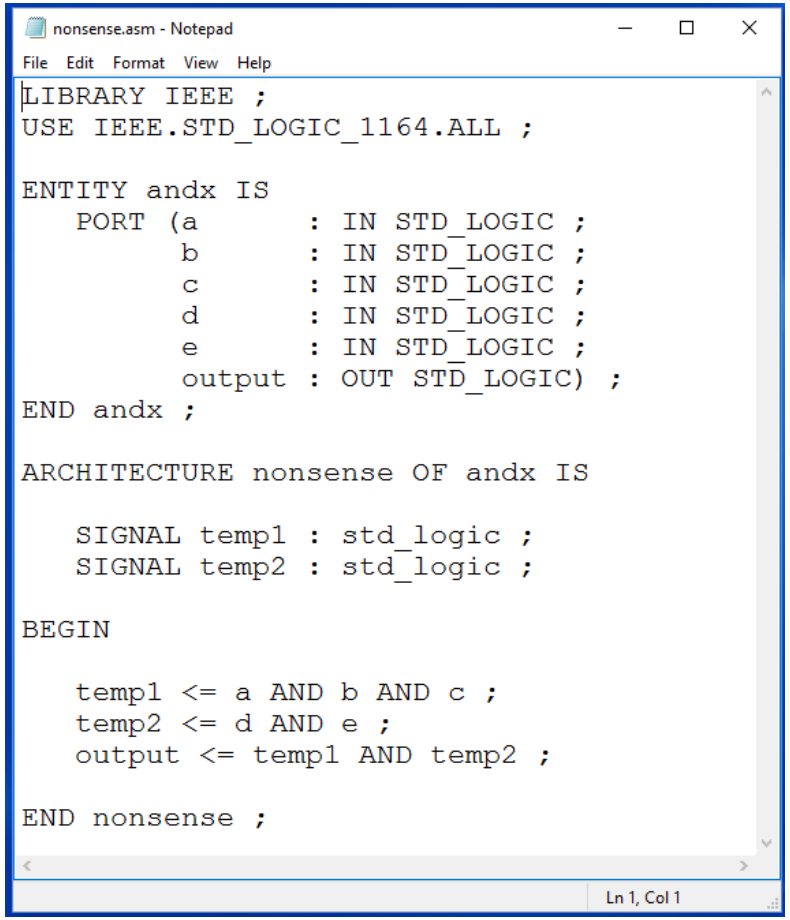
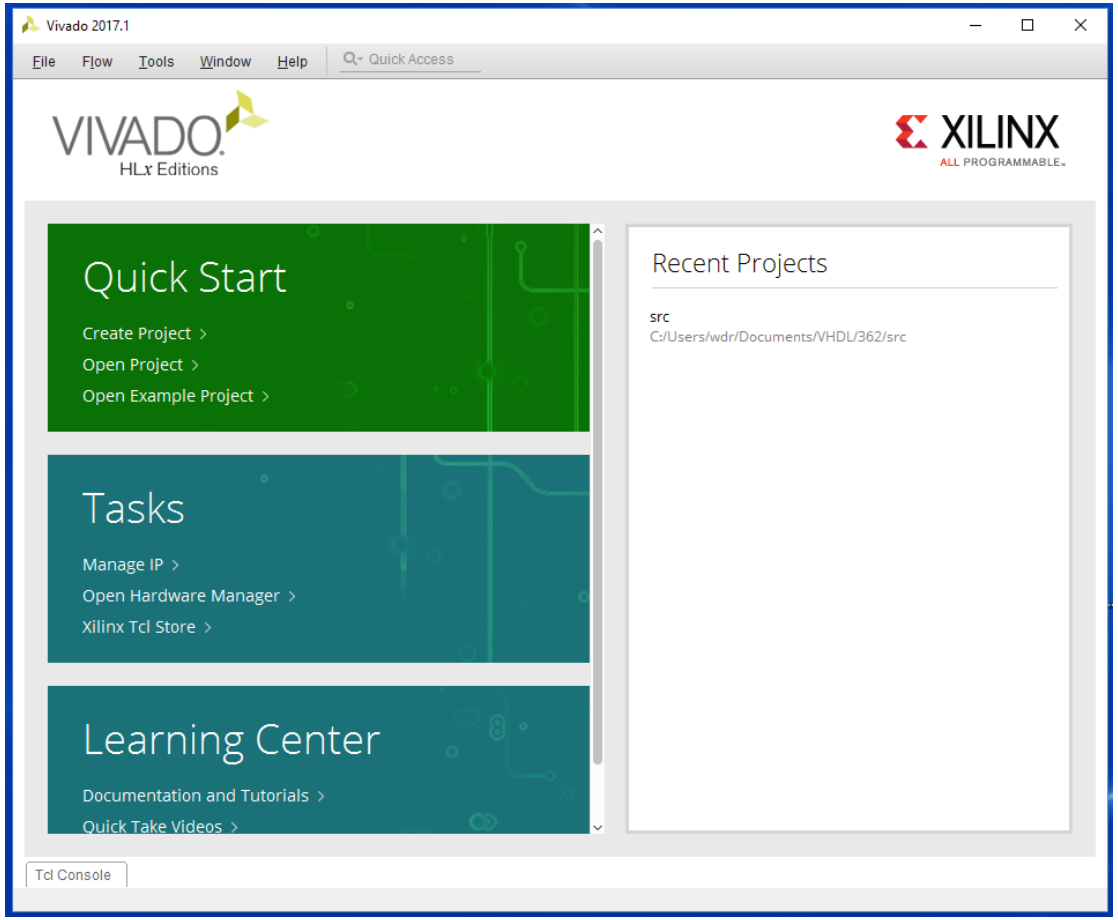
September 19, 2017

Updated Septembert 10, 2018

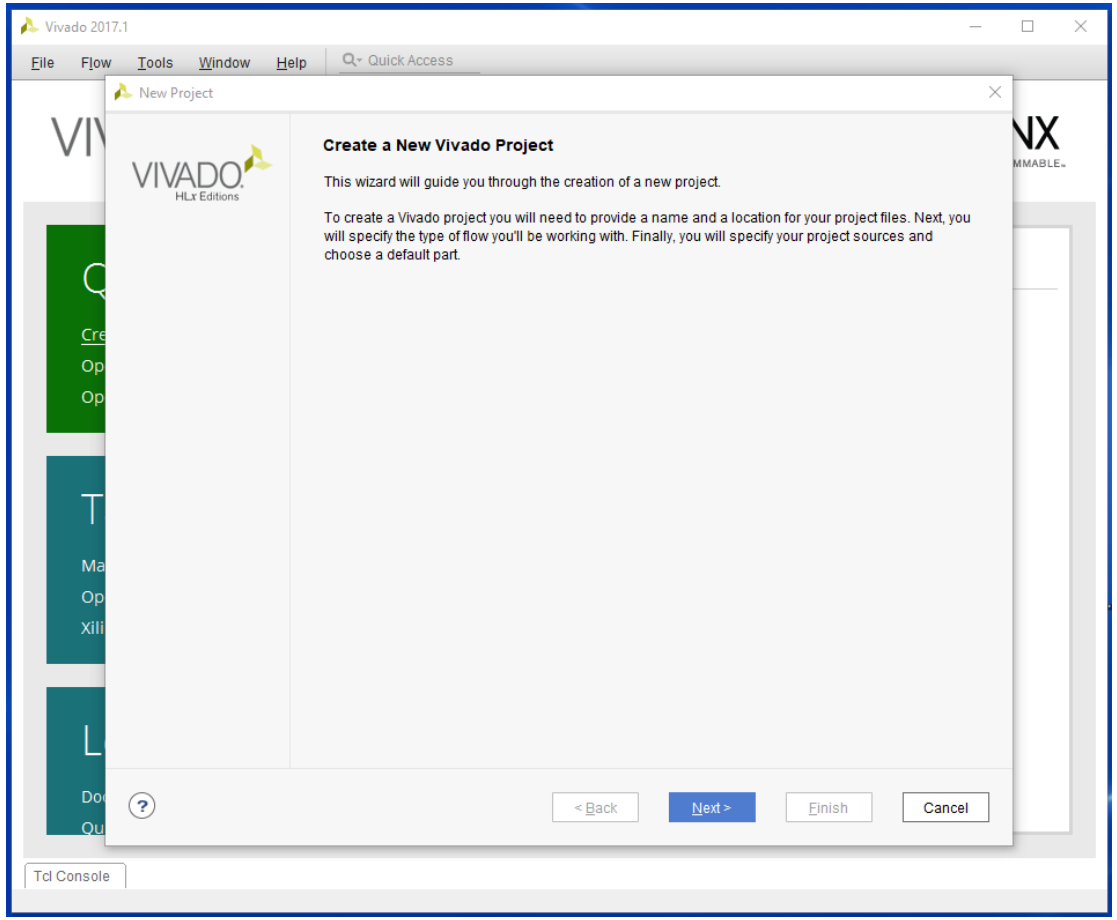
Create your source using a text editor: example.vhd



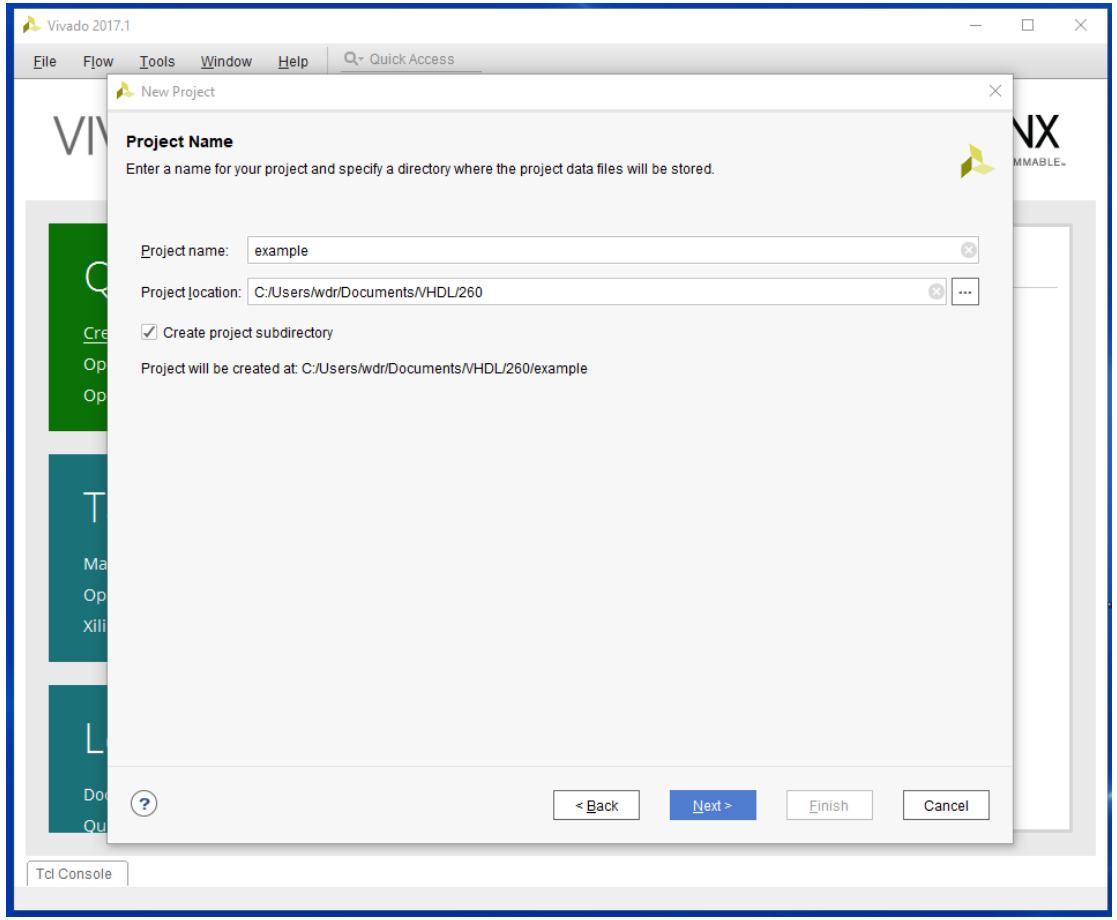
Run Vivado and select “Create New Project”



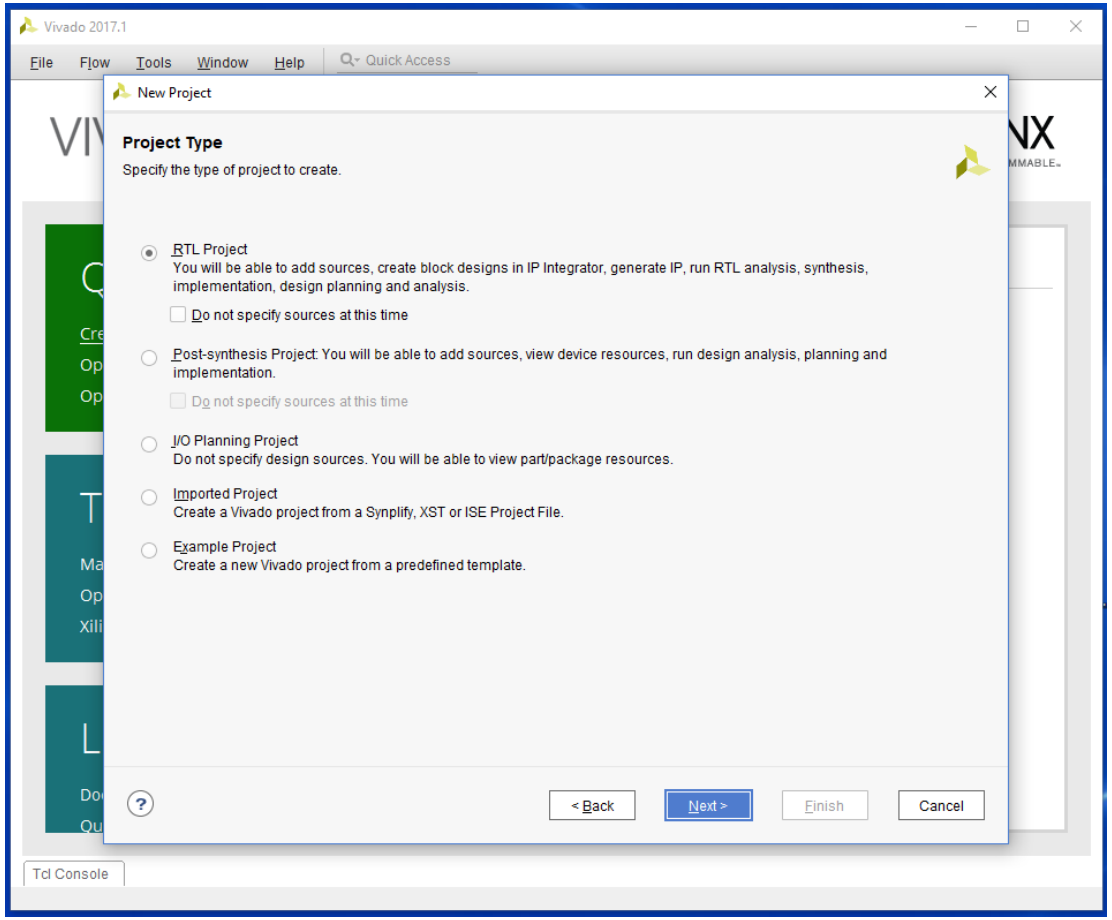
Read the info screen and click “Next”



Select the project directory and name your project



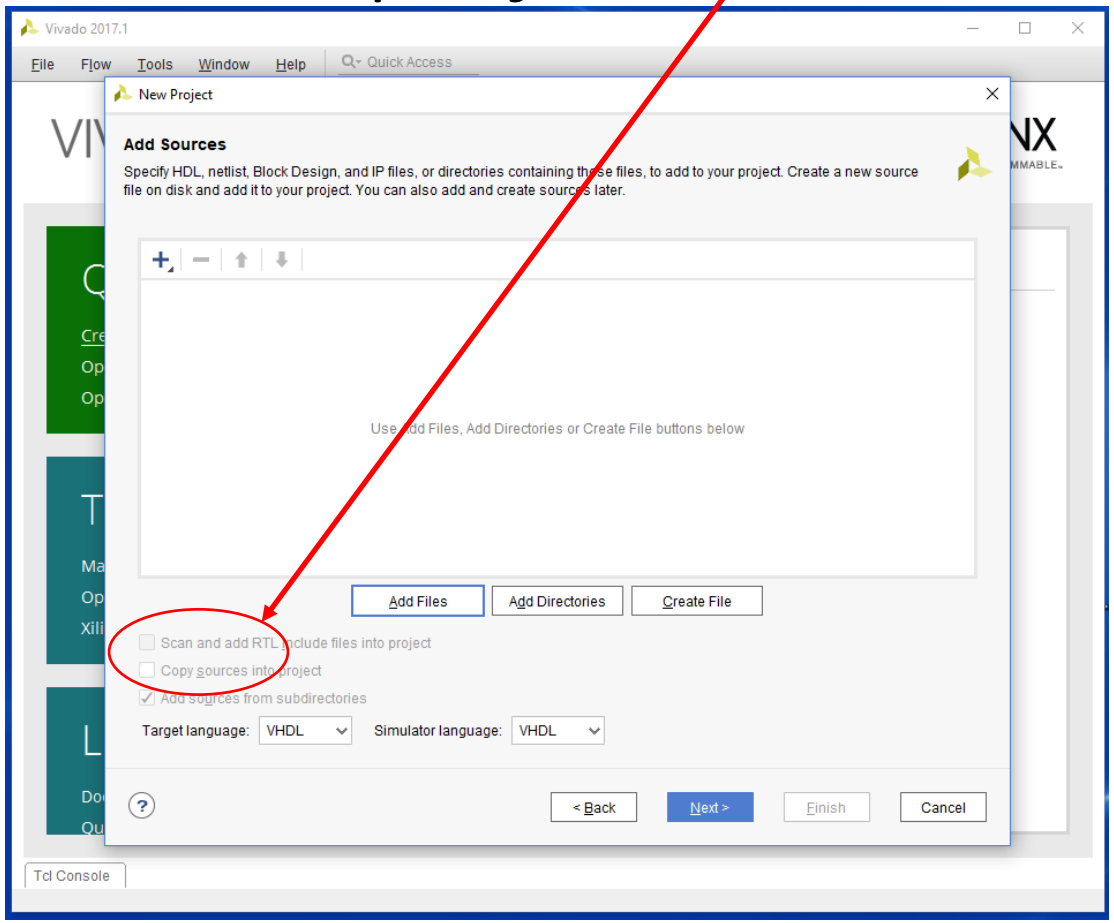
Select “RTL Project” and click “Next”



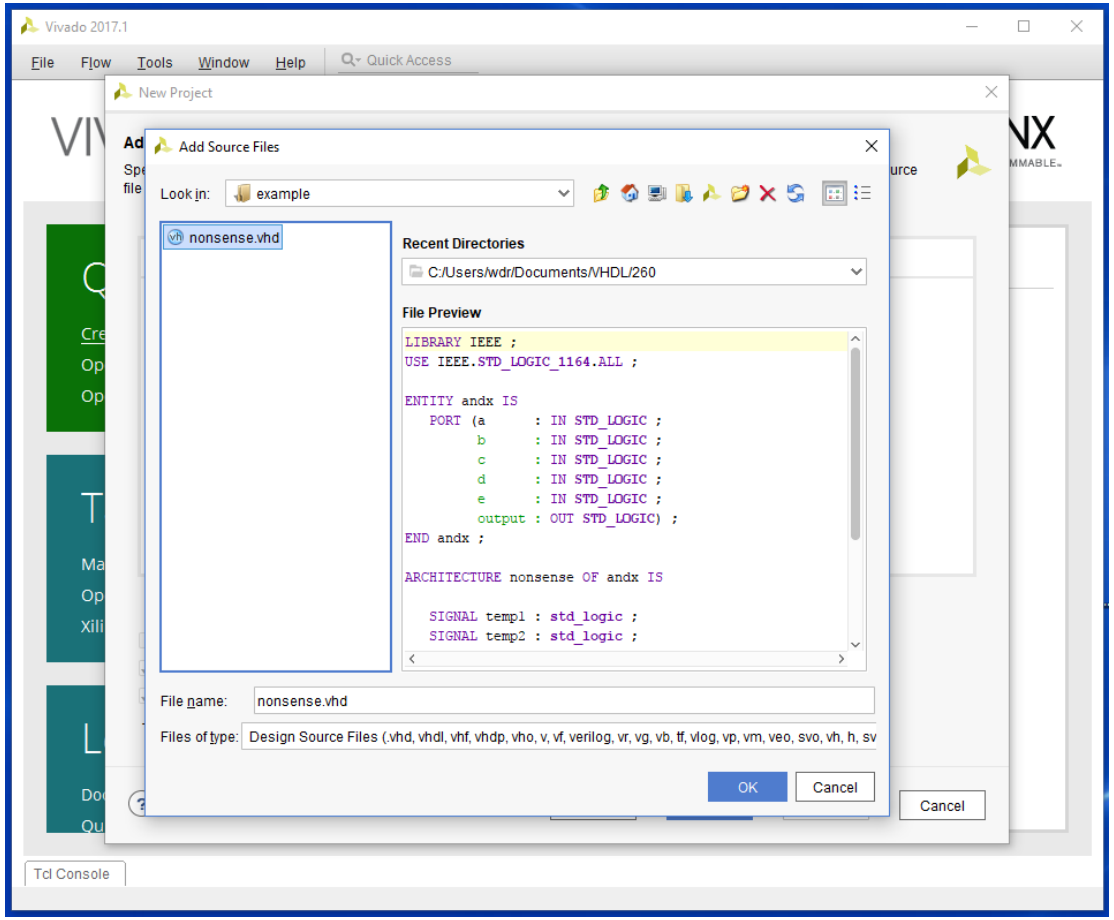
This is a very important step!

- After you create your project by clicking “next” on the last screen, your root project subdirectory is created
- Copy your source files into the root directory at this point, always keeping a copy of any work you did in case you mess up things as you start learning Vivado
- On the next screen, if you check “Copy sources into project, they will be automatically stuck in a subdirectory below the root project directory, and when you edit your sources in Vivado you will not be editing the files in the root directory – you will probably become very confused!

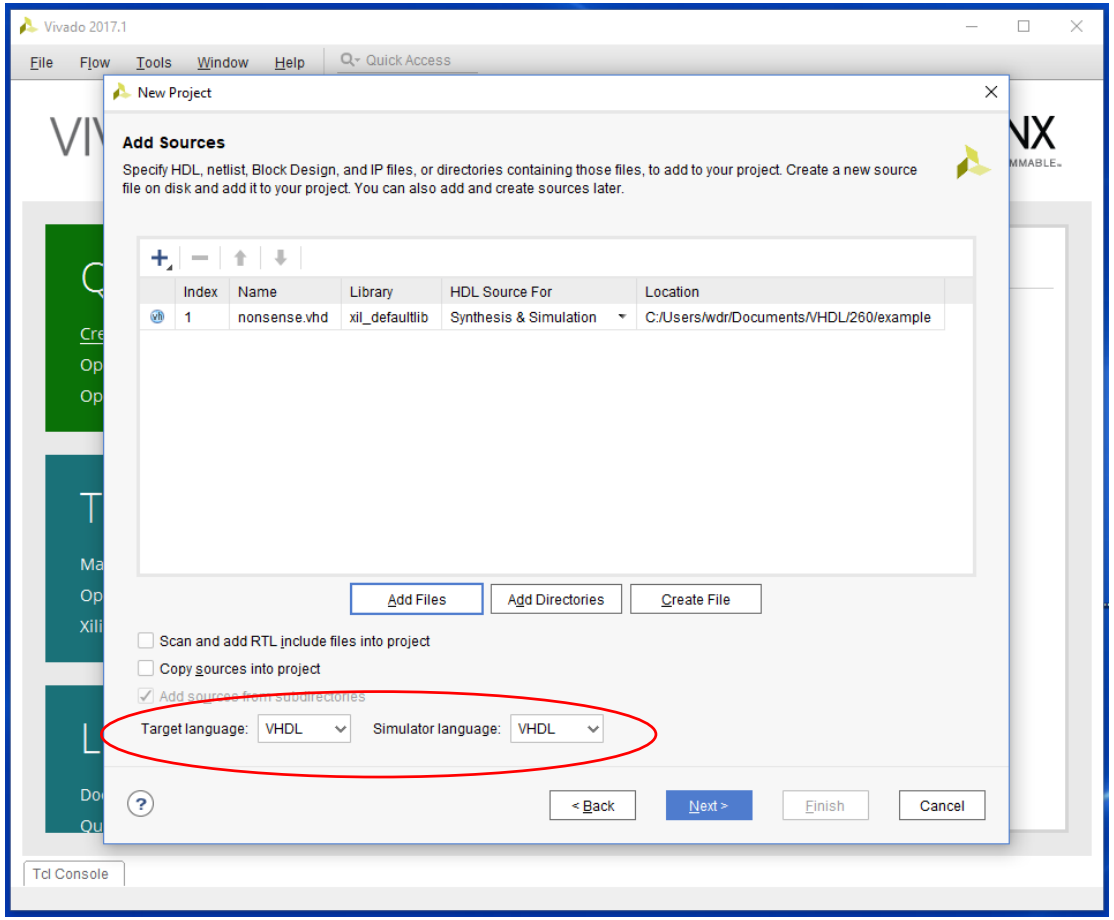
Select “Add Files” from the “Add Sources” GUI: Make sure you don’t check “Copy sources into project!”



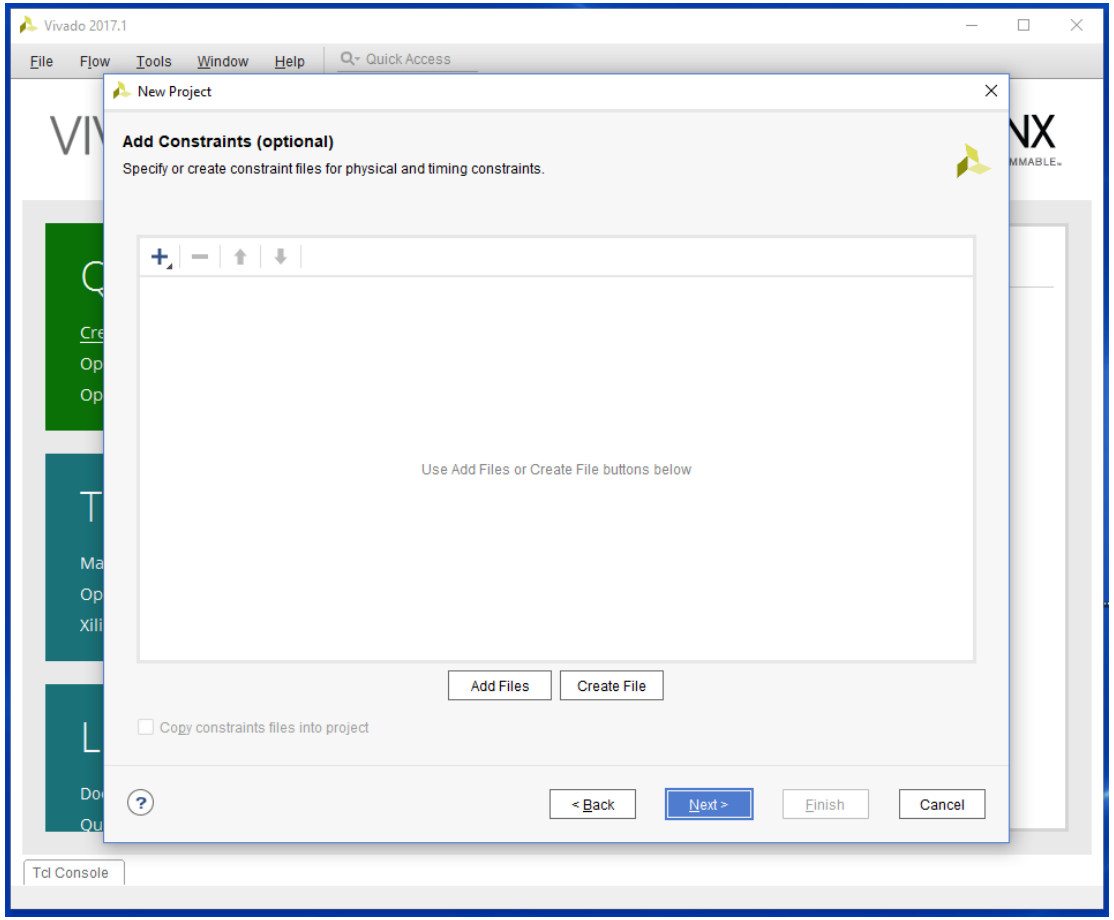
Navigate to your project directory and select your source example.vhd file, then click “OK”



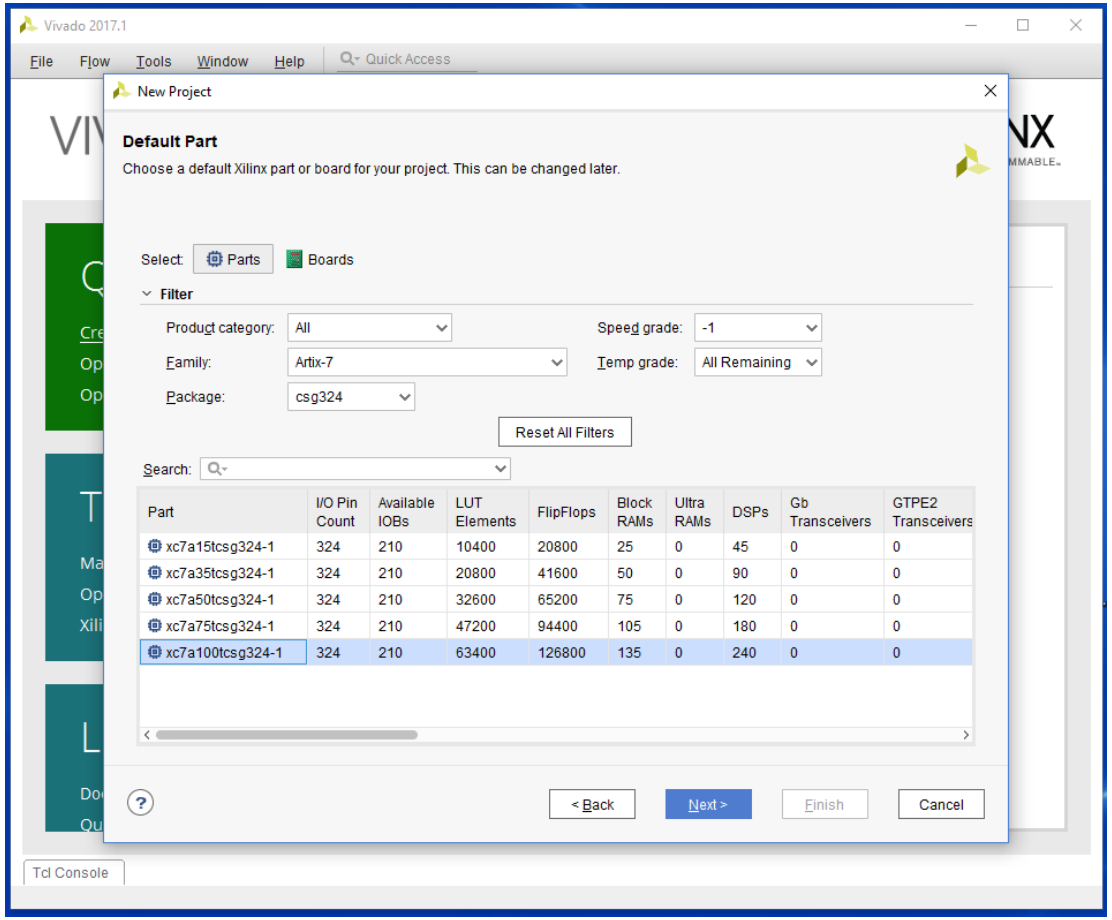
Make sure the Target and Simulator Language is set to VHDL, then click “Next”



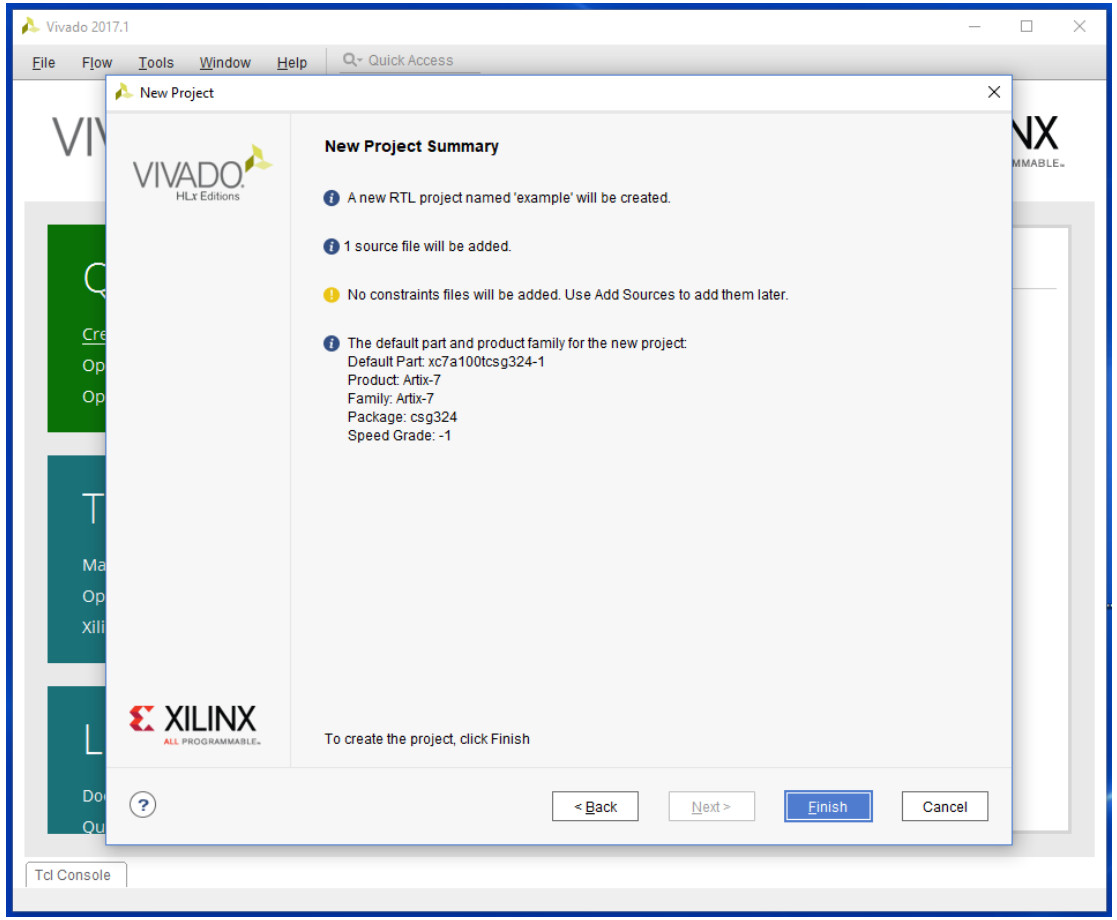
Don’t add add constraints now, just select “Next”



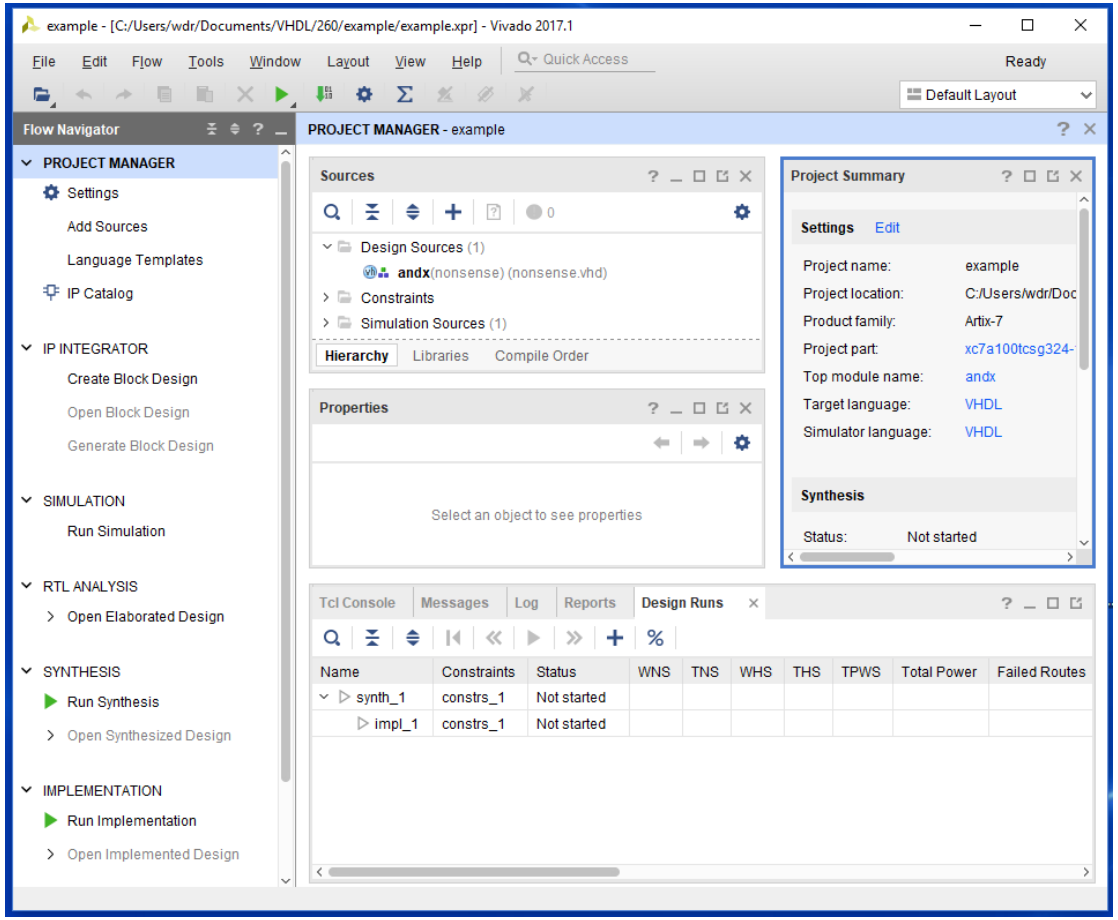
Select the FPGA used on the CSE 260M demo board (Xilinx Artix 7 xc7a100tcsg324-1)



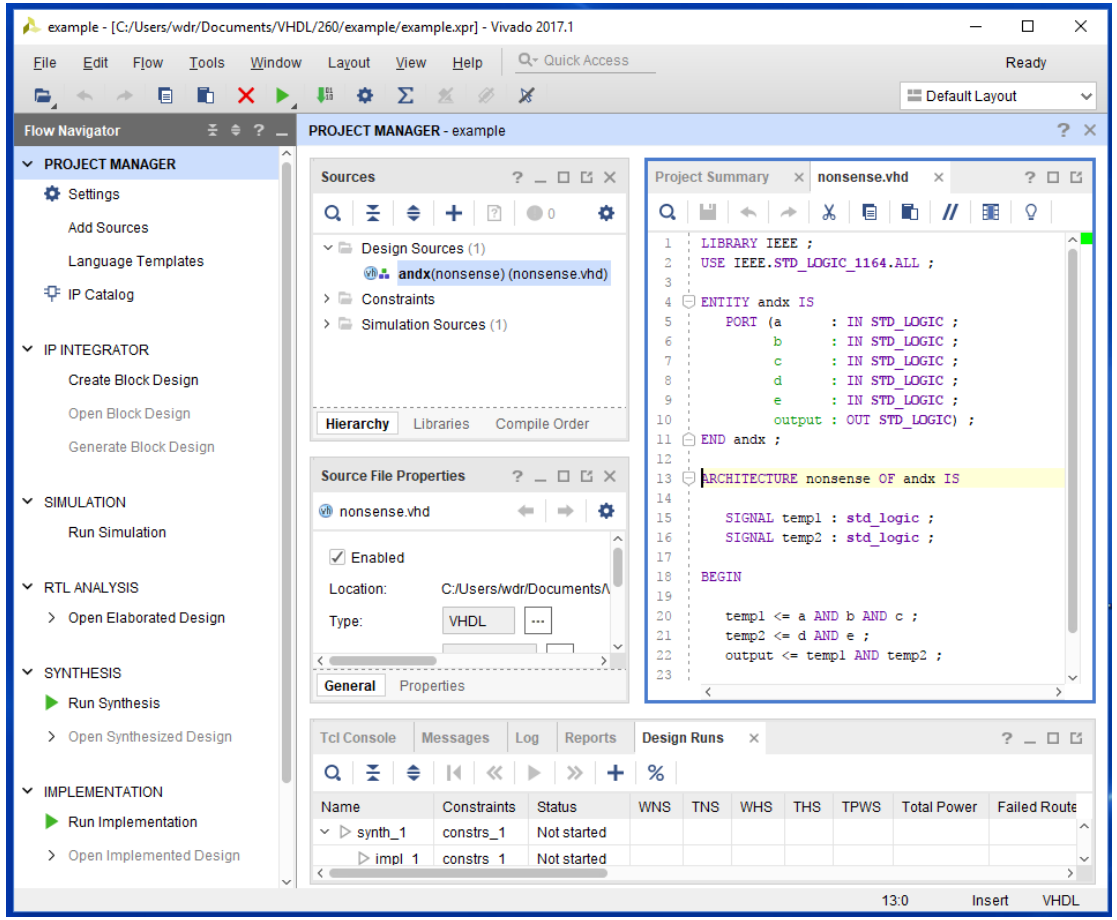
Read the info screen and click “Finish”



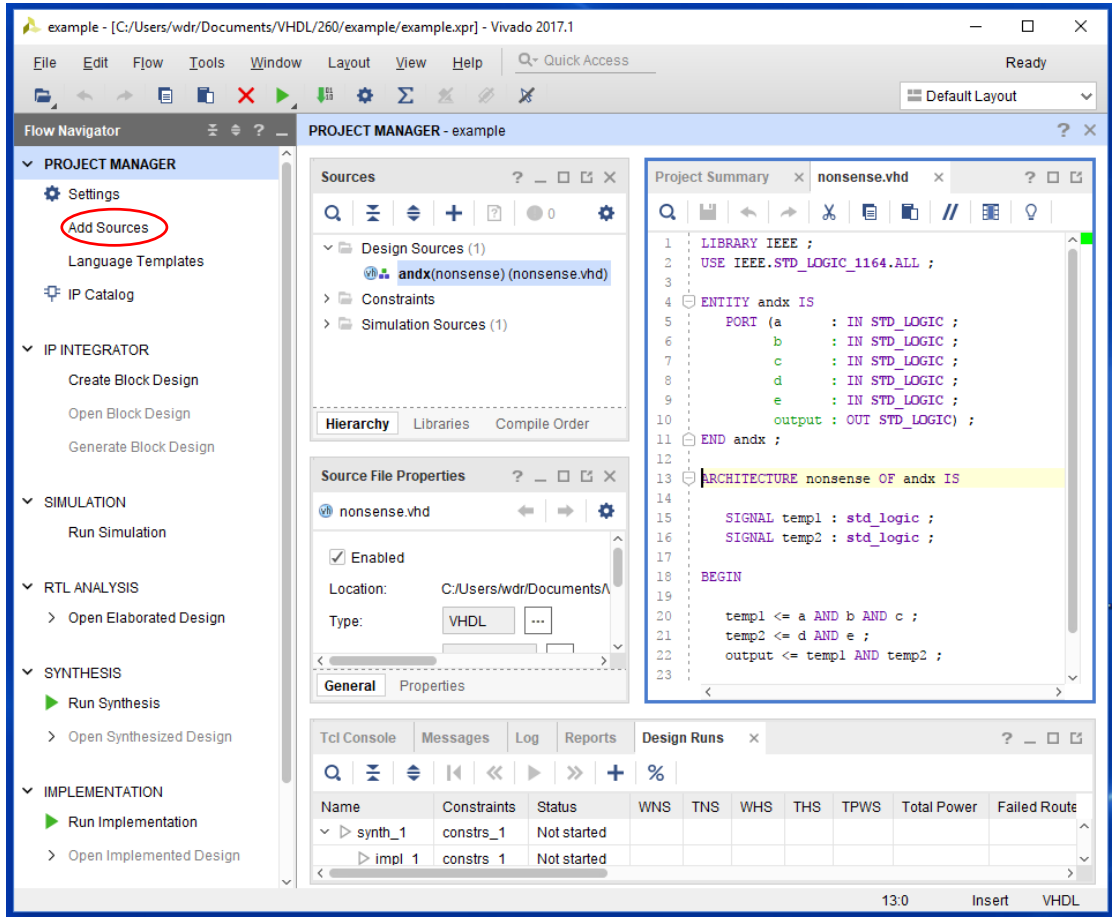
This is what you should get: A Vivado Project!



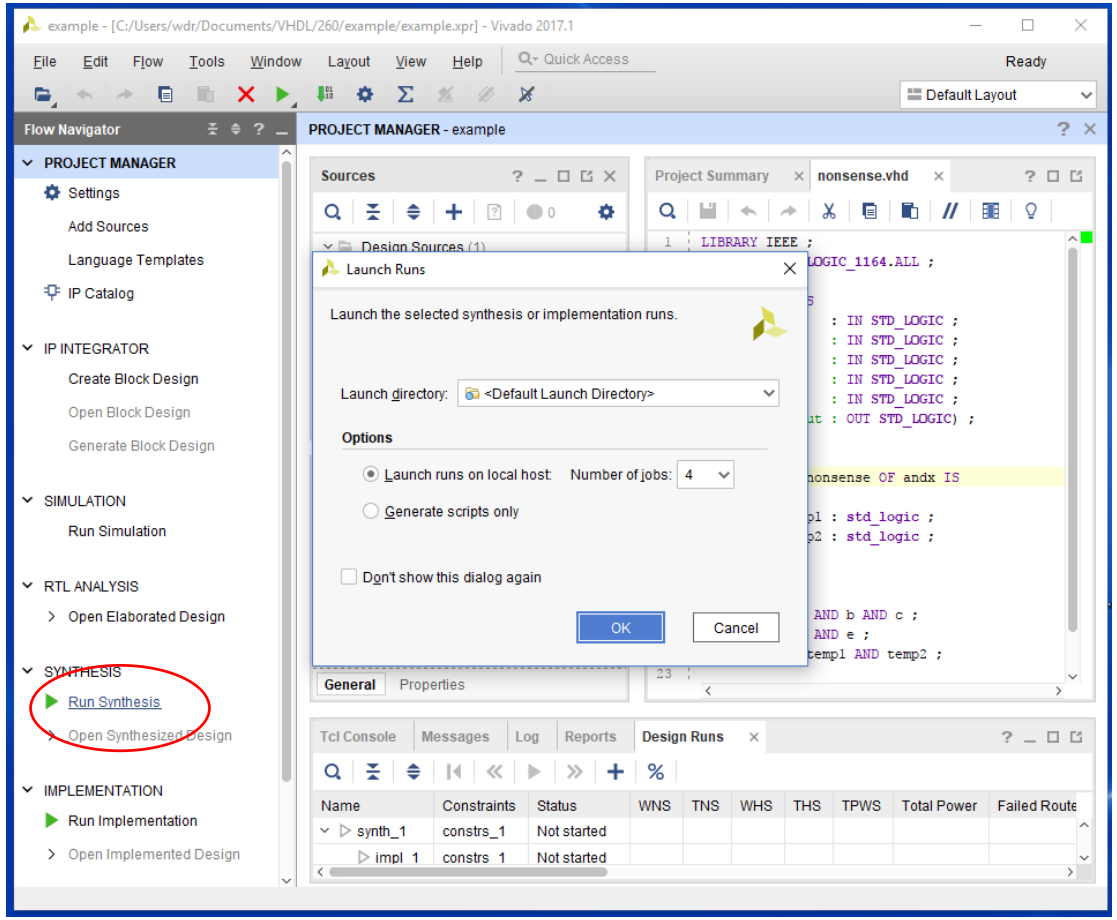
The Vivado Project Manager allows you to view and edit your source file



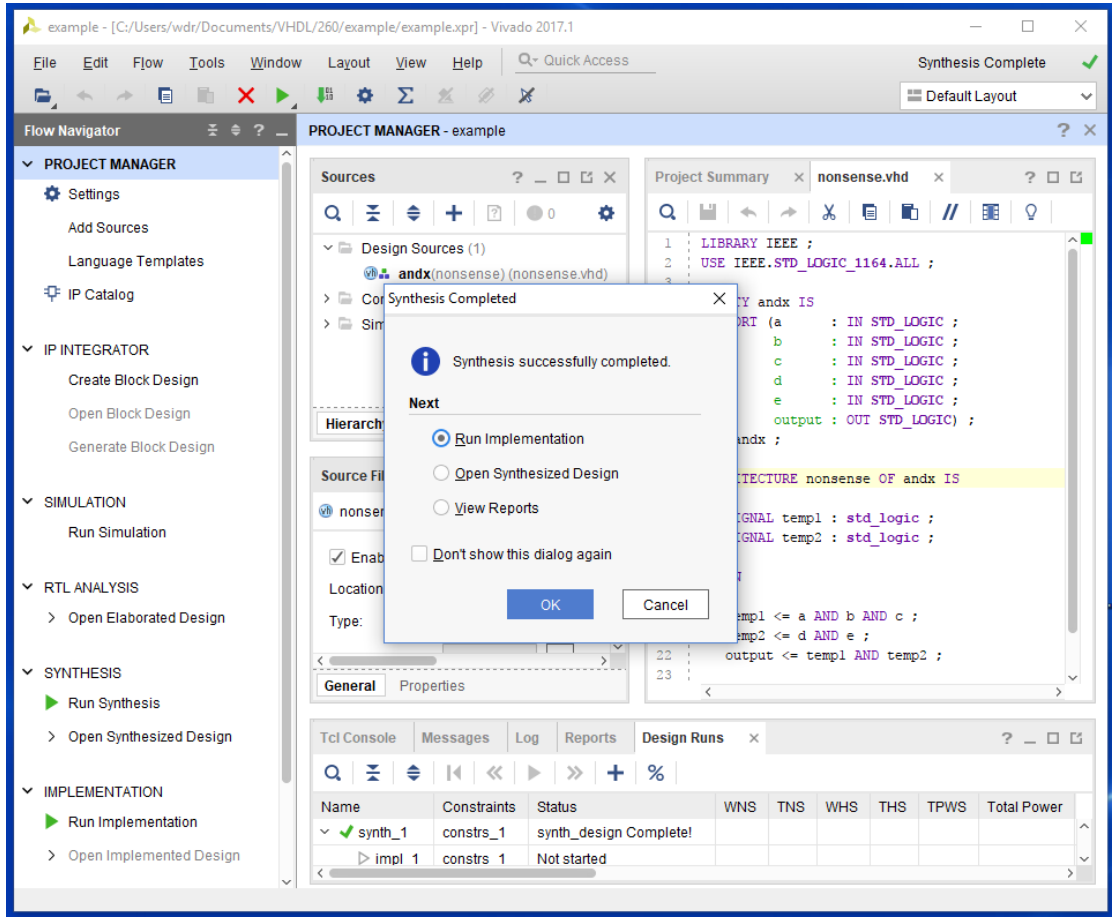
If you didn’t create your VHDL source file ahead of time, you can use the GUI to create one



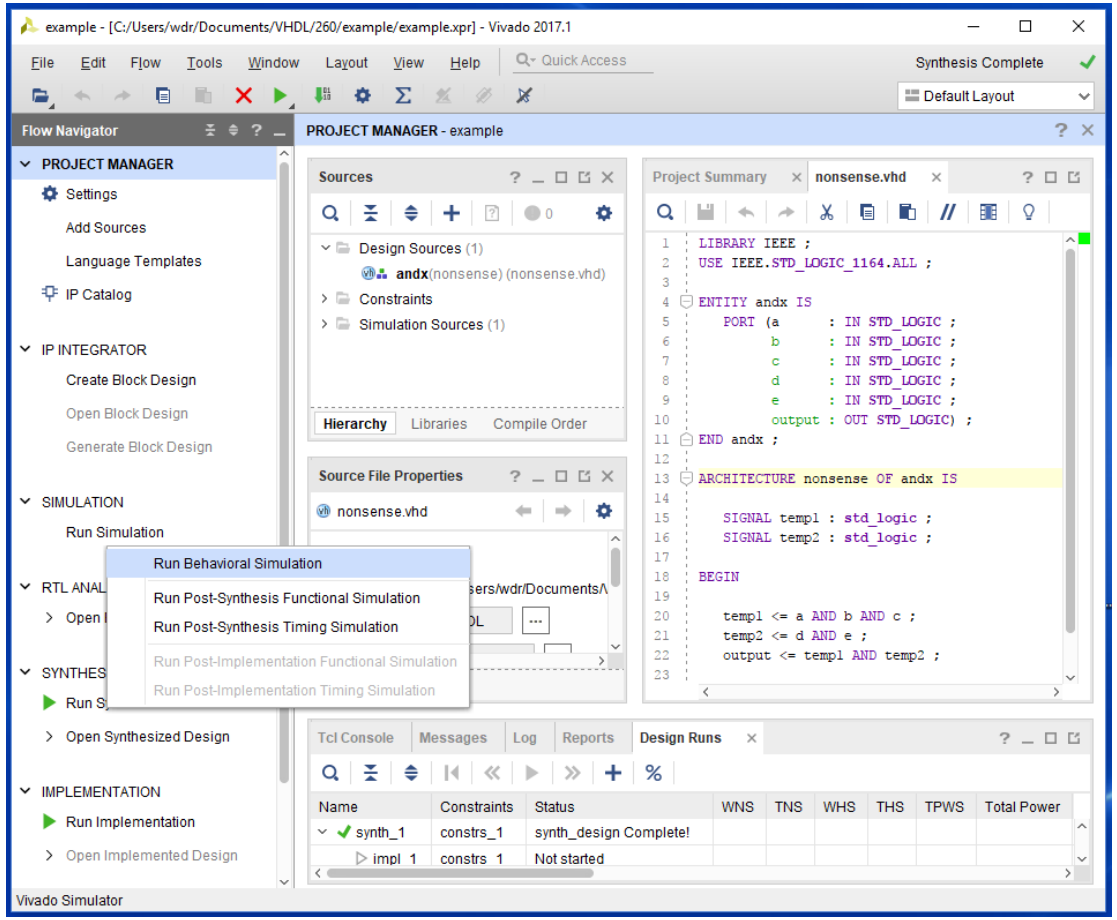
You have to synthesize your design before you can simulate it!



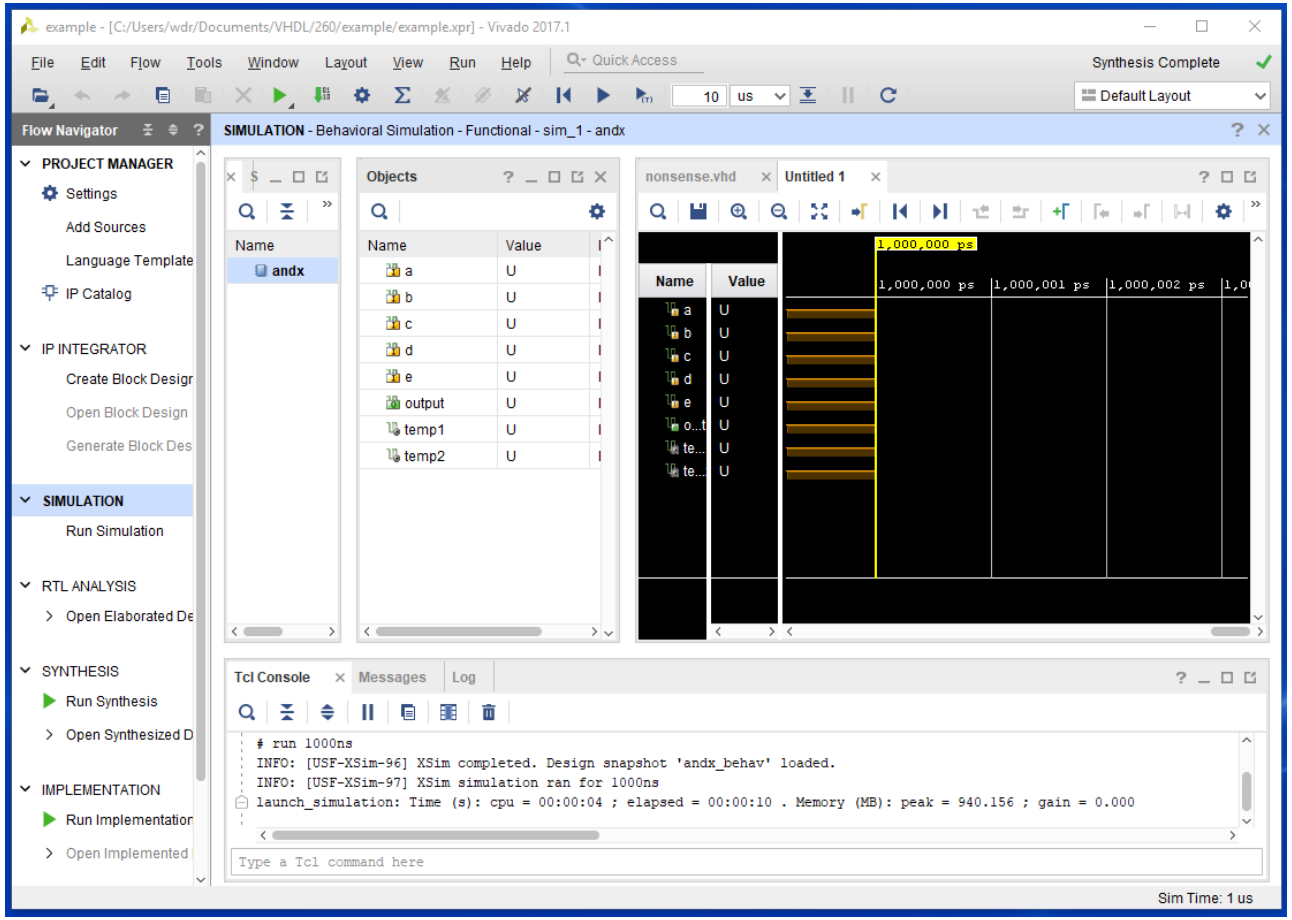
If you are just trying to simulate your design, you can select “Cancel” once you get a successful synthesis: No need to implement the design!



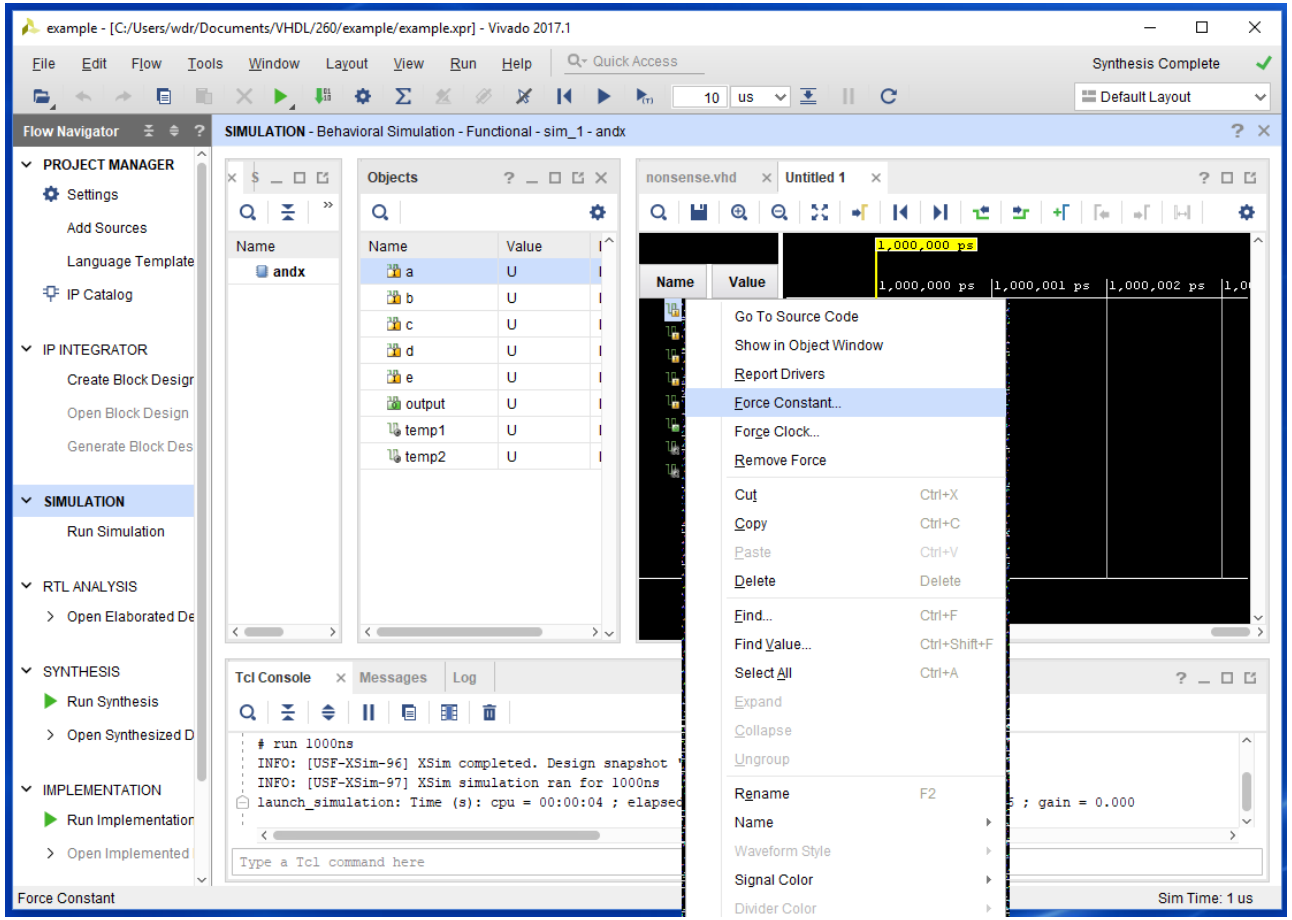
Run the simulator by right clicking on the “Run Simulation” menu item



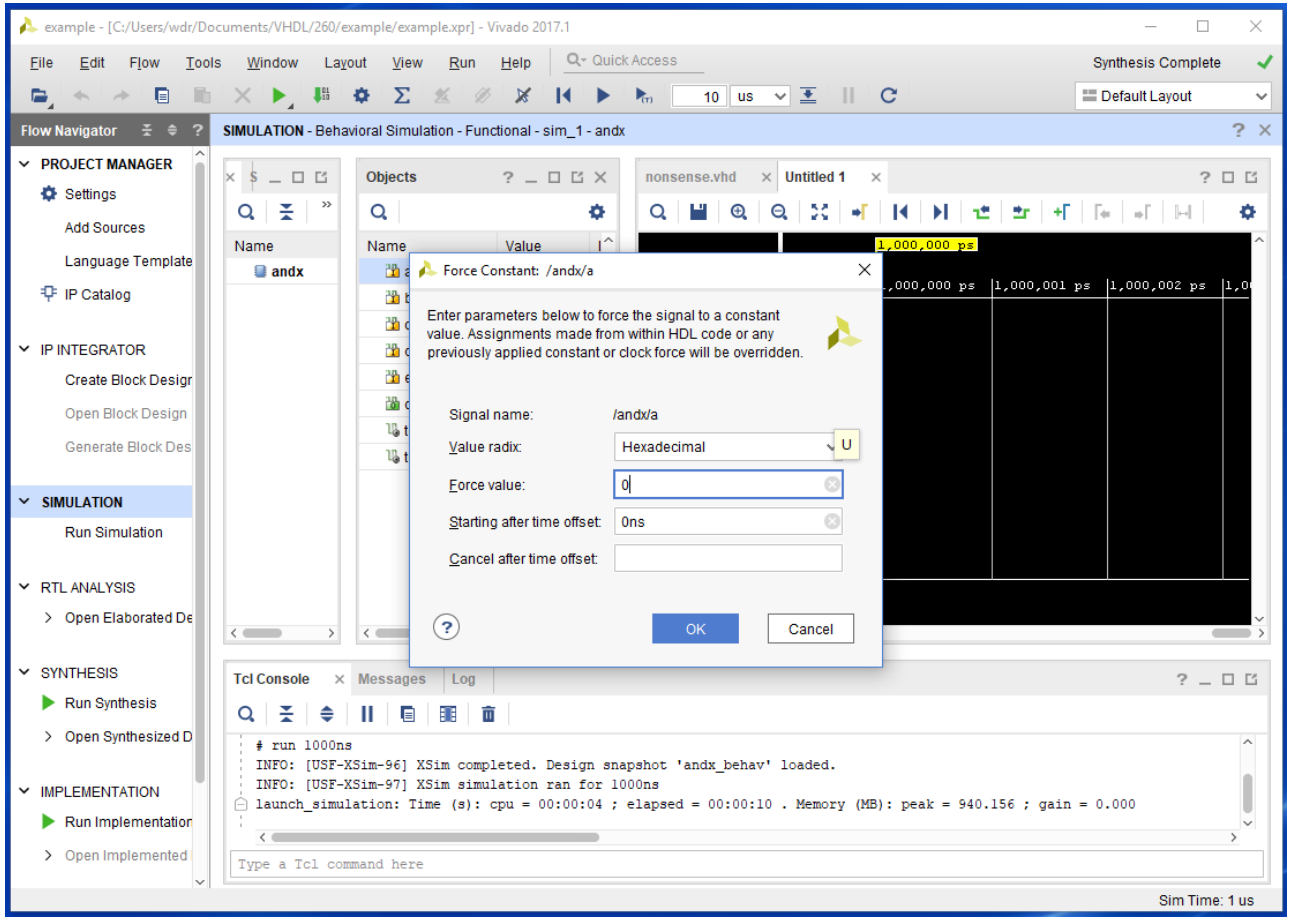
The simulator will take a few seconds to initialize (minutes for big designs)



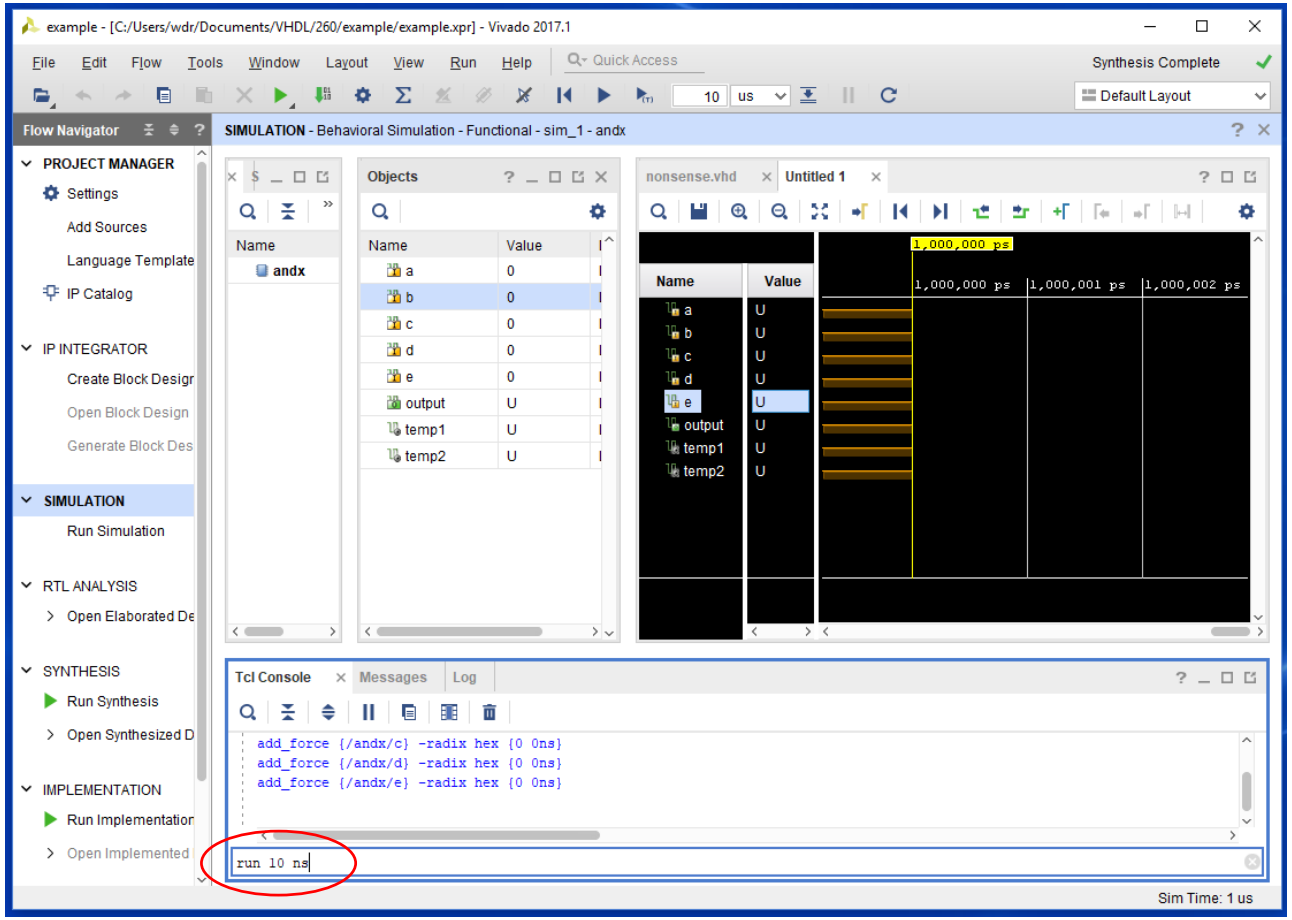
Force the initial stimulus values by right clicking on each input in the “Objects” menu



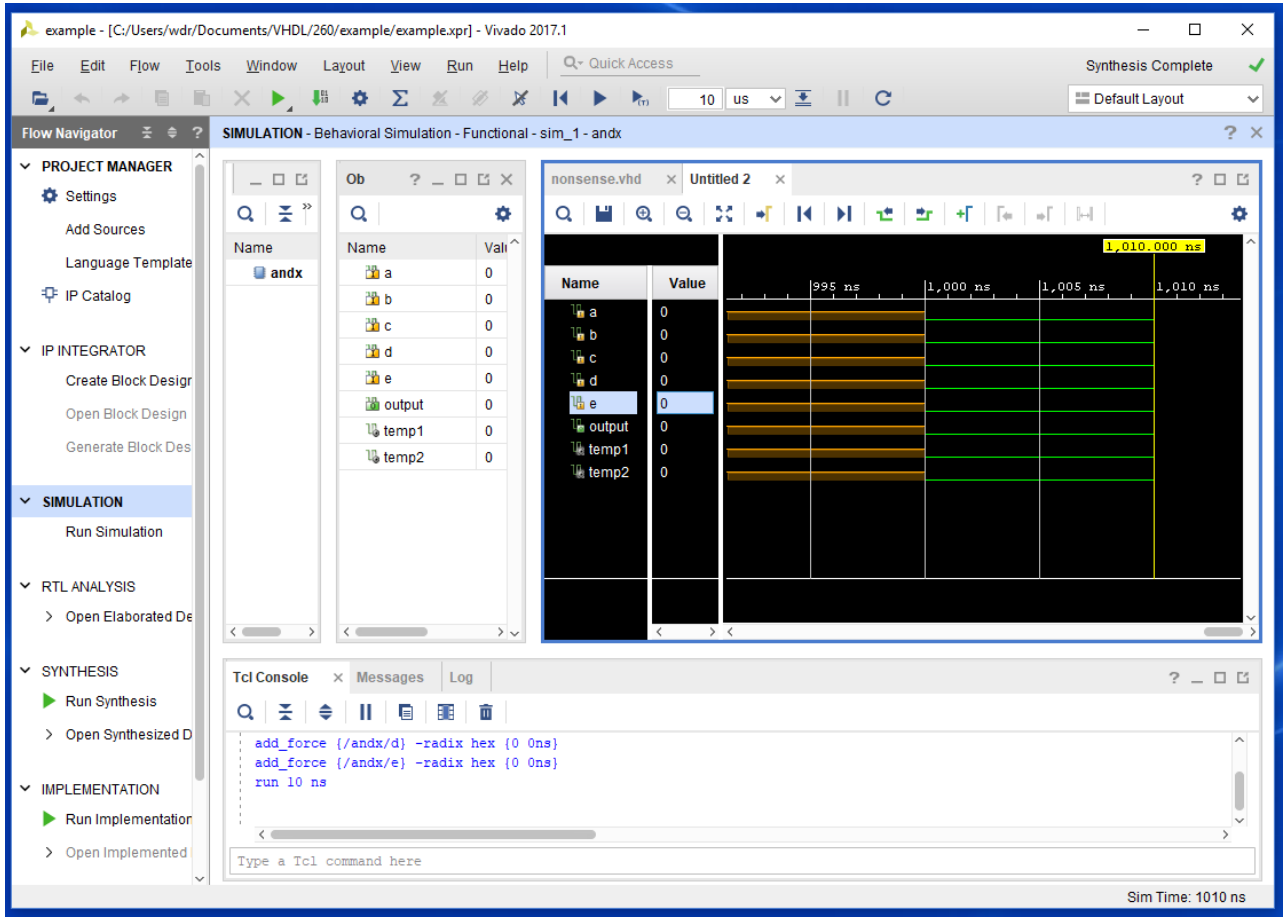
For this example, signal “a” is forced to logic 0



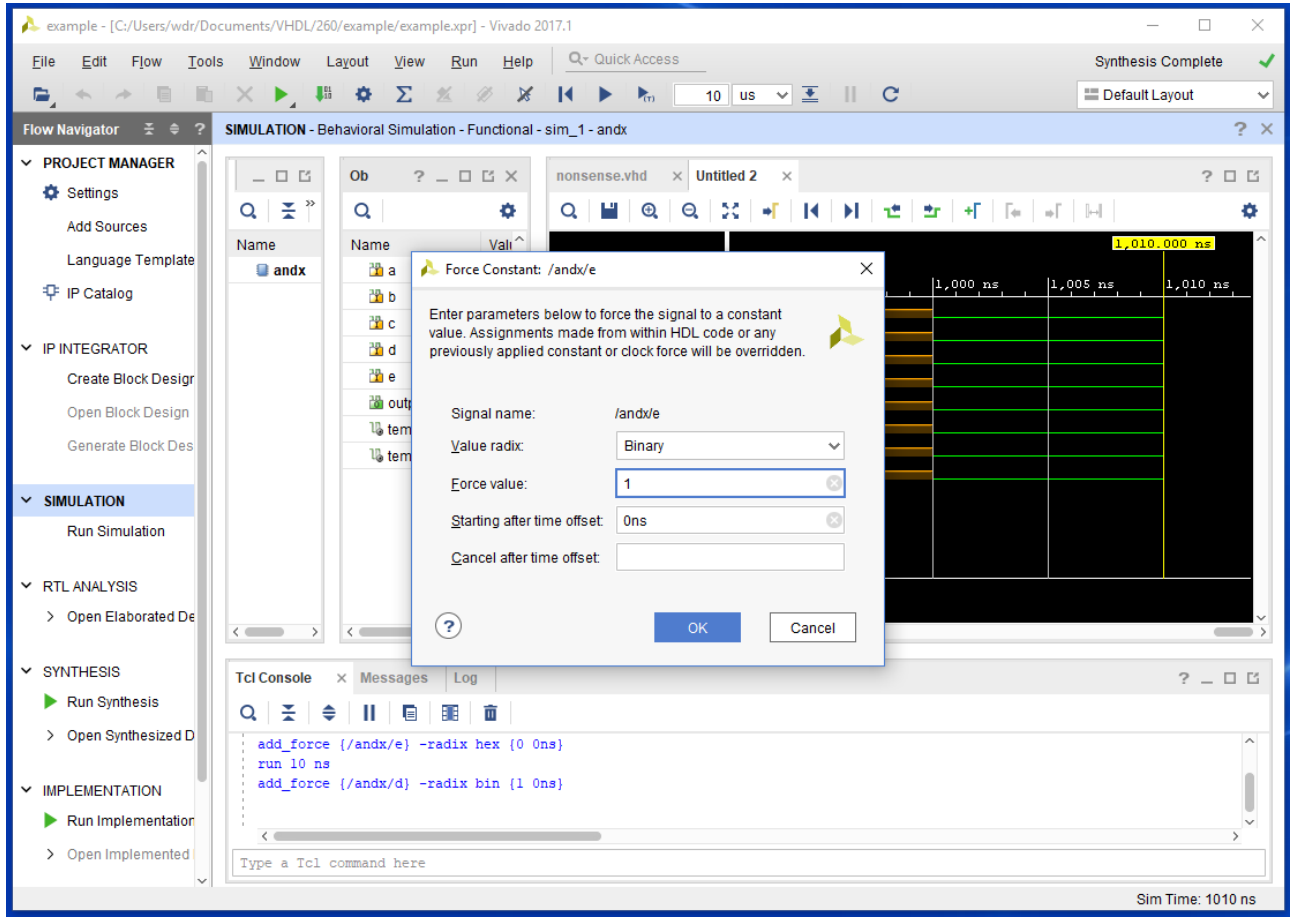
Run the simulator for 10 ns by typing “Run 10 ns” in the TCL Console



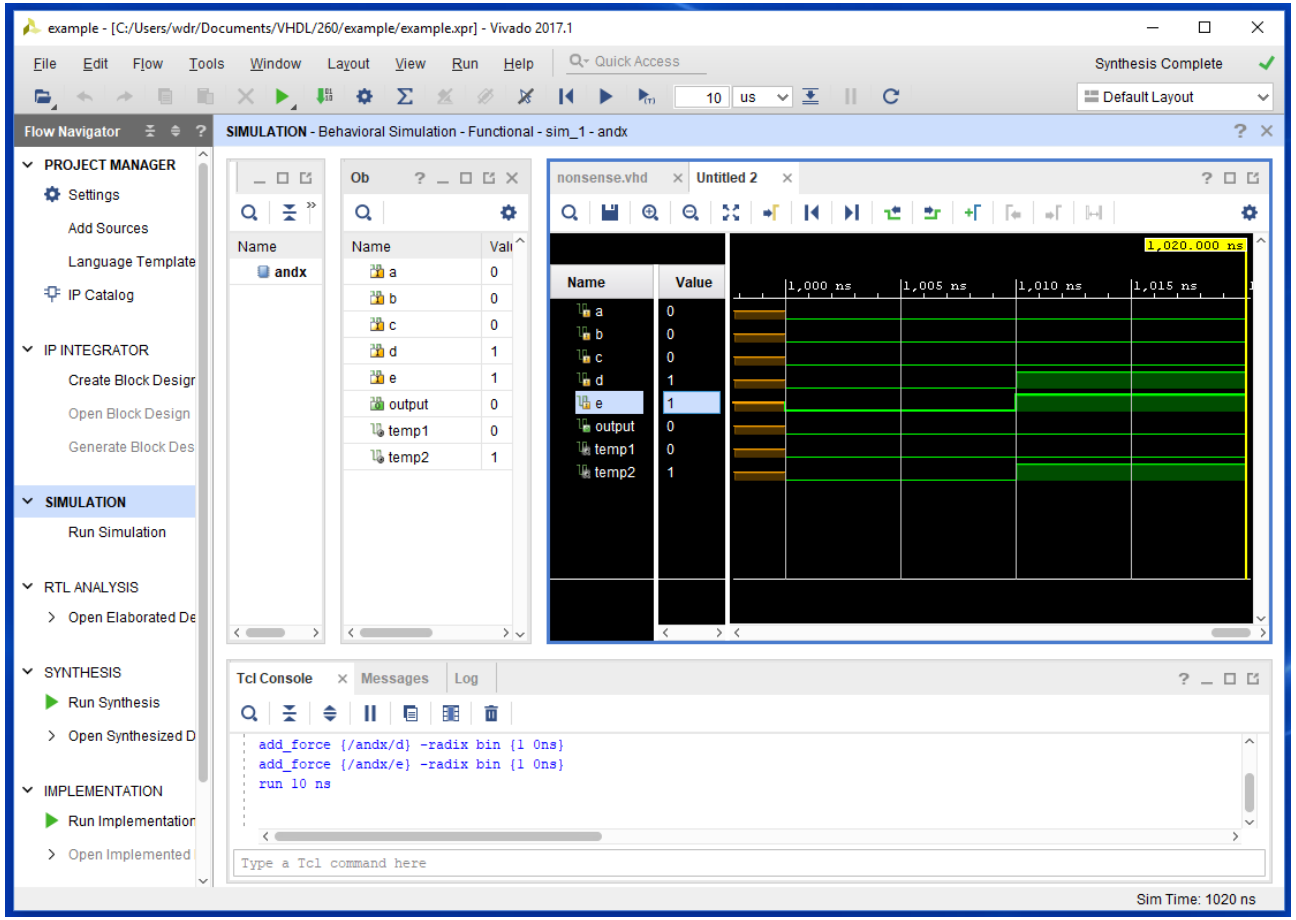
Use the zoom “magnifying glass” controls to adjust the simulation display



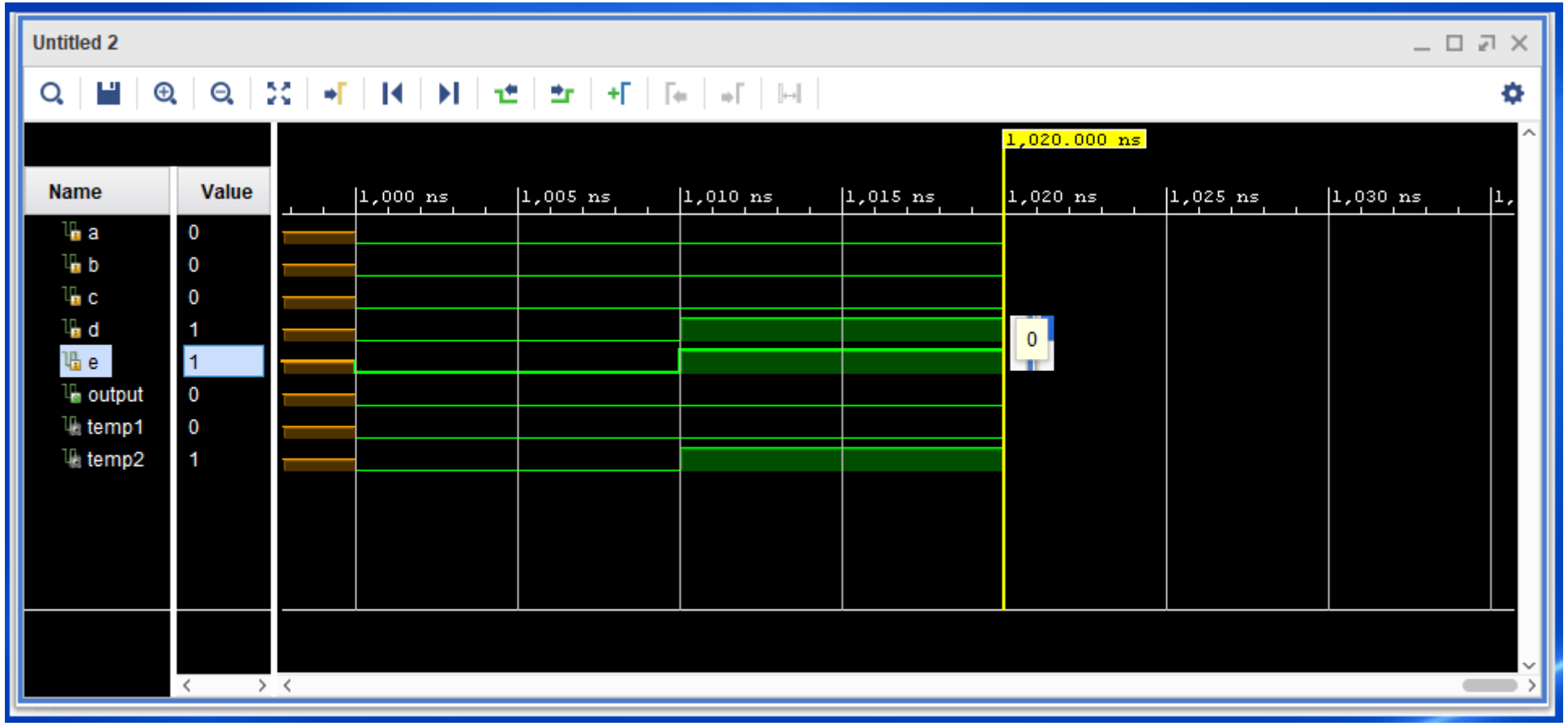
Force additional stimulus values by right clicking on inputs in the “Objects” menu



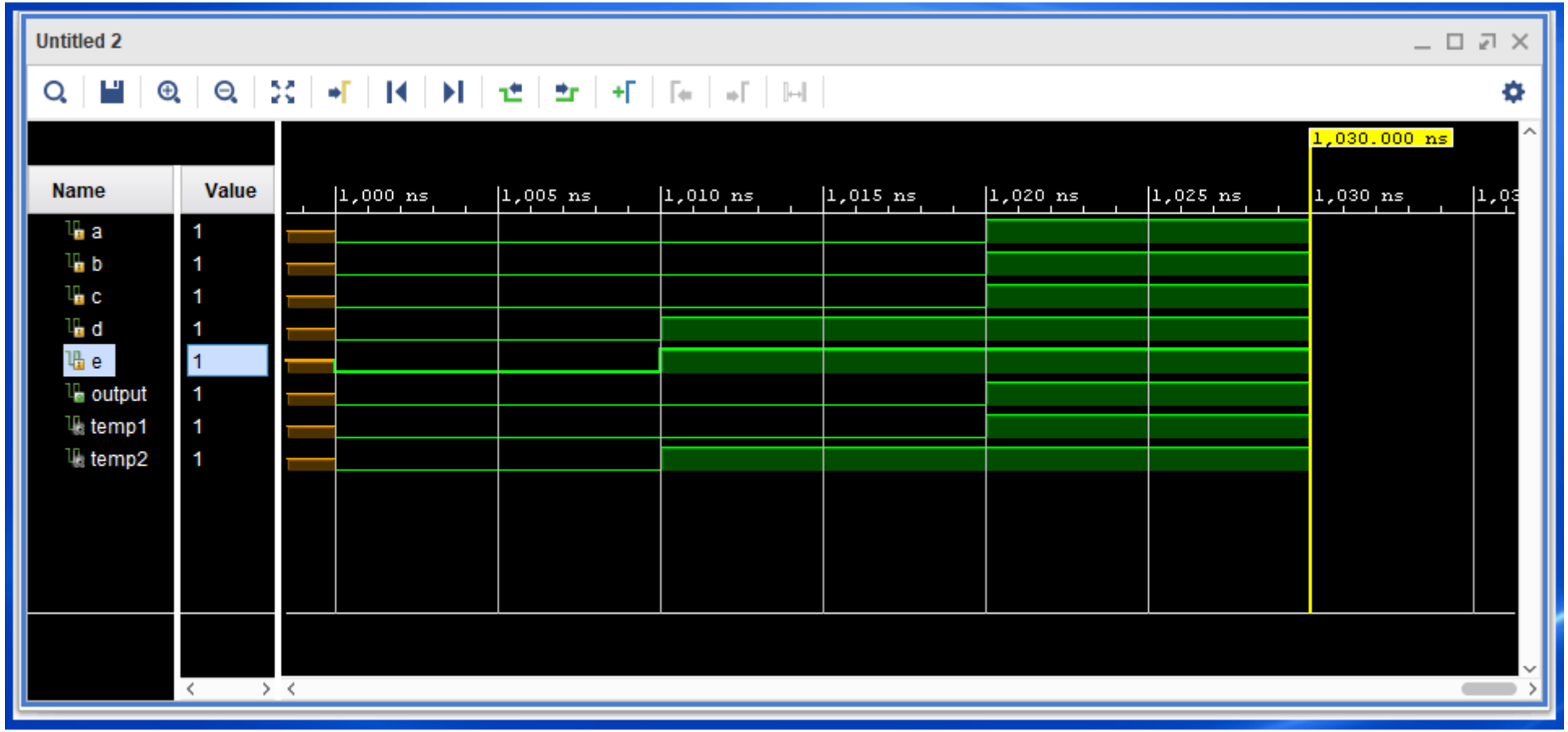
Run the simulator for an additional 10 ns after changing stimulus values using the TCL Console



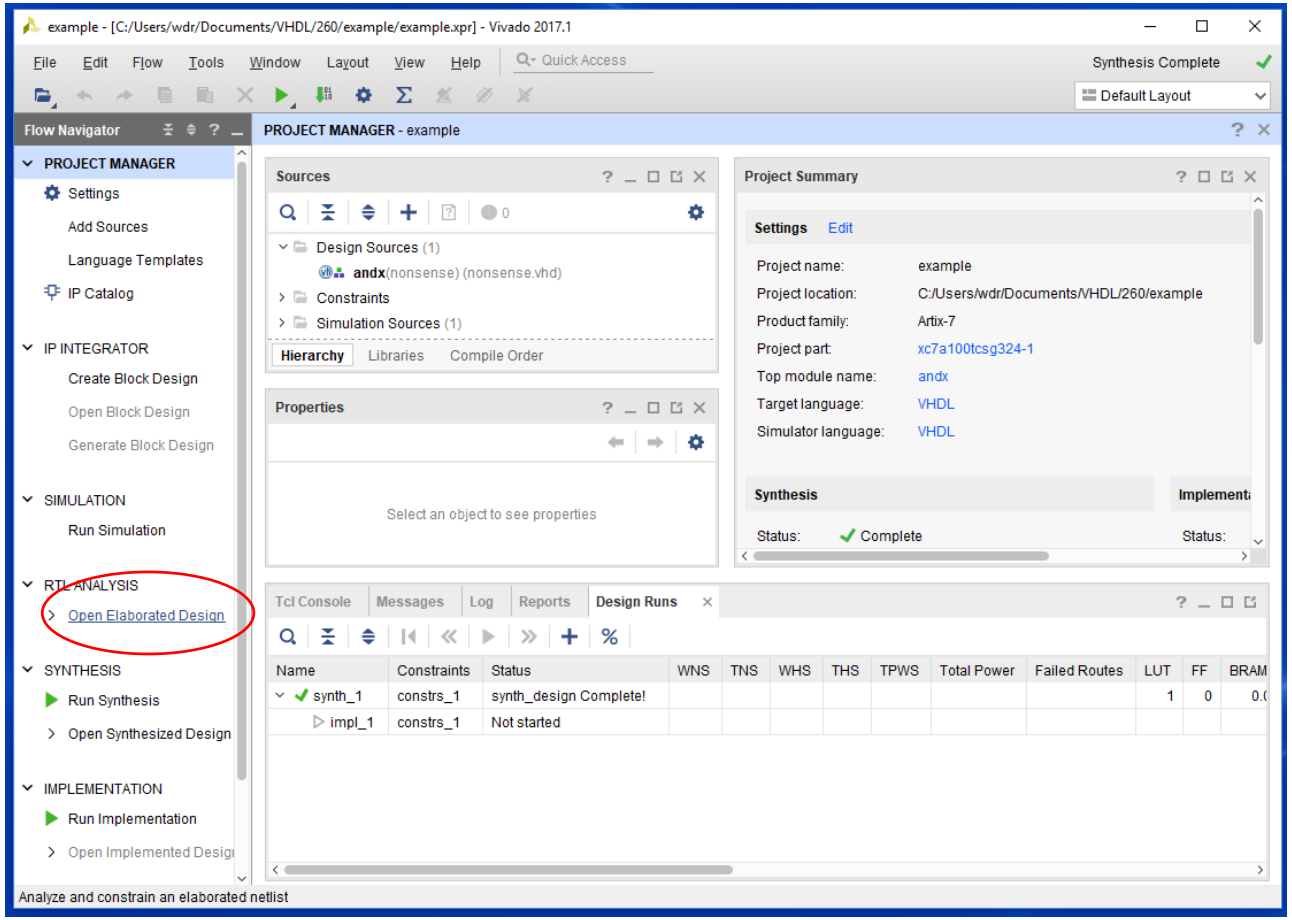
You can unlock the simulation window from the Vivado GUI



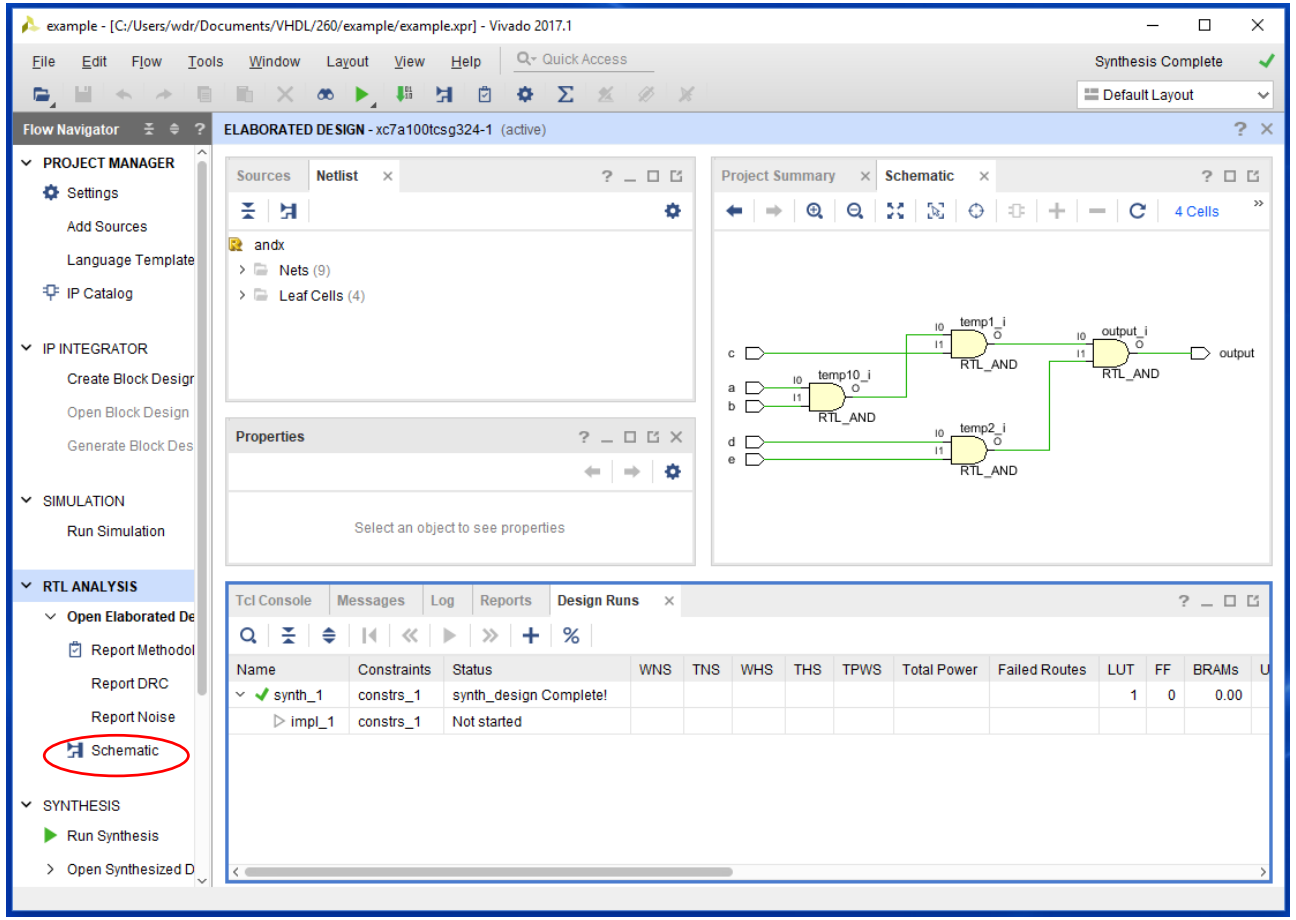
If you force all inputs to ‘1’, the output will go high after you run an additional 10 ns!



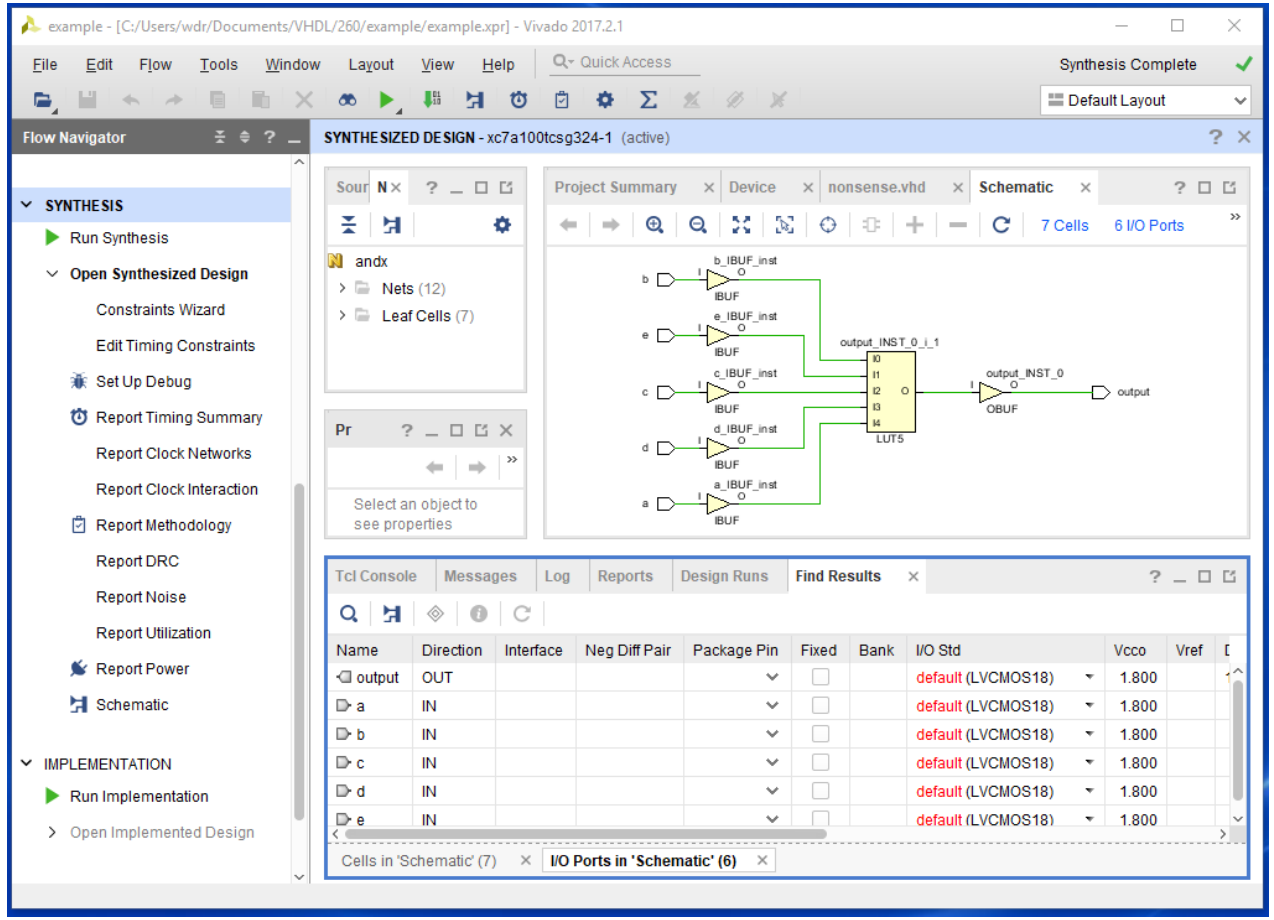
Open the Elaborated Design produced by the Synthesizer to see what your VHDL implied!



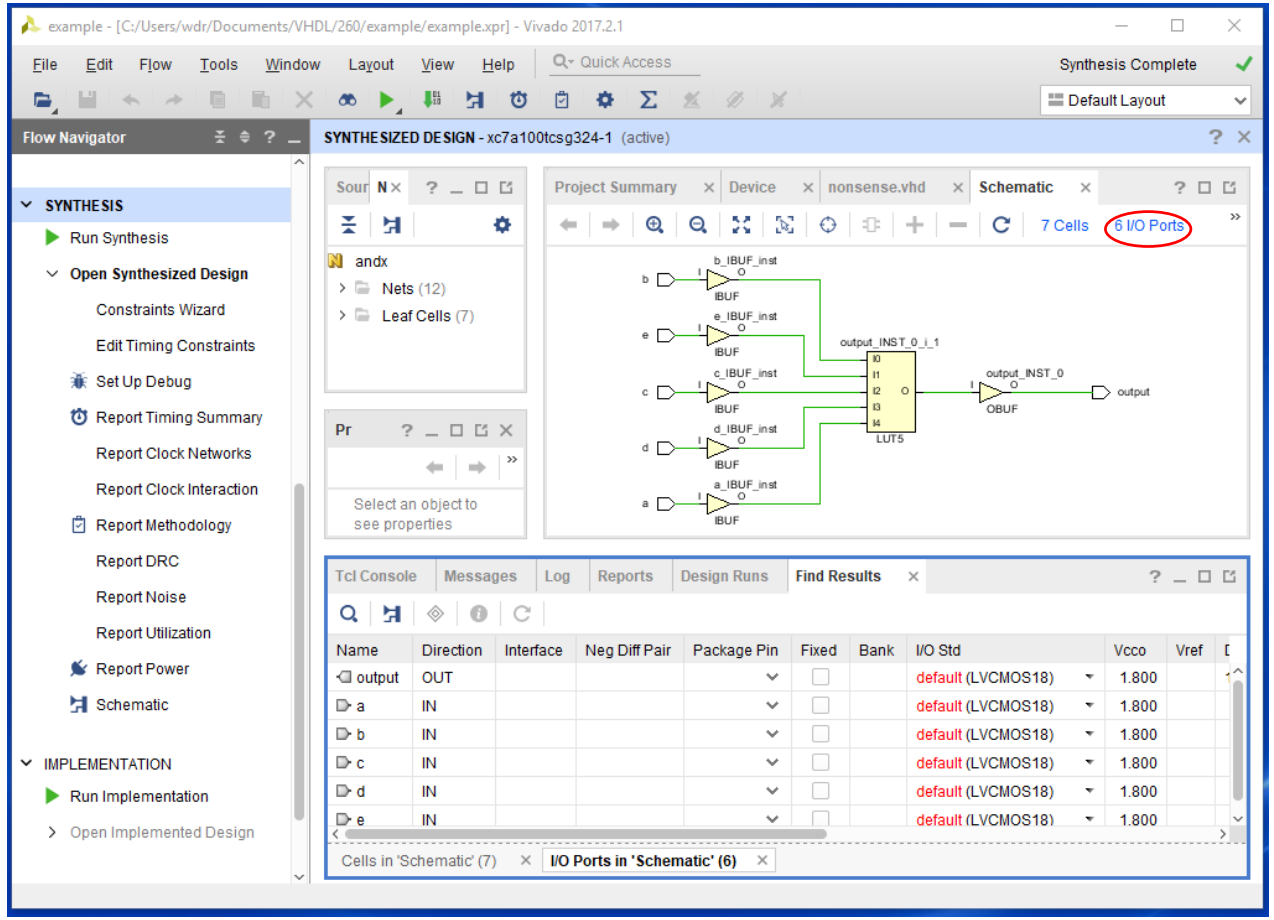
Notice that the schematic is not “optimal,” but it is logically what your VHDL implied



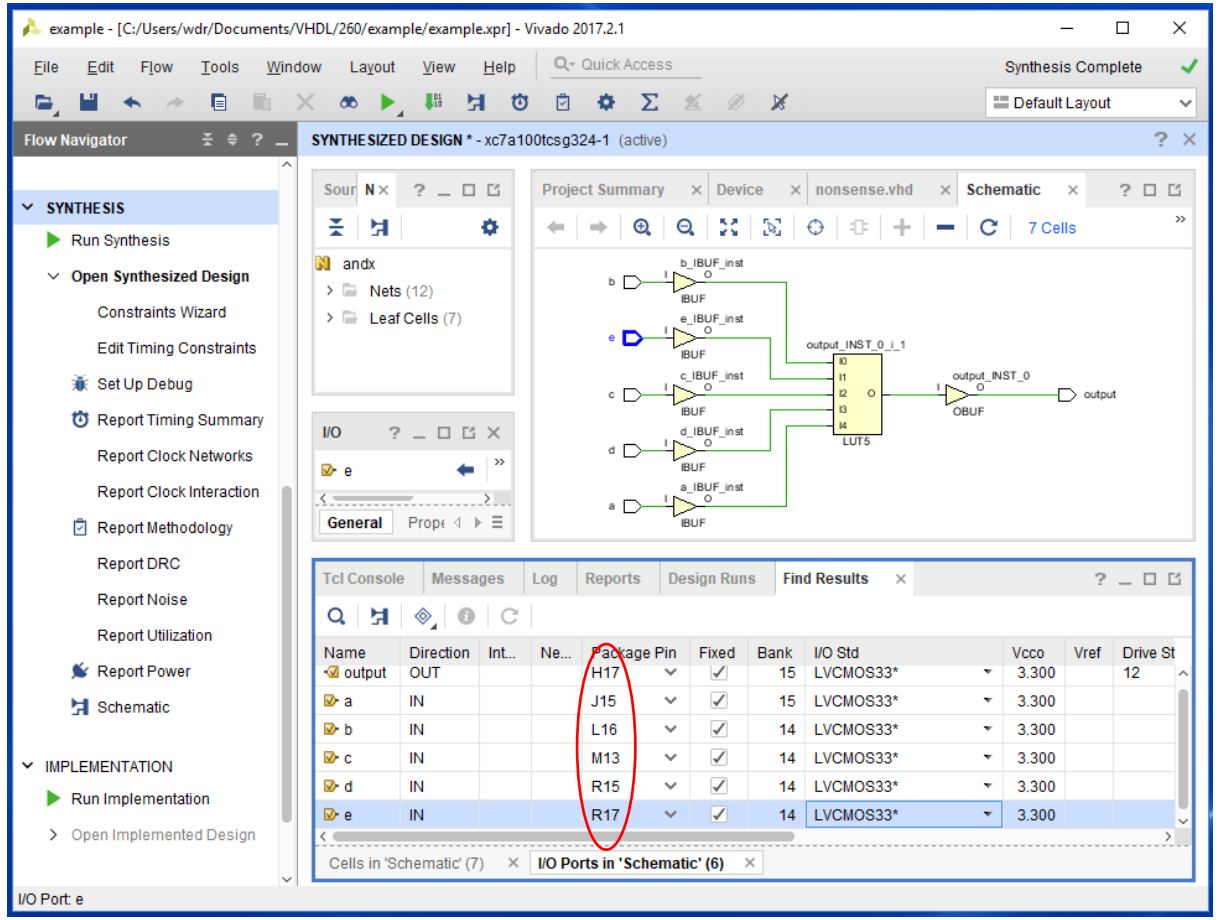
Open the Synthesized Design and view the schematic: A single LUT!



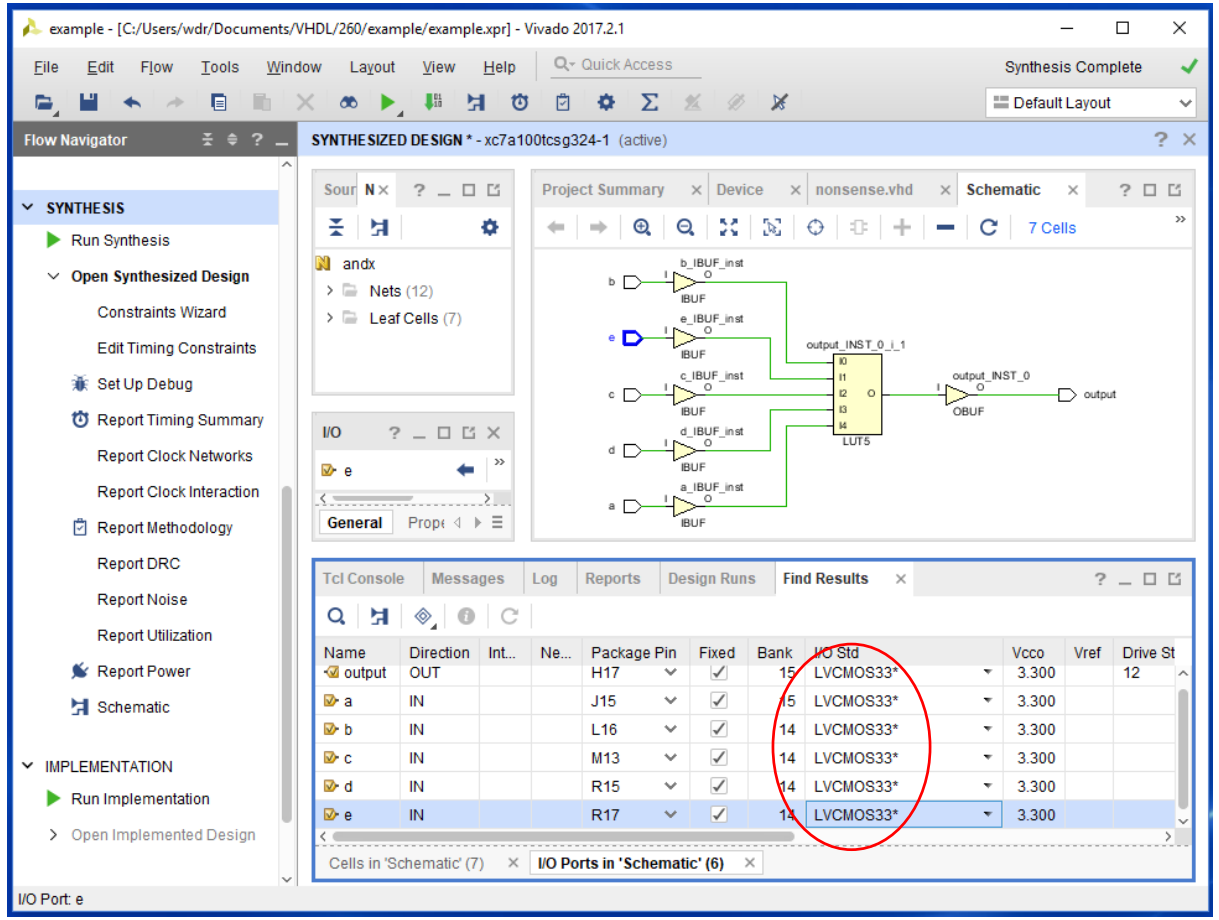
Expand the Schematic so you can see the “6 I/O Ports” option; select it to view the pins



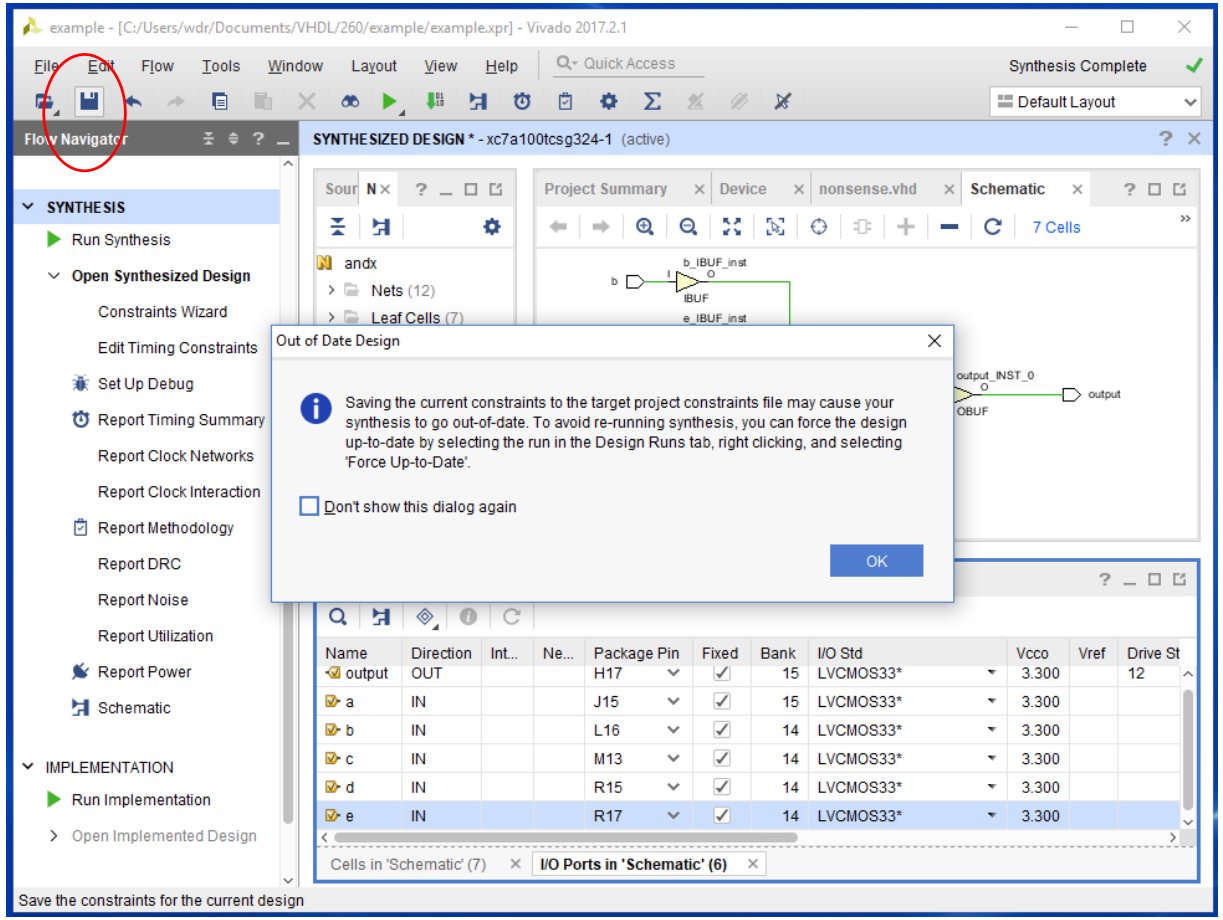
Assign the pins to SW(4:0) and LD(0) using the documentation for the demo board



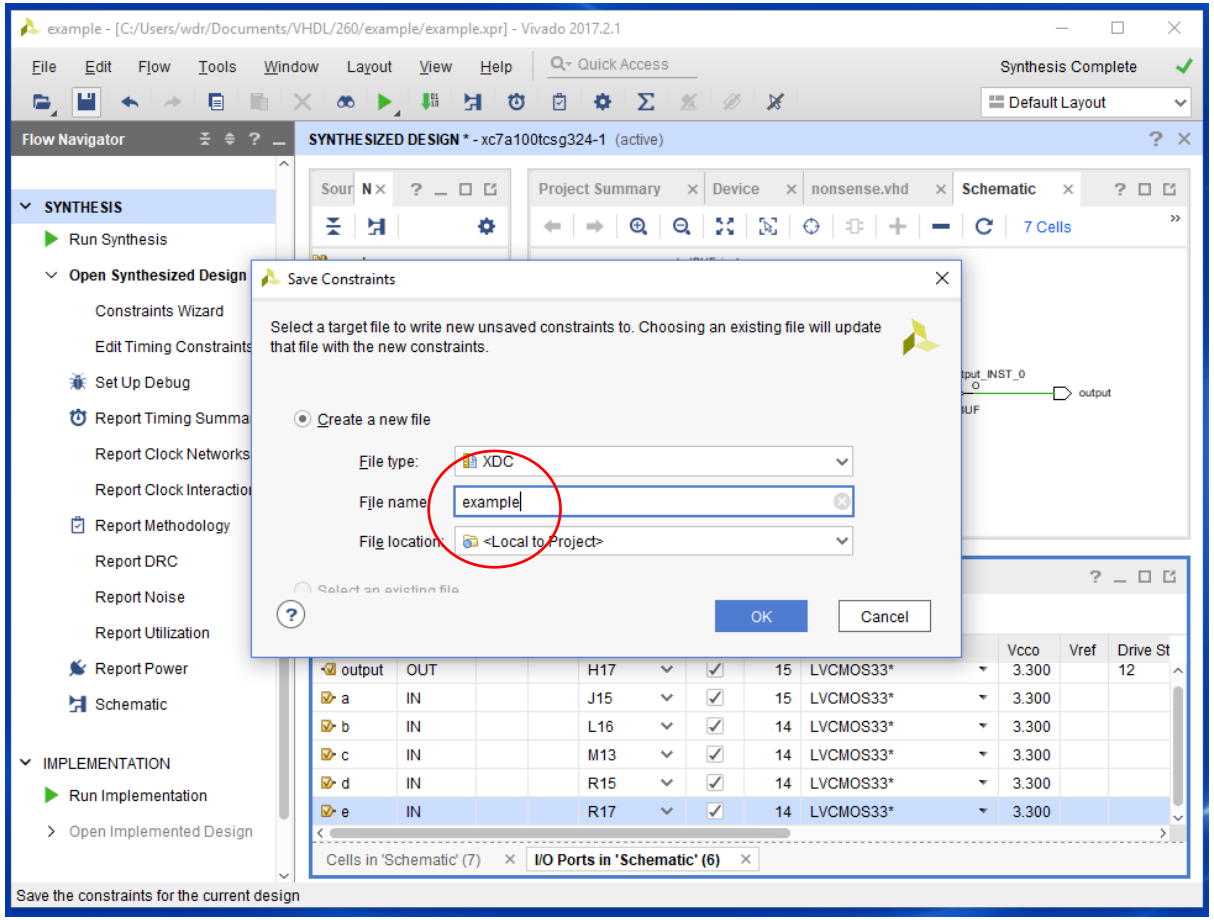
Make sure you use LVCMOS33 as discussed in class as the I/O standard!



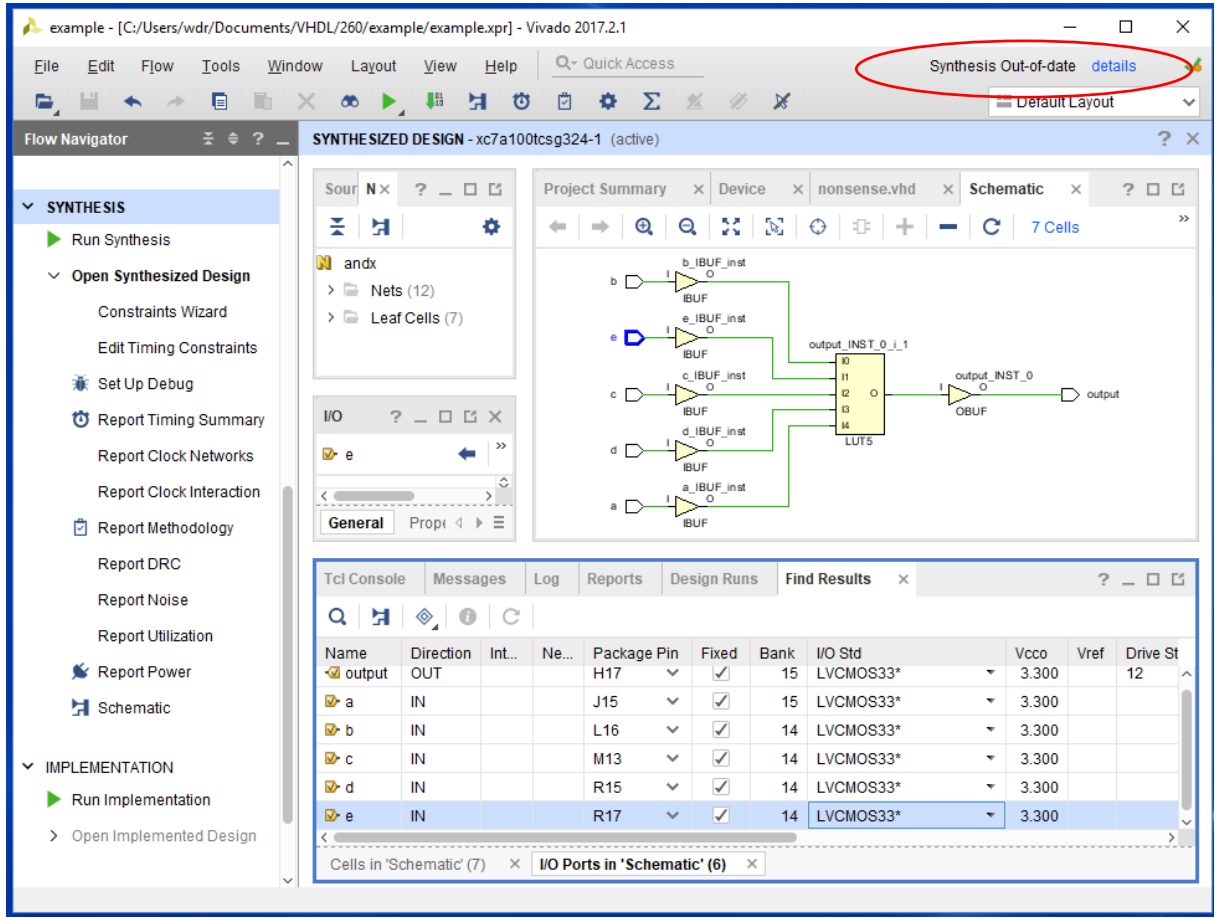
When you save the design, you will be prompted for a constraints file name



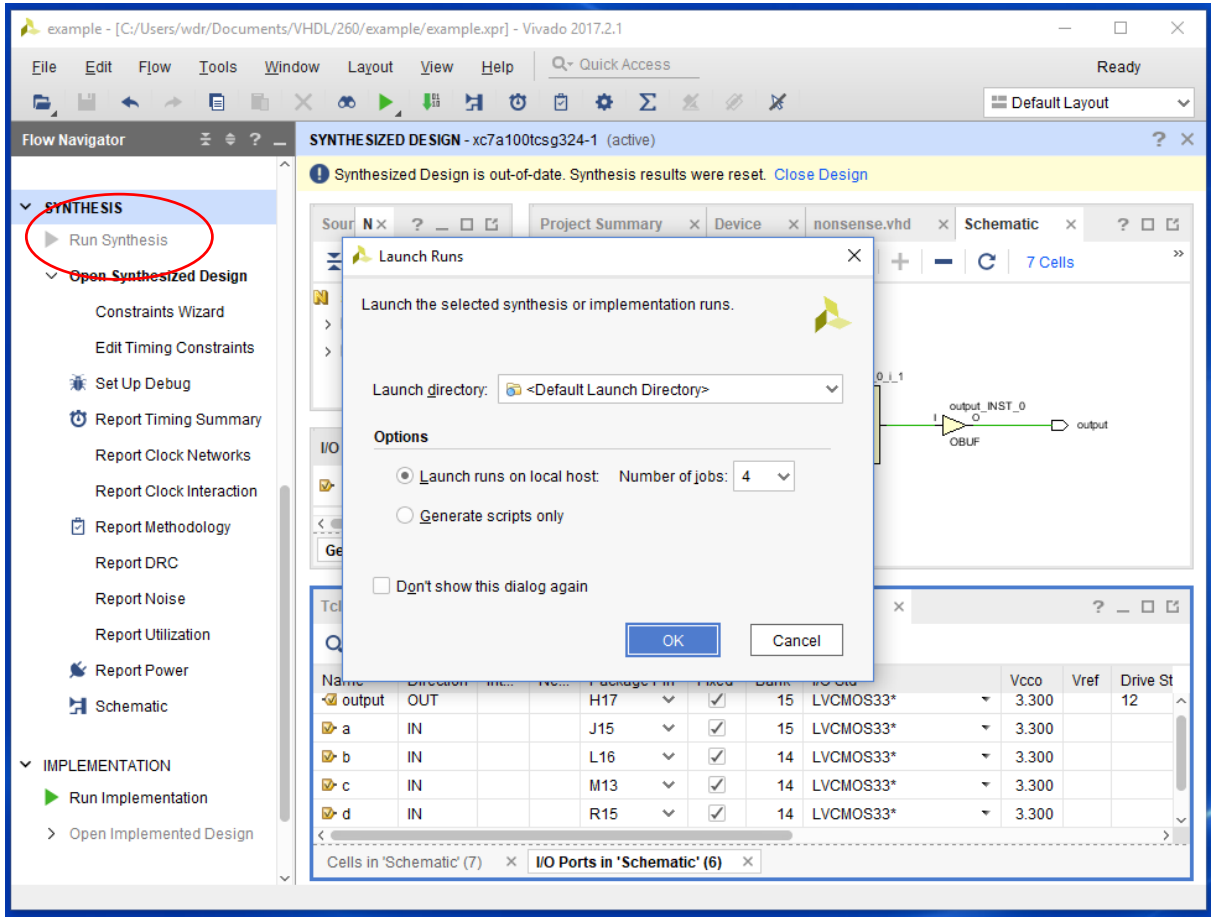
When you save the design, you will be prompted for a constraints file name



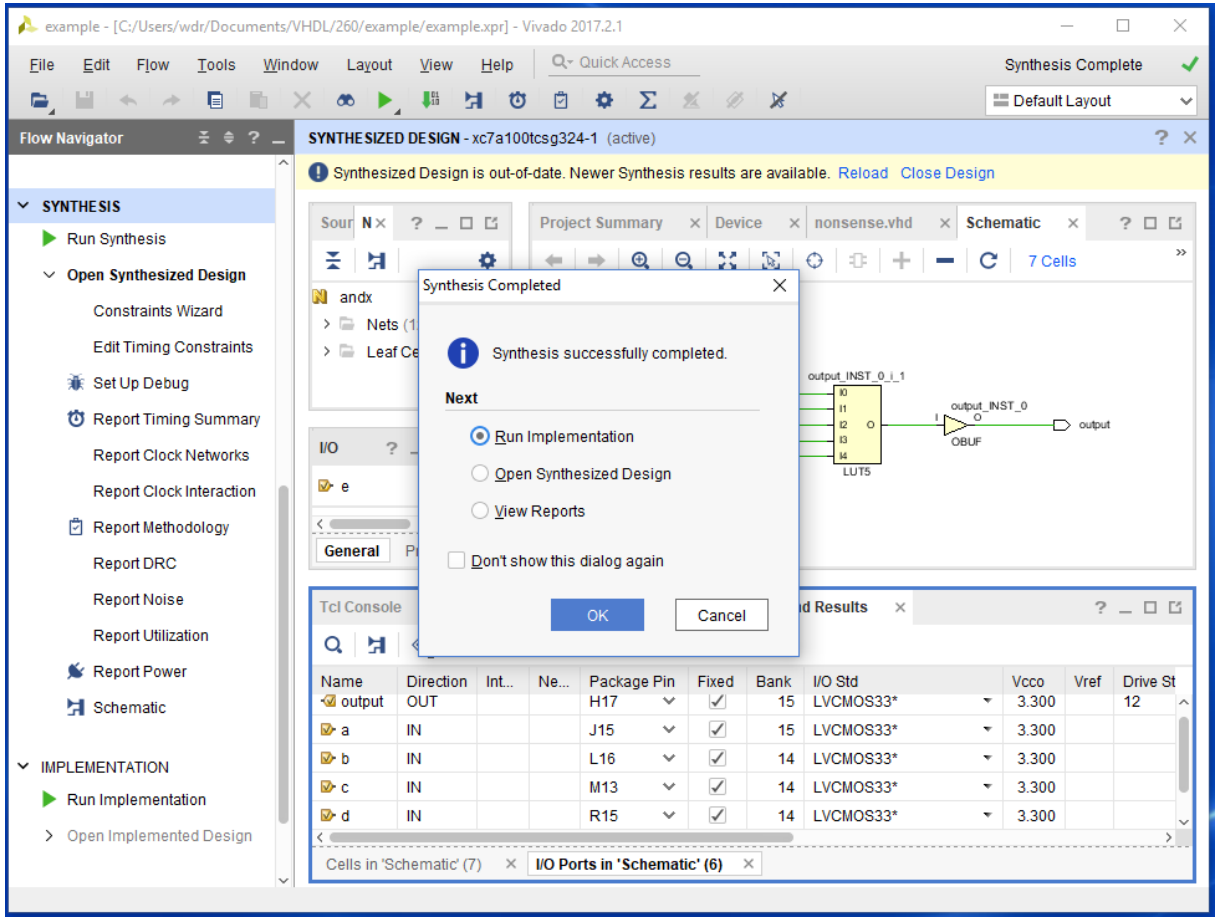
The synthesis will now be out of date because of your pin assignments and I/O standard selection



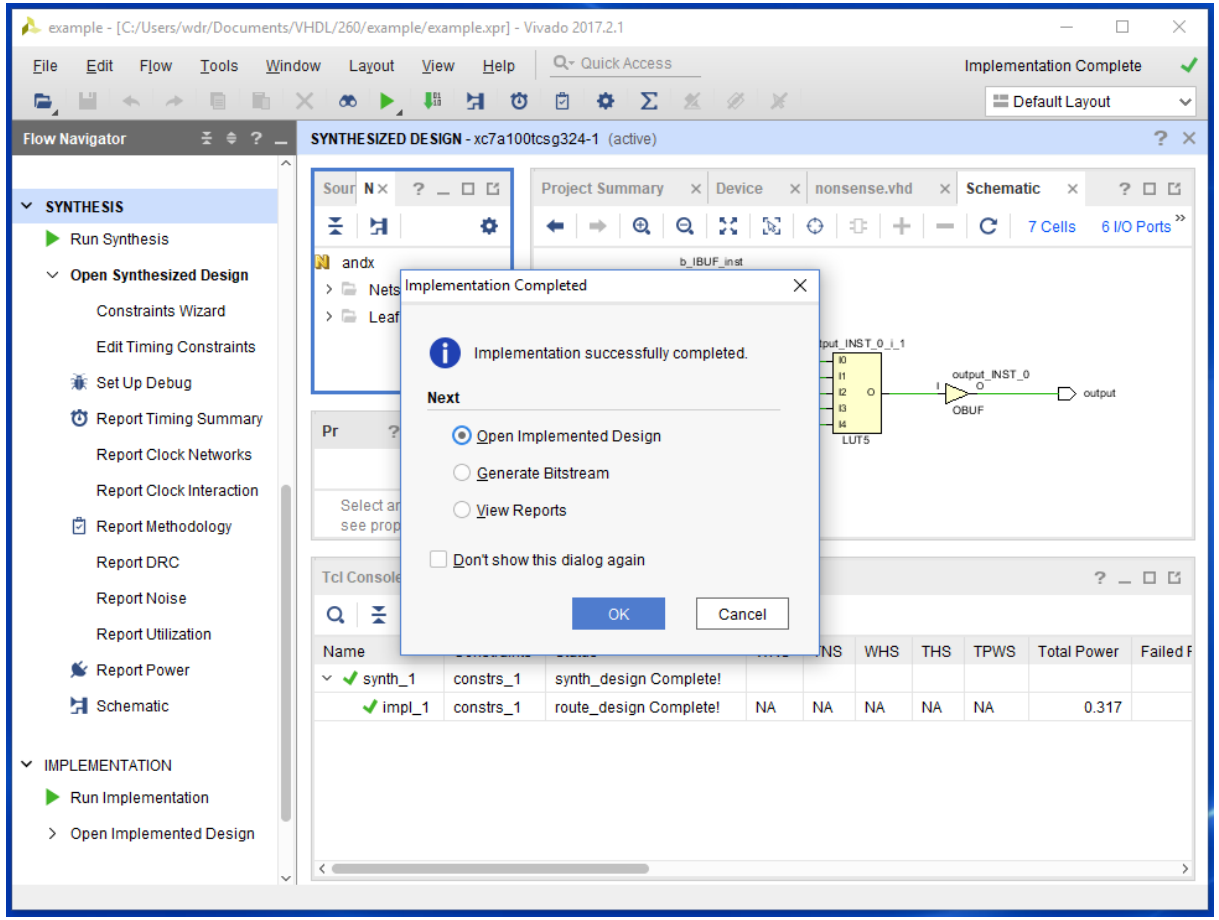
Run synthesis again…



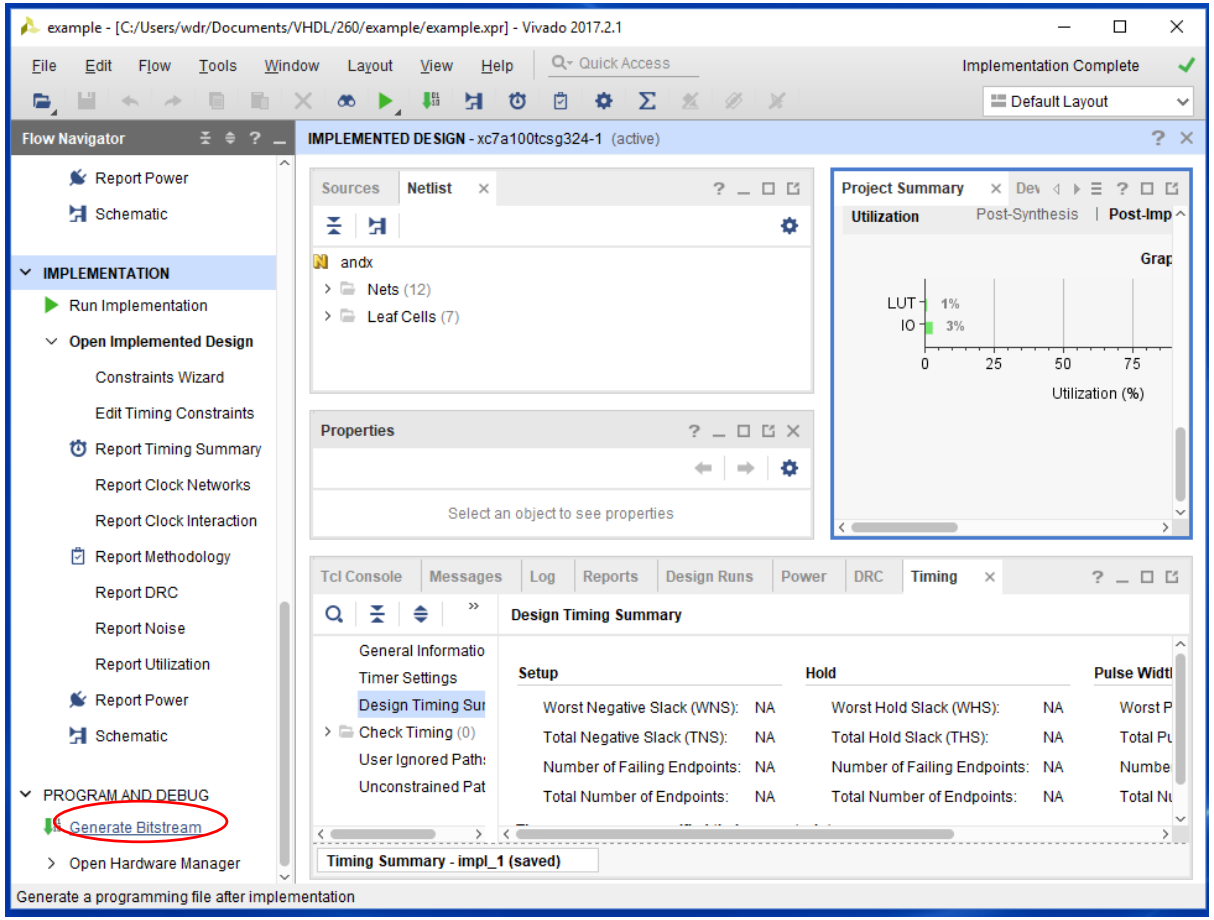
This time, run select “Run Implemenation” by clicking “OK”



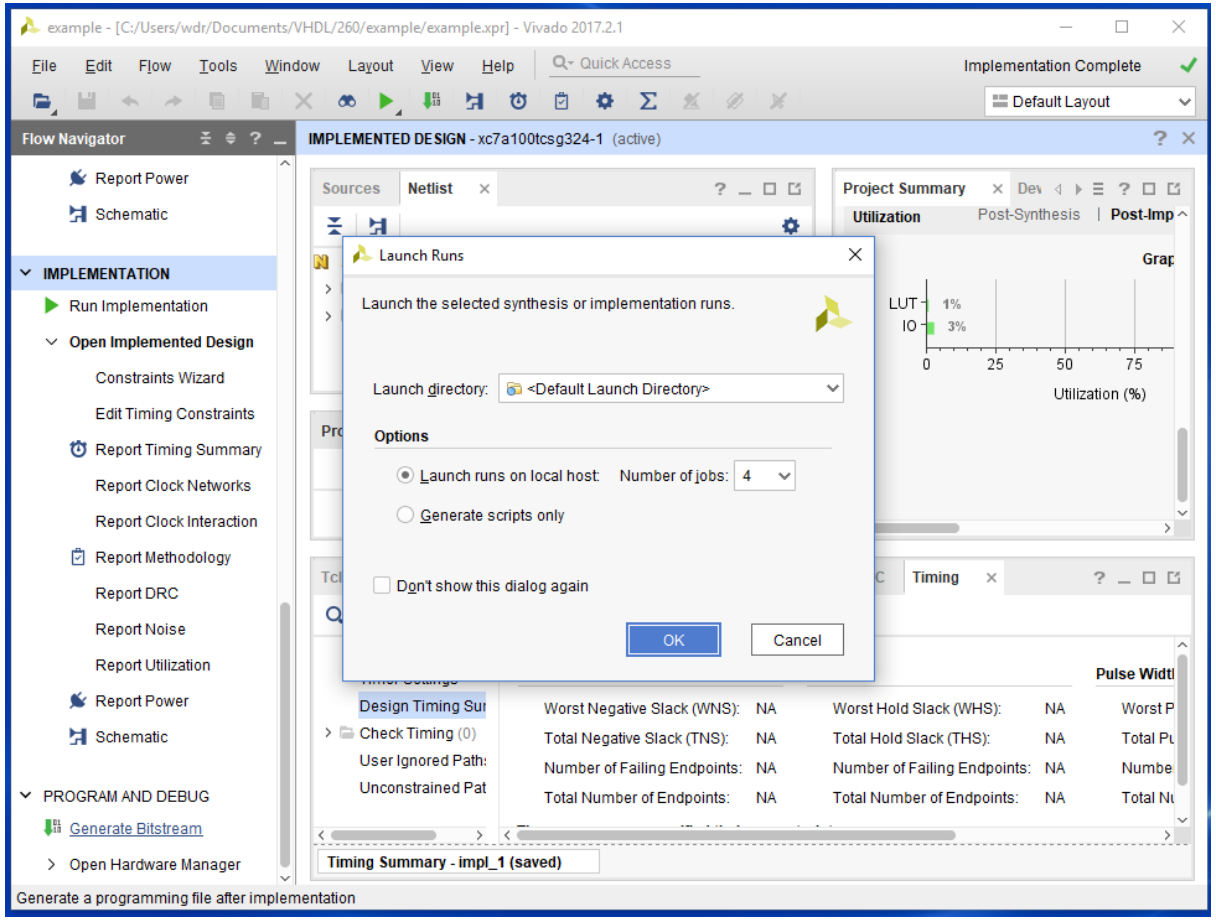
Select “Open Implemented Design” once place and route finishes



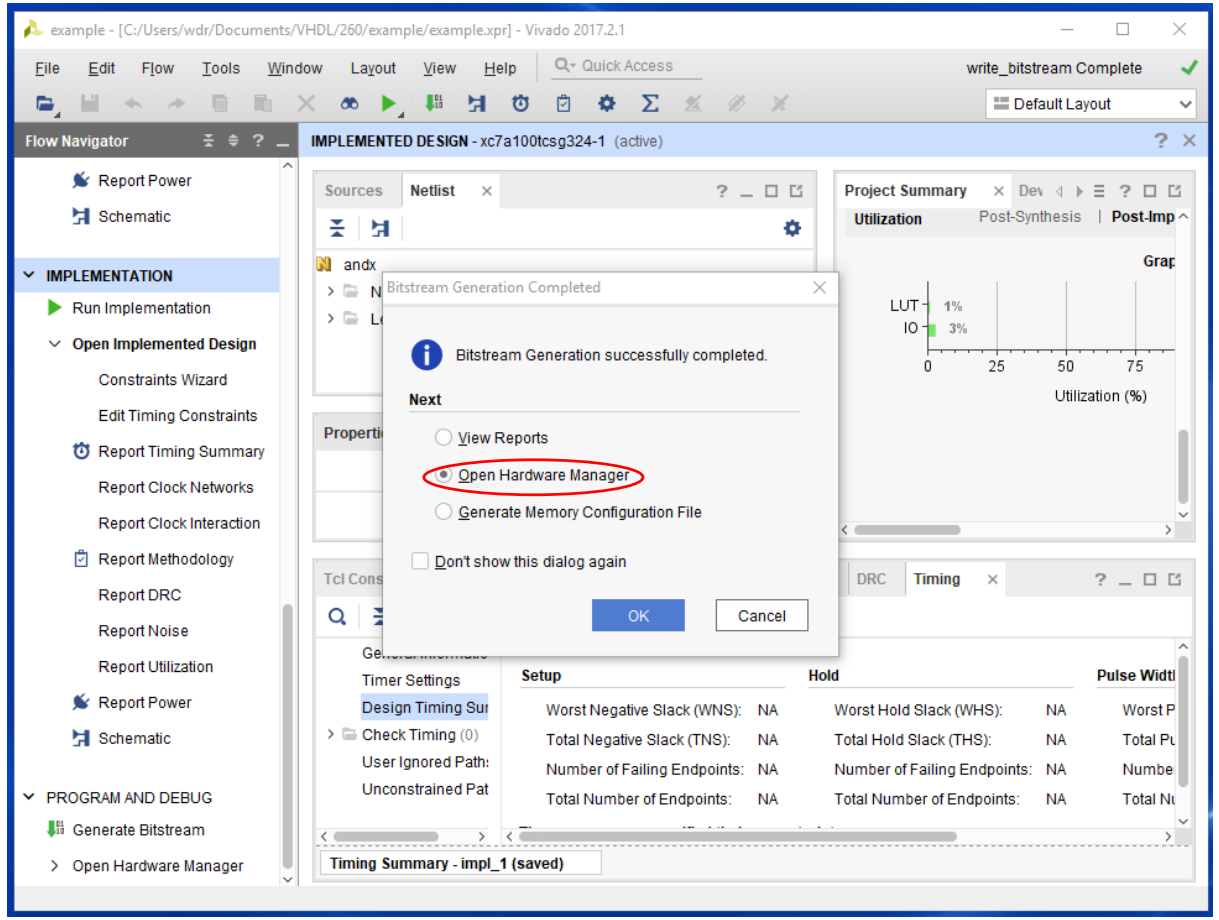
After looking at Reports, select "Generate Bitstream"



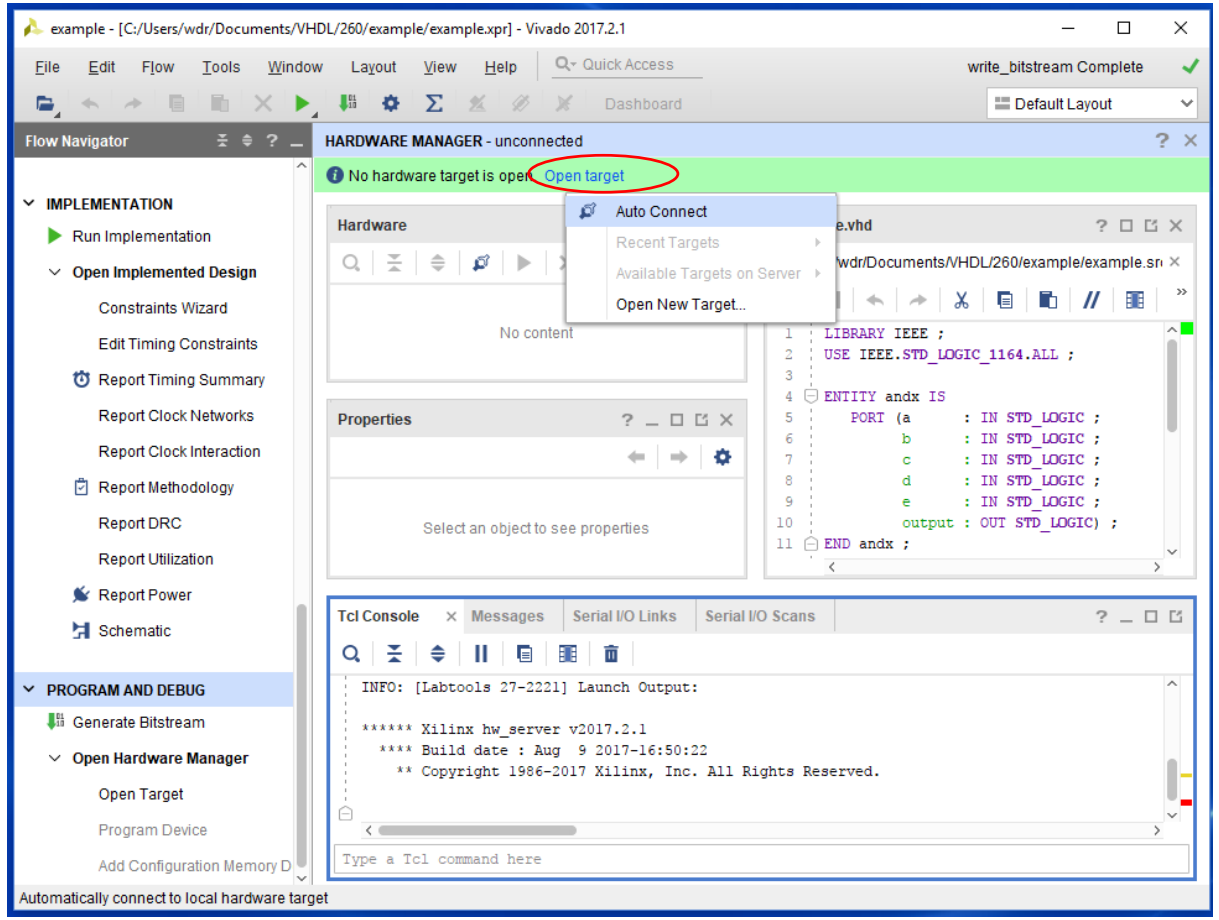
Clock “OK” at the info screen…



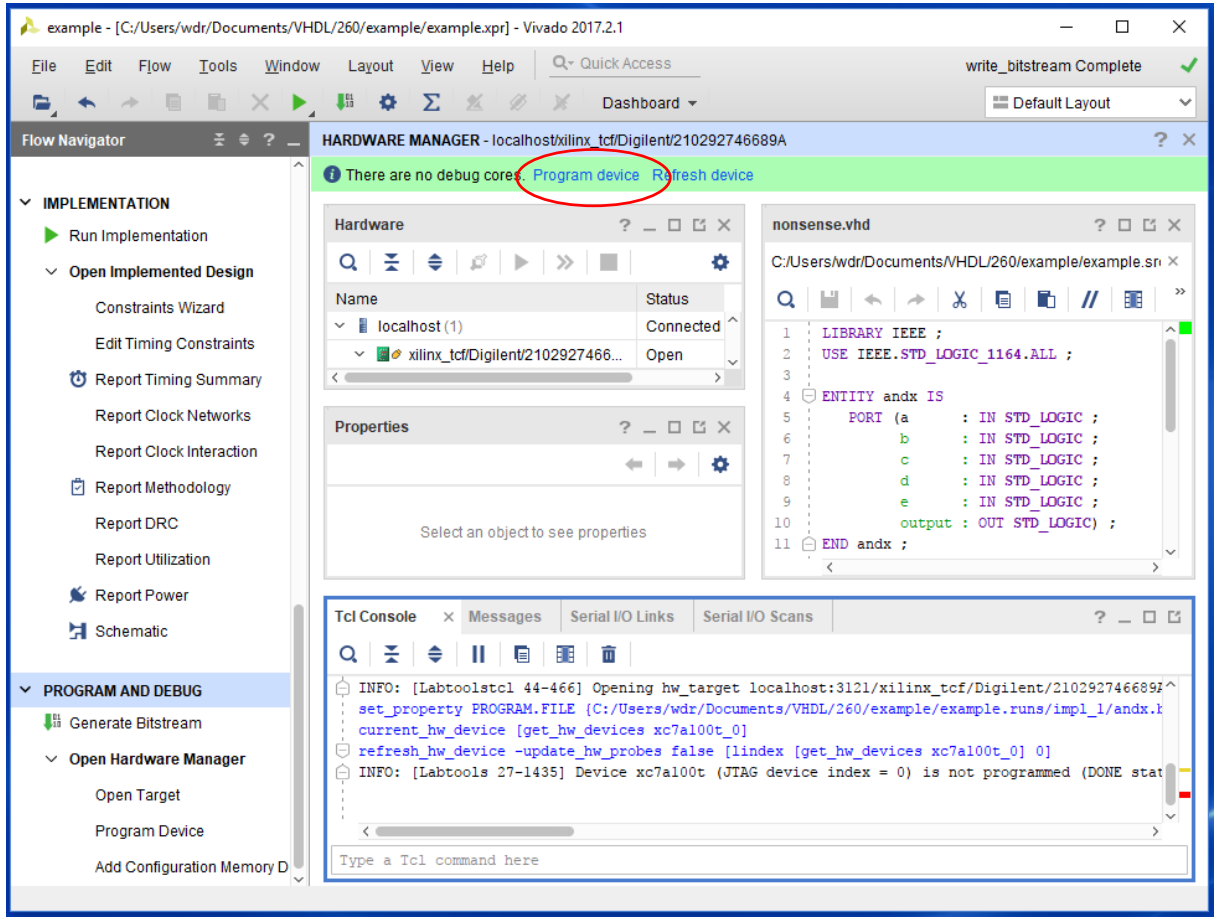
When Generate Bitstream finishes, select “Open Hardware Manager”



After plugging in the Digilent FPGA board to your laptop or PC, select “Open Target”



Select “Program device” after you see the Hardware Manager connect to the FPGA



Once the FPGA is programmed, you can test your design using the switches and LEDs!