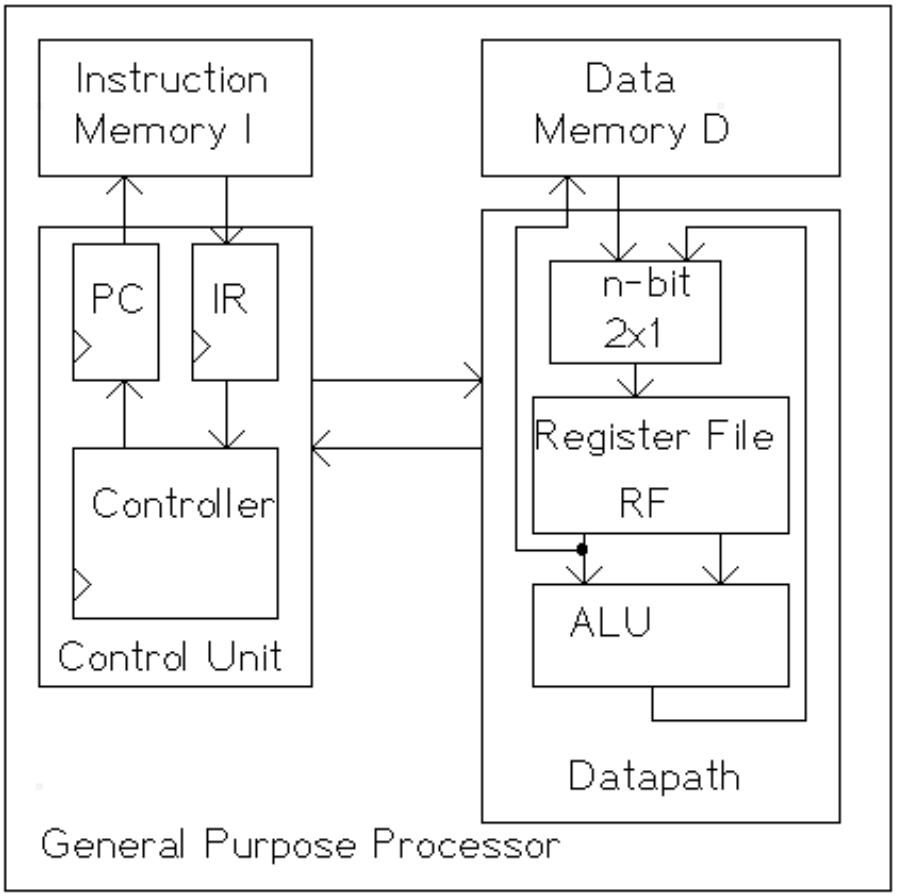
Chapter 8

Programmable Processors Chapter 8

Programmable Processors

- GPP has:
  - Datapath
    - Register File
    - ALU
  - Control Unit
    - Program Counter – PC
    - Instruction Register – IR
  - Instruction Memory
  - Data Memory



Control Unit

- Interprets Instruction in IR
- Instructions for this machine are all the same size in bits.
- An instruction specifies an operation, and maybe operands, and result.
- Operands and result are from/too the RF.
- Operations includes load/store.

Control Unit

- Fetch/Execute cycle
  - Fetch instruction from I memory
  - Decode instruction
  - Execute instruction
- Cycle may take multiple clock cycles
- PC starts at a known address (0 for this machine)
- PC increments to next instruction (usually)

Instruction Set

- Instruction is 16-bits
- Opcode is IR<15..12>
- Load and Store register address is IR<11..8>
- D Memory Address is IR<7..0>
- Operand 1 register address is IR<7..4>
- Operand 2 register address is IR<3..0>

Instruction Set

- Machine Code and Mnemonics
- MOV destination, source
  - One address is a register address the other is a D memory address.
  - Load and store use the MOV mnemonic
  - Register address always starts with “R”.
- ADD result, operand1, operand2