# Chapter 3

Sequential Logic
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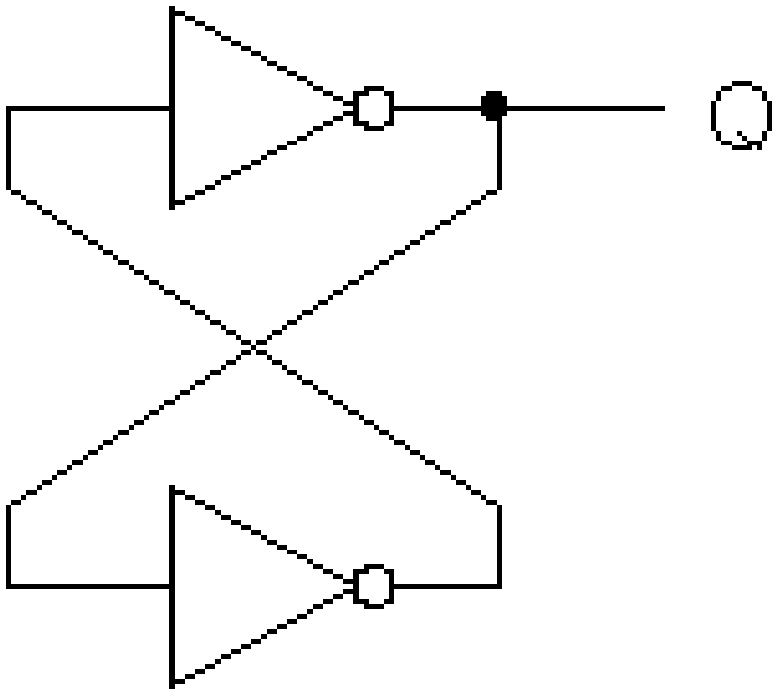
# Sequential Logic

- Combinational logic – The output signals are determined by the current state of the input signals.
- Sequential logic – The output signals are determined by the current state of the input signals and the history of the circuit.  A sequential circuit has memory.

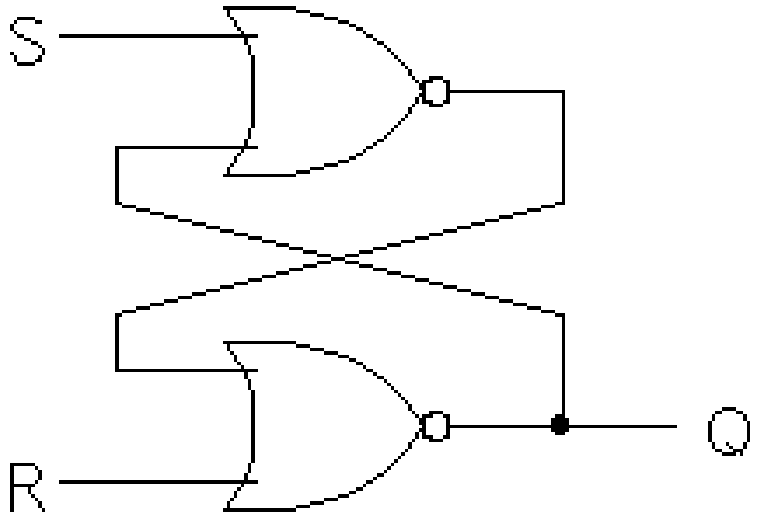
# Sequential Logic

- Consider the following circuit:



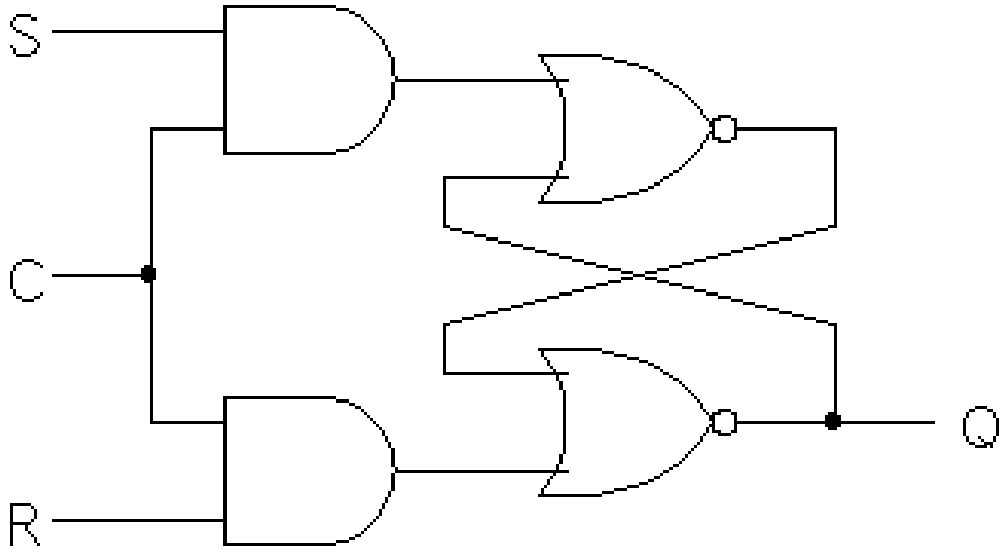
# Basic SR Latch

- Replace the inverters from the previous slide with NOR gates.
- Write a truth table for the circuit.



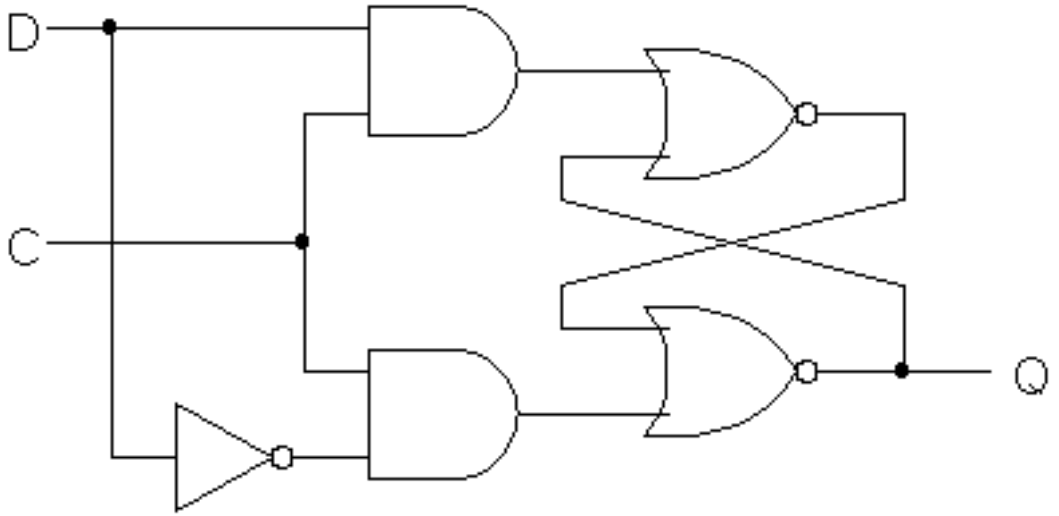
# Level-Sensitive SR Latch

- Add an extra level of AND gates to provide a control signal.
- The control signal allows the S and R inputs to change without changing the outputs.



# D-type Latch

- The output follows the D input while the control signal is high.  The latch freezes the output when the control signal goes low.



# Edge-Triggered D-type Flip-Flop

- Uses a master-slave set of D latches.
- The output changes to the value of the D input only when the Clk input changes from a low to high.
- This is the building block for most digital systems.

# Register

- A set of D-type Flip-Flops using a common clock.
- The number of Flip-Flops is the number of bits in the word.
- Used to create a pipeline of operations.

# Finite State Machine FSM

- A general FSM has:
  - Inputs
  - Outputs
  - Flip-Flops holding the current state
  - Combinational logic to create the next state
  - Combinational logic for the output

# FSM Design

- From a written description draw a state diagram.
- Create the state table (truth table)
- Determine the flip-flop inputs for the next state and output.
- Optimize the combinational logic
- Draw the circuit

# FSM Design

- Two FSM models
- Mealy model – The outputs change as the input changes.
- Moore model – The outputs change only on clock edges.
- A more general model could be both.

# Mealy Model

- Design a Mealy Model FSM that detects the bit pattern 1010111 (least significant bit first) in a serial bit stream.  The bit pattern may appear anywhere in the stream (it can overlap).

# Moore Model

- Design a Moore Model FSM that detects the bit pattern 1010111 (least significant bit first) in a serial bit stream.  The bit pattern may appear anywhere in the stream (it can overlap).