CIRCUITS LABORATORY

EXPERIMENT 10

DIGITAL LOGIC CIRCUITS

10.1 ABSTRACT

The purpose of this experiment is to understand and measure the electrical properties of TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal Oxide Semiconductor) logic circuits and compare your results to the manufacturers' specifications. Your objectives are to: measure the Voltage Transfer Characteristics (VTC) of an inverter from each of the logic families; determine the power dissipation for each inverter type as a function of operating frequency; construct a ring oscillator with each inverter type to determine the typical propagation delay; and understand how to read and interpret manufacturers' data sheets in order to compare your results to the logic circuits' specifications.

10.2 INTRODUCTION

Over the last twenty years, logic designers have seen the number of devices per integrated circuit grow rapidly. While the number of devices and functions per chip has increased dramatically, the input and output characteristics of the various logic families have remained fairly constant reflecting the properties of the transistor types employed. Folklore has it that TTL is fast and power hungry and CMOS is slower and power efficient. In this lab you will try to independently verify or debunk the folklore.

10.3 INVERTER DESIGNS

We will first take a look at the symbolic diagram of a simple inverter in each

family. Regardless of the logic family, the logic diagram for an inverter is given by Figure 10.1 below.

Figure 10.1: Inverter logic symbol.

The labels in figure 10.1 (a) indicate that if the input signal is asserted when the voltage representing it is high, then the output signal is asserted when its voltage is low. These labels are consistent with the Mixed Logic Standard. Sometimes we see the input labeled A and the output labeled A' or A not as in Figure 10.1(b), which is known as the Positive Logic Standard. A "mixed logician" calls the 7404 and similar devices voltage inverters since they do not invert the logic of the signal passing through it, but, rather, invert the voltage which indicates the logical variable is TRUE or asserted (i.e., when the input is TRUE it has a high voltage and the output is also TRUE and has a low voltage).

10.3.1 Transistor Inverter

The basic saturating-transistor logic can be best illustrated by first considering a simple transistor-inverter stage shown in Fig10.2(a). The normal (or static condition) of the transistor is either OFF (in the cutoff region) or ON (the transistor is saturated). These two conditions can relate to the two binary states of logic 1 (or TRUE) and logic 0 (or FALSE). Of course, the transistor must pass through the active region in order to make the transition from one state to the other. The goal is to make the transition region as small as possible.

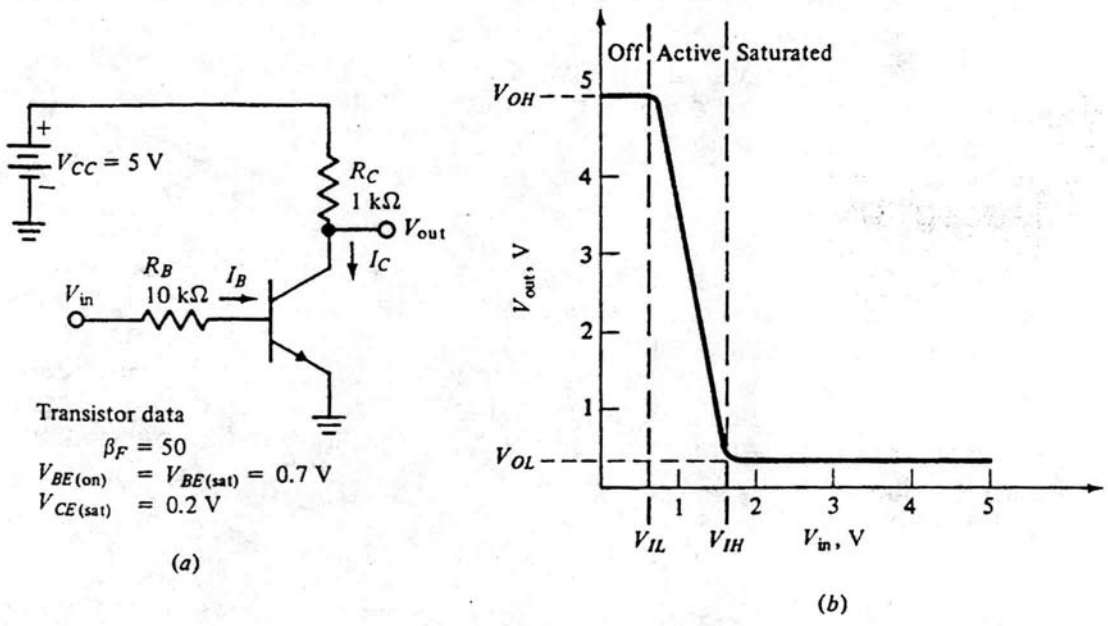

Figure 10.2: (a) Circuit diagram of a transistor inverter
(b) Voltage transfer characteristic of an unloaded inverter

In order to understand the operation of the simple transistor-inverter shown in Figure 10.2 (a), consider the voltage transfer characteristics shown in Fig. 10.2(b). Notice that the transistor is OFF when V_{in} is less than $V_{BE(ON)}$ = 0.7 V and the output voltage $V_{OUT} = V_{CE} = V_{CC}$ = 5 V. As V_{in} increases, the transistor turns on and enters the active region and it follows that:

$$V_{OUT} = V_{CE} = V_{CC} - I_C R_C \qquad (10.1)$$

$$I_C = \beta_{DC} I_B \qquad (10.2)$$

$$I_B = \frac{V_{in} - V_{BE(ON)}}{R_B} . \qquad (10.3)$$

As V_{in} continues to increase, the transistor will saturate. In this case,

$$I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} \qquad (10.4)$$

$$V_{OUT} = V_{CE(SAT)} . \qquad (10.5)$$

The breakpoints of the voltage transfer characteristic indicate where the transistor's operating region changes from cutoff to active and from active to saturated.

At the input, the threshold voltage for the LOW level is called V_{IL} and represents the Edge of Cutoff (EOC), which is the breakpoint where the transistor moves from the cutoff to the active region. The threshold voltage for the HIGH level is called V_{IH} and represents the Edge of Saturation (EOS), which is the breakpoint where the transistor moves from the active to the saturated region. For the output, the threshold voltages are represented by V_{OL} and V_{OH}, respectively. These voltage levels are shown graphically in Figure 10.3 for the circuit of Figure 10.2 (a).

This can be summarized for the transistor-inverter as follows:

$$V_{IL} = V_{IN,LOW} = V_{IN(EOC)} \tag{10.6}$$

$$V_{IH} = V_{IN,HIGH} = V_{IN(EOS)} \tag{10.7}$$

$$V_{OL} = V_{OUT,LOW} = V_{CE(SAT)} \tag{10.8}$$

$$V_{OH} = V_{OUT,HIGH} = V_{CC} \tag{10.9}$$

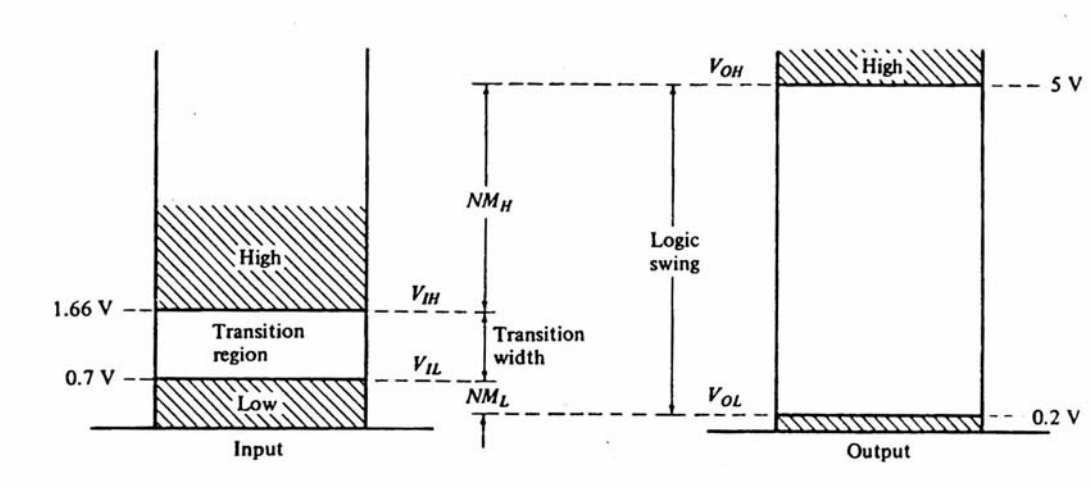

Figure 10.3: Logic-level diagram.

Considering the circuit shown in Figure 10.2(a), when V_{IN} is less than $V_{BE(ON)} = 0.7$ V, it is recognized as a LOW-input level. Thus, $V_{IL} = V_{IN(EOC)} = V_{BE(ON)} = 0.7$ V. The HIGH-input level is the value of V_{IN} that results in the transistor being at the Edge of Saturation (EOS). For this case, the collector and base currents are given by:

$$I_{C(EOS)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} = \frac{(5-0.2)V}{1k\Omega} = 4.8mA \qquad (10.10)$$

$$I_{B(EOS)} = \frac{I_{C(EOS)}}{\beta_{DC}} = \frac{4.8mA}{50} = 0.096mA\,. \qquad (10.11)$$

Now, the input voltage is given by

$$V_{IN} = I_B R_B + V_{BE(ON)} \quad . \qquad (10.12)$$

Therefore, the input voltage at the Edge of Saturation is

$$V_{IN(EOS)} = I_{B(EOS)} R_B + V_{BE(ON)}$$

$$= (.096 \text{ mA})\ (10\text{k}\Omega)\ +\ 0.7 \text{ V} = 1.66 \text{ V}. \qquad (10.13)$$

Thus, $V_{IH} = V_{IN(EOS)} = 1.66$ V for this example. Finally, the output voltage levels are given by $V_{OH} = V_{CC} = 5$ V and $V_{OL} = V_{CE(SAT)} = 0.2$ V as shown in Figure 10.3.

It should be noted that input voltages between V_{IL} and V_{IH} (i.e., from 0.7 to 1.66 volts in the example) should be avoided because they lead to output voltage levels that are ambiguous. This results from the fact that the transistor is in its active region when the input voltages are in the transition region and this violates the constraint that the transistor should only operate in either its cutoff or saturated regions.

The difference between the two output voltages (V_{OH} - V_{OL}) determines the logic swing of the circuit. As shown in Figure 10.3, the logic swing is given by

$$\text{Logic Swing} = V_{OH} - V_{OL}. \qquad (10.14)$$

Notice that the output levels are compatible with the input levels since V_{OL} and V_{OH} are safely within the acceptable input LOW and input HIGH voltage regions, respectively. That is, the input LOW threshold voltage (V_{IL}) is greater than the output LOW-level voltage (V_{OL}). Hence, there is a safety margin of (V_{IL} - V_{OL}). This difference determines the LOW-level noise margin (NM_L) for the circuit and is given by

$$NM_L = V_{IL} - V_{OL}. \qquad (10.15)$$

Similarly, the difference (V_{OH} - V_{IH}) is the HIGH-level noise margin (NM_H) and is given by

$$NM_H = V_{OH} - V_{IH} \qquad (10.16)$$

The transition width (TW) is defined by the equation

$$TW = V_{IH} - V_{IL}, \qquad (10.17)$$

which is the minimum width of the transition between the two states. Notice that an increased noise-margin is obtained as either V_{OH} or V_{OL} move away from each other or as V_{IH} and V_{IL} move toward each other. Thus, with a larger logic swing or a narrower transition width, the noise margins improve.

10.3.2 TTL Inverter Transistor Diagram

Figure 10.4 illustrates the electronic components that comprise a typical TTL inverter such as the 7404. If the base current of Ql is less than $I_{IL,}$ which is defined as the

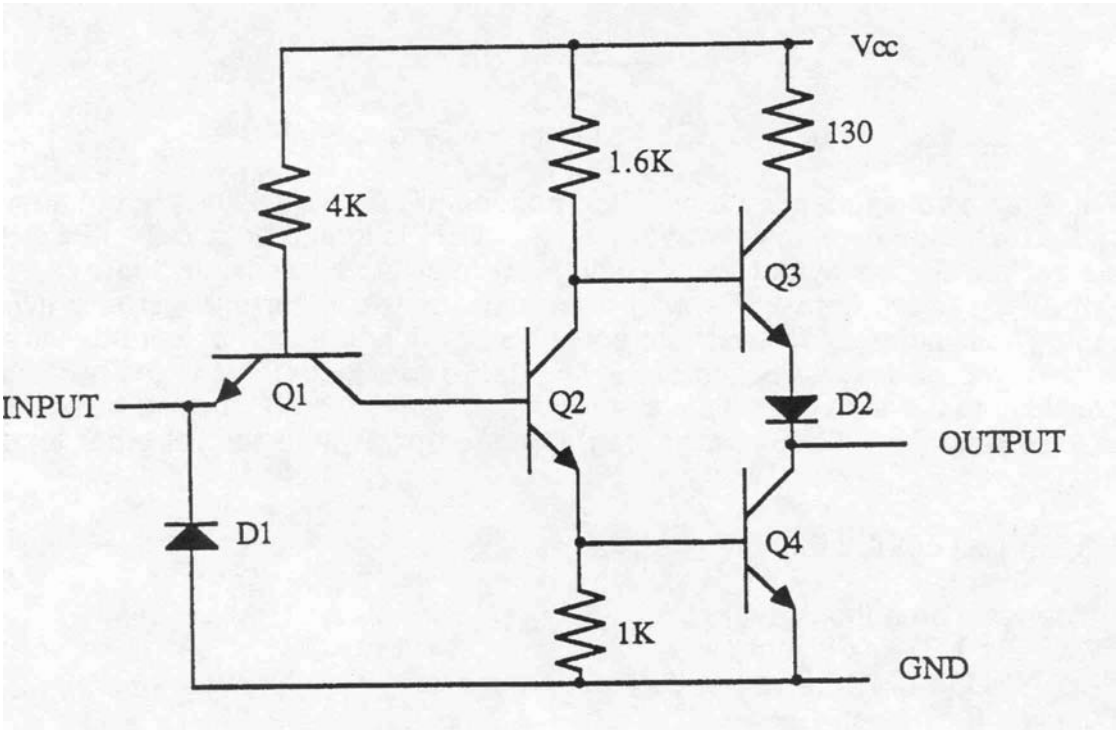

Figure 10.4: 7404 Inverter Circuit Diagram

low current (1.6 mA), Q1 is off and, consequently, Q2 is on, Q3 is off and Q4 is on and, therefore, the output is pulled low. When the base current of Ql equals or exceeds I_{IL}, Q1 turns on, turning Q2 and Q4 off and Q3 on, which pulls the output high through D2. Due to the fact that a considerable amount of current must be drawn from the emitter of Ql to convey a low input voltage, careless designers have, through the years, given rise to and spread the erroneous folklore that "unused or floating inputs to TTL circuits are assumed high so no connection is needed to hardwire a TTL input high". However, floating inputs cause unreliable operation that can be extremely difficult to troubleshoot and correct. Therefore, ***floating inputs should never to be included in any designs*.**

10.3.3 CMOS Inverter Transistor Diagram

Compared to the TTL Inverter described above, a CMOS Inverter circuit is much simpler. As shown in Figure 10.5, it consists solely of a mathched pair of n-channel and

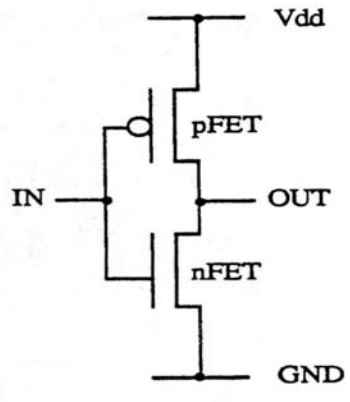

Figure 10.5: CMOS inverter circuit diagram

p-channel Field Effect Transistosr (FETs). Both FETs are enhancement mode devices. Using these two types of transistors, any desired Boolean logic function can be implemented. CMOS logic circuits have the unique property that the power supply current drain is virtually zero except when a logic transition is occurring. Furthermore,

the circuits have very high input resistance and relatively low output resistance, independent of the logic level. These desirable properties allow the circuits to be interconnected without regard to fan-out limitations in cases where speed is not paramount. A low input voltage turns the pFET on and the nFET off, causing the output to rise to V_{dd}. When the input voltage is high the pFET is turned off and the nFET is turned on, pulling the output low. During an input logic transition, there is an interval during which both FETs will be on and a pulse of current will be drawn from the power supply. This current spike occurs during every logical transition and causes the power dissipation, known as dynamic power, by the inverter to be proportional to the number of transitions that the inverter makes per second. At very high clocking rates, the power dissipation in CMOS circuits can approach or exceed that of other logic families. Dynamic power is given as $P_D = fC(V_{dd})^2$ where f is the clock frequency in Hertz, C is the capacitive load on the inverter, and V_{dd} is the inverter power supply voltage.

10.4. REQUIRED EQUIPMENT

Solderless Breadboard

Two 7404 TTL Hex Inverter ICs

Two 74HCO4 CMOS Inverter ICs

Function Generator & DC Power Supply

Oscilloscope

Digital Multi Meters (DMMs)

10.5. EXPERIMENTAL PROCEDURE

The connections built into the soderless breadboard include horizontal power busses and vertical signal busses as shown in Figure 10.6.

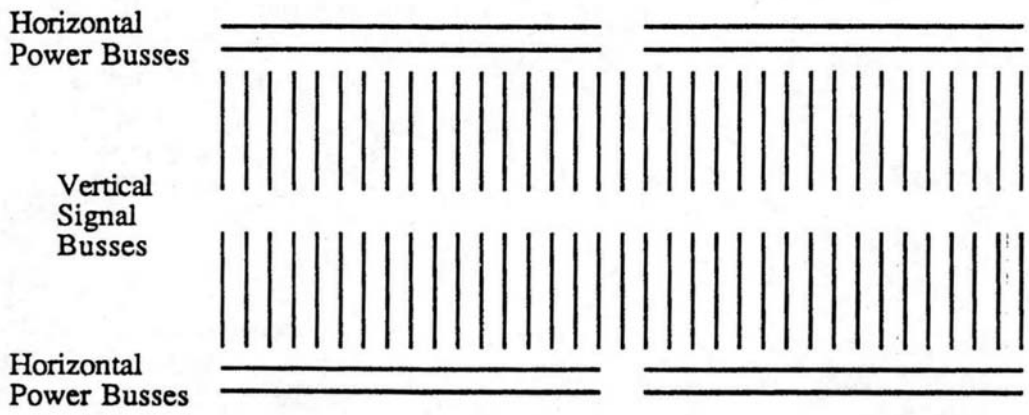

Figure 10.6: Solderless breadboard.

Note that the upper and lower vertical busses are independent and the left and right vertical busses are as well. Hence, you must insert the IC so that it straddles the centerline of the breadboard in the vertical dimension and if you need power and/or ground to be available along the entire horizontal bus you must insert a jumper to connect the left and right sides. You should connect the power supplies and insert the IC to be tested as shown in Figure 10.7.

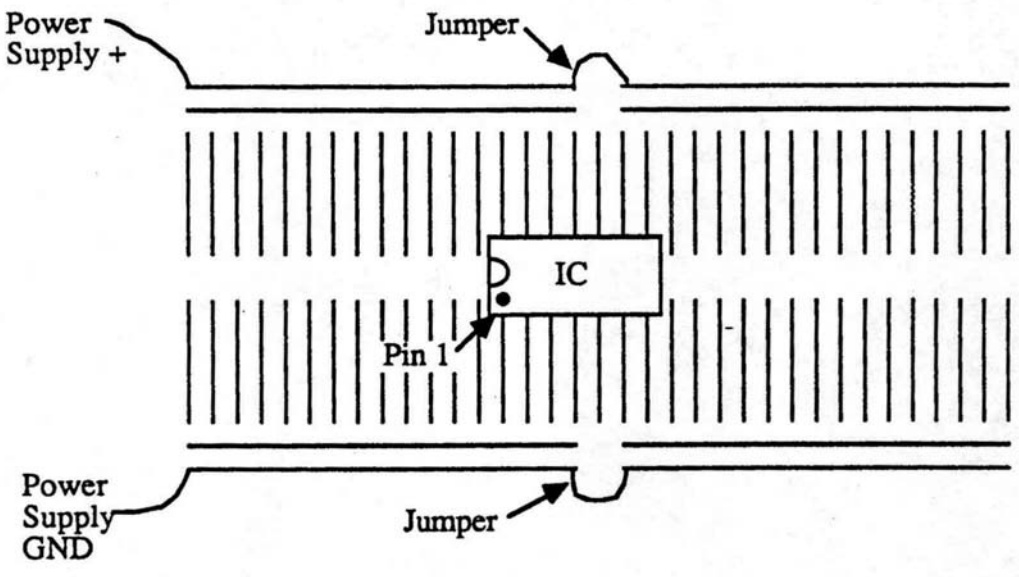

Figure 10.7: Proper IC placement and power connection.

Now, you will complete the following experimental procedures for both types of ICs, namely, the TTL 7404 and the CMOS 74HCO4 Hex Inverters. In both cases, you will be provided with a copy of the manufacturers' data sheets and be required to learn how to read and interpret the specifications given for each gate in order to determine some important characteristics of the two different logic families and compare these with the results of your measurements. Also, it should be noted that these two ICs are "pin for pin" compatible. This means that you can construct the required circuit(s) using the 7404 first and take your measurements for the TTL IC; then, you can simply remove the TTL IC and replace it with the 74HCO4 and take your measurements for the CMOS IC. (Note: Always shut off the power to your solderless breadboard whenever you modify the wiring or replace an IC).

10.5.1 Voltage Transfer Characteristic (VTC)

Unlike the logic gates used in introductory logic courses, real world gates do not have the classic inputs and outputs of "0" and "1". Instead, these are represented by voltage levels whose values are dependent upon the logic family. It is of interest to determine the quantitative relationship between the input and output voltages for the two inverters which were described qualitatively in the previous sections. These input-output relationship is known as the voltage transfer characteristics and can be measured by varying the input voltage while recording the resulting output voltage. A DC Power Supply will be used to measure the static output input-voltages and then the Function Generator and Scope in the X-Y mode to measure the dynamic transfer characteristics.

10.5.1.1 TTL Inverter Static Outputs

Connect the 7404 IC as shown in Figure 10.8. Note that you must implement a voltage follower like that shown in Figure 9.4 on the output on the DC Power Supply.

Slowly change the input voltage from 0 to +5 volts and verify that the output responds as expected, i.e., it changes from $V_{OH,}$ the Output High voltage, to $V_{OL,}$ the Output Low voltage. Measure and record V_{OH} and V_{OL} using the DMM or the oscilloscope.

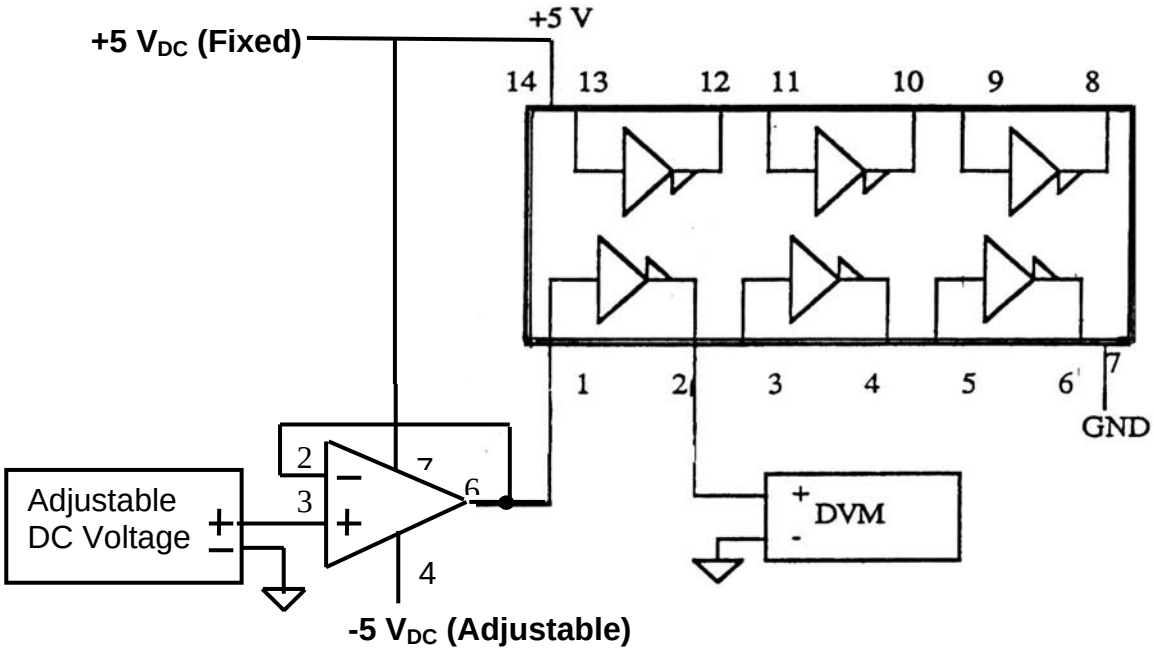

Figure 10.8: Setup for determination V_{OH} and V_{OL} for the 74X04 IC.

10.5.1.2 CMOS Inverter Static Outputs

Repeat the above procedure using the 74HC04 CMOS inverter.

10.5.1.3 TTL Inverter Voltage Transfer Characteristics

Construct the circuit shown in Figure 10.9 using one of the 7404 TTL Inverters. Before connecting the output of the function generator to pin 1 of the IC, you should adjust the waveform, amplitude, and DC offset of the generator to obtain the waveform shown in Figure 10.10. **DO NOT exceed 5 volts**. The frequency, while not critical, should be set to approximately 500 hertz.

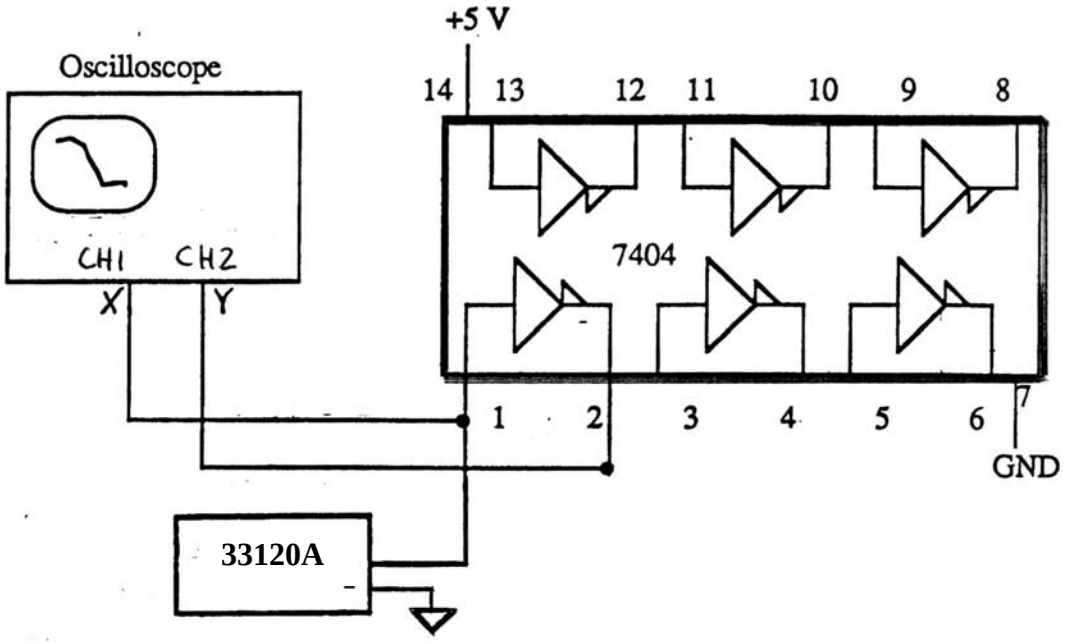

Figure 10.9: Setup for determination of 74x04 transfer characteristics.

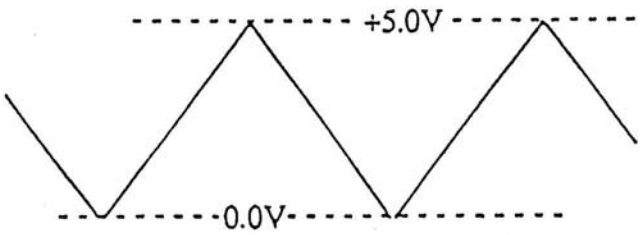

Figure 10.10: Function generator output waveform.

Once the function generator is correctly adjusted, connect its output to both pin 1 of the IC and to CH 1 of the scope. Connect the output on pin 2 of the IC to the CH 2 input of the scope. Set the Volts/Div of CH 1 and CH 2 to 1V/div. Choose X-Y mode of the scope.

With this setup, the scope is now in X-Y mode. In this mode the horizontal deflection of the scope trace is controlled by the voltage applied to CH 1 while the vertical trace deflection is determined by the voltage applied to CH 2. It should be clear that time has now been eliminated from the display, and that two voltages that have the

same period, when applied to CH 1 and CH 2, will give a stationary display whose width and height are adjustable by the Volts/div. controls of CH 1 and CH 2, respectively.

Now, with the triangular input driving the X-axis, when the input rises from 0 to +5 V, the sweep on the display will move from left to right a total of 5 divisions. Then it will move back when the input goes from +5 to 0 V and this process will repeat at a rate equal to the frequency of the function generator. At the same time, this signal is input to the inverter. So, the output of the inverter is also controlled by this signal. Since the output is connected to CH 2, which drives the vertical or Y axis, it follows that the changes in the output with respect to the input can be observed on the scope's display. A typical waveform is shown in Figure 10.11 where the output signal variations are shown as a function of the input signal going from 0 to 5 V and from 5 to 0 V. It follows that the vertical axis display will show the output going from V_{OH} to V_{OL} and then back from V_{OL} to V_{OH} with some hysteresis since the output variation is not the same for a positive going transition compared to a negative going one.

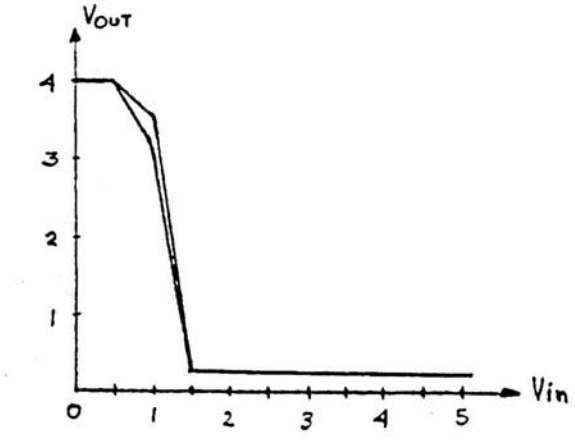

Figure 10.11: Typical 7404 Voltage Transfer Characteristic.

Now make a hardcopy the waveform seen on the scope, which is the voltage transfer characteristic, i.e., V_{OUT} versus V_{IN}. Identify V_{OH}, V_{OL}, V_{IH} and V_{IL} plus the transition region for your 74XO4 Inverter on the hardcopy.

10.5.1.4 CMOS Inverter Dynamic Transfer Characteristics

Repeat the above procedure using the 74HCO4 CMOS Inverter.

10.5.2 Power Dissipation

As with transfer characteristics, power consumption varies across logic families. In this part, you will determine the static power dissipation of the TTL 7404 and CMOS 74HCO4 Inverters and the dynamic power of the CMOS 74HCO4 Inverter

10.5.2.1 TTL Inverter Static Power Dissipation

Construct the circuit shown in Fig. 10.12. As indicated, connect all six of the inverters in parallel by jumpering the input pins 1, 3, 5, 9, 11 and 13 together. Connect a

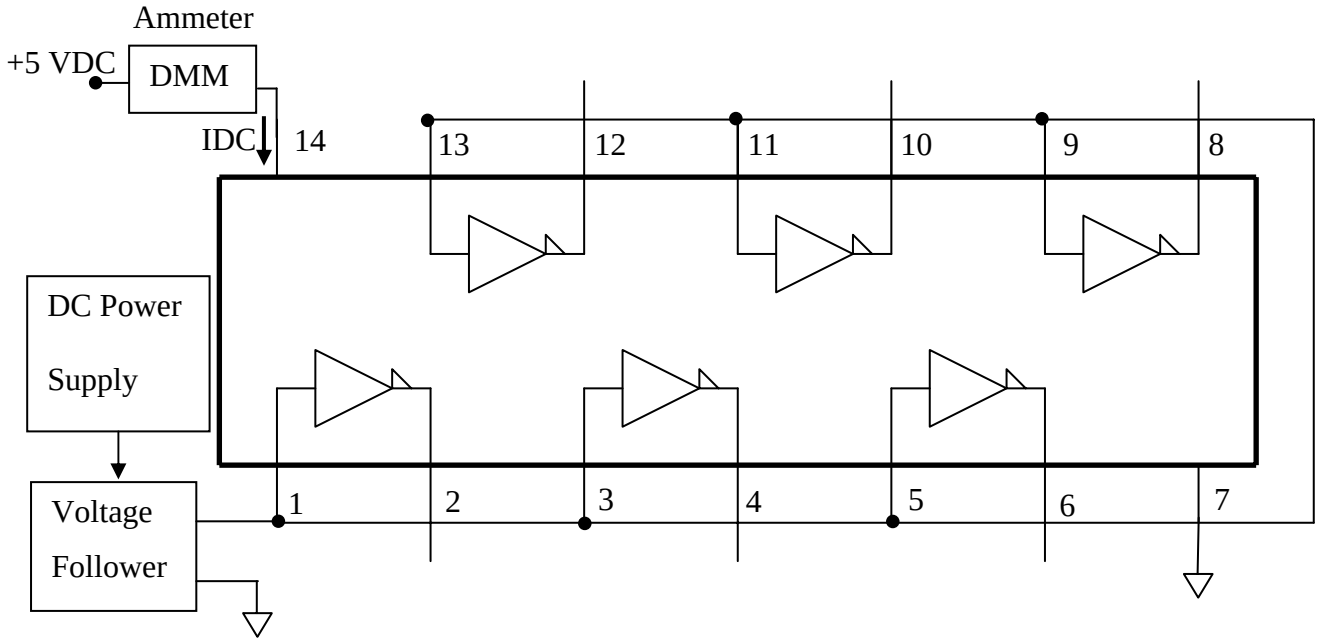

Figure 10.12: Setup to measure the supply current of the 74X04.

DMM in series with the +5 volt power supply and set it to read the current. Now, ***connect the other DC power supply using a voltage follower*** (see Figure 10.8) to the common input pins. Set its output first to be V_{OL} and then second to be V_{OH} while recording the power supply current when the input voltages are at each of these two levels.

10.5.2.2 CMOS Inverter Static Power Dissipation

Repeat the above procedure using the 74HCO4 CMOS Inverter.

10.5.2.3 Dynamic Power Dissipation

To illustrate dynamic power associated with the 74HCO4 CMOS Inverters, modify the circuit shown in Figure 10.12 by attaching 10 pF capacitors to each inverter output (pins 2, 4, 6, 8, 10, and 12). Substitute a square wave varying from 0 to +5 V with a 50% duty cycle using the function generator as the input voltage ***without the voltage follower***. Now, vary the frequency of the square wave from 10 Hz up to 100 kHz in even logarithmic steps (10 Hz, 100 Hz, 1 kHz, 10Hz, & 100 kHz) and measure and record the effect on the power supply current. Note that the average P_D = VDC*IDC/6.

10.5.3 Propagation Delay

Another important characteristic of digital logic devices is the propagation delay, which is defined as the time it takes a signal to propagate from the input to the output of the device. Again, in introductory courses on digital logic design, it is often assumed that a gate's propagation delay is zero. However, this is not the case with actual elements. In addition, elements from different logic families that perform the same function generally have different propagation delays. In this part of the experiment, you will determine the propagation delay for the TTL and CMOS Inverters.

While it is desirable to measure the propagation delay of an individual gate directly, this requires an oscilloscope with a very high bandwidth because the delay of

most elementary gates is only a few nanoseconds (ns). Since the oscilloscopes in the laboratory may not possess the necessary bandwidth to make these measurements directly, we will use an indirect method. The approach is to make a measurement on a large number of inverters connected in a ring to form what is known as a "Ring Oscillator". First, you can determine the total delay of all the inverters connected in the ring by measuring the period of the oscillation. The propagation delay of a single inverter can then be determined by dividing the period by twice the total number of inverters.

10.5.3.1 TTL Inverter Propagation Delay

Using two 7404 TTL ICs, construct the circuit shown in Figure 10.13. Notice that

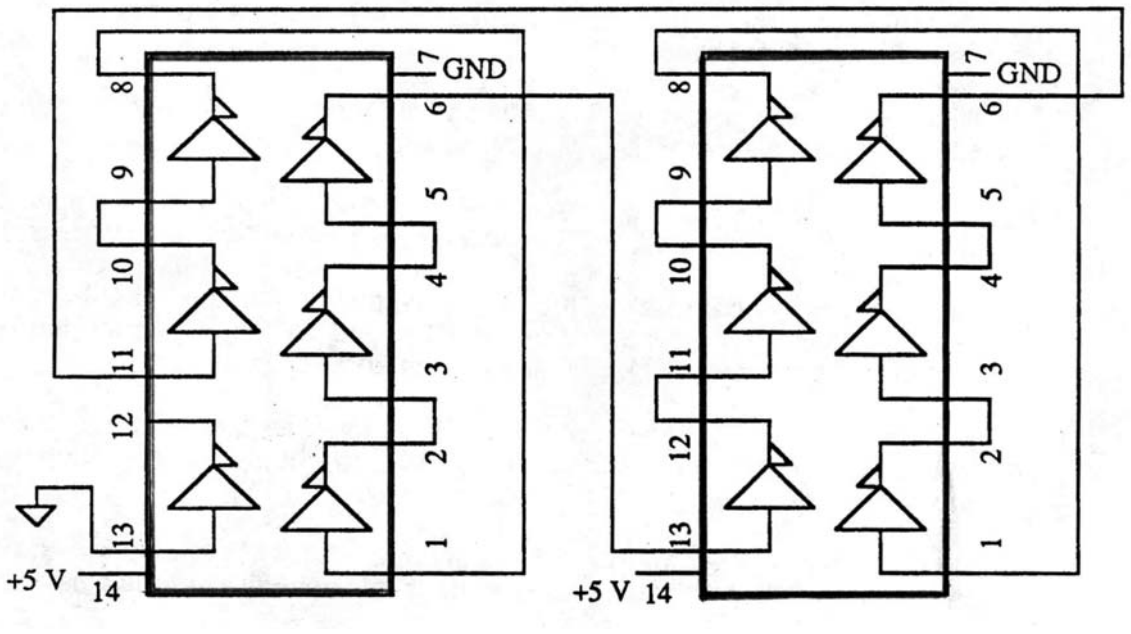

Figure 10.13: 74X04 IC 11 stage ring oscillator.

eleven inverters are used to construct the ring. Copy the waveform seen at the output of a selected inverter and measure the period of oscillation. (Note: If you don't observe an oscillating signal, then you should "debug" your circuit by using the scope to observe the

signals at the input and output of each inverter respectively, to verify correct wiring and/or to isolate a faulty inverter).

10.5.3.2 CMOS Inverter Propagation Delay

Repeat the above procedure using the 74HCO4 CMOS Inverter ICs.

10.6 REPORT

10.6.1 Determine the typical and maximum Logic Swing, Transition Width, and Noise Margin from the specifications for the TTL 7404 Inverter.

10.6.2 What are the TTL V_{OH} and V_{OL} that you measured in 10.5.1.1 and how do these compare to the specifications for the 7404 inverter? Is your gate within spec?

10.6.3 Label the voltage transfer characteristic (i.e., V_{OUT} versus V_{IN}) of the 7404 from your copy in section 10.5.1.3. Identify V_{OH}, V_{OL}, V_{IH} and V_{IL} plus the transition region of your gate on your transfer characteristic.

10.6.4 Determine the power dissipation of a 7404 inverter as a function of input voltage. Is the power dissipation higher for a input HIGH or LOW? What is the average power dissipation assuming a 50% duty cycle? How do your measurements compare to the ones obtained by using the data from the TTL specifications

10.6.5 Include the copy of the waveform observed at the output of a selected inverter of the ring oscillator and indicate the measured period. Calculate the average propagation delay through the 7404 based on the measured ring oscillator period. Compare this to the 7404 propagation delay TTL specifications.

10.6.6 Determine the typical and maximum Logic Swing, Transition Width, and Noise Margin from the specifications for the CMOS 74HCO4 Inverter.

10.6.7 What are the CMOS V_{OH} and V_{OL} that you measured per Section 10.5.1.2 and how do these compare to the CMOS specifications for the 74HCO4 inverter?

10.6.8 Label V_{OUT} and V_{IN} for the 74HC04 on your hardcopy of its voltage transfer characteristic and identify V_{OH}, V_{OL}, V_{IH} and V_{IL} plus the transition region.

10.6.9 Plot the power dissipation of the CMOS inverter as a function of frequency. What is its predicted static (DC or zero frequency) power dissipation? Does this agree with your static (DC) measurements?

10.6.10 Calculate the average propagation delay through the 74HC04 inverter using the measured ring oscillator period. How does this compare to the value obtained from the CMOS specifications?

10.6.11 The power delay product (or speed-power product) is defined as the product of the propagation delay time (Tpd) and power dissipation (Pd) of the gate. Calculate the power delay product for the CMOS inverter.

10.6.12 Based upon the analysis performed in this experiment, describe the major differences between these two IC logic families. In particular, address the differences in their transfer characteristics (i.e., logic swing, noise immunity, and transition width), power consumption, and speed of operation. Finally, list some applications where CMOS is a better choice than TTL and vice versa.

10.6.13 Design Problem: For the transistor in the logical inverter circuits of Figure 10.14, assume that $\beta_{DC(min)} = 50$ and $R_3 = 1\ M\Omega$. Find values for R_1 and R_2 such that the first inverter can drive 4 identical inverter circuits simultaneously, i.e, it has a 'fan out' of 4 as shown. Standard 5% resistors must be used for R_1 and R_2.

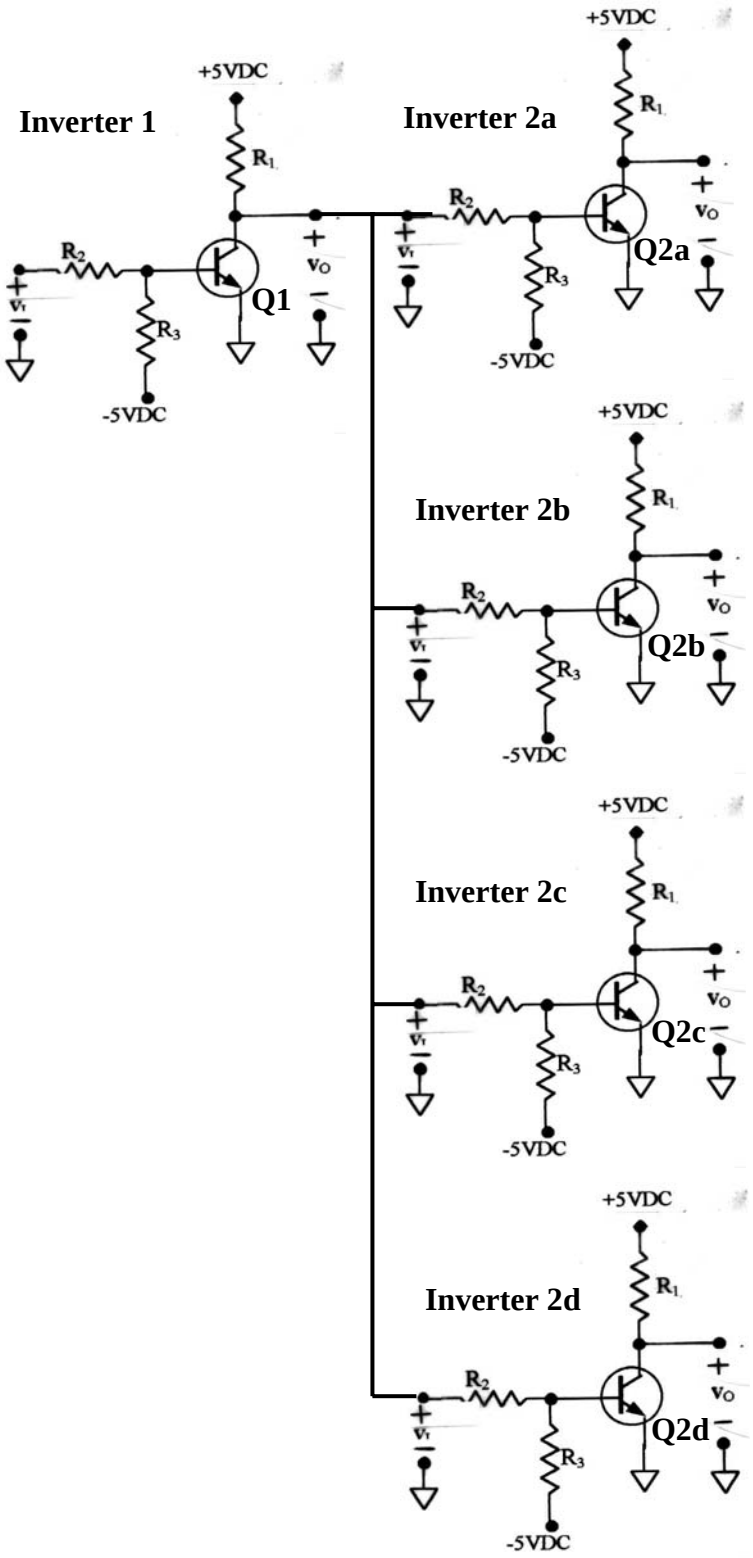

Figure 10.14: Transistor Inverter Fan-Out of Four

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