CIRCUITS LABORATORY

EXPERIMENT 7

Design of a Single Transistor Amplifier

7.1 OBJECTIVES

The objectives of this laboratory are to:

(a) Gain experience in the analysis and design of an elementary, single transistor amplifier,

(b) Build and thoroughly test the amplifier,

(c) Make a careful comparison between the amplifier's design specifications and the experimental measurements with corrective action being taken for any results that do not agree with theory.

7.2 INTRODUCTION

The single transistor amplifier is one of the major keys to understanding the analysis and design of all analog electronic systems. Stereos, television sets, radios, long distance telephone communication circuits, and many other practical systems employ principles that we will explore in this experiment.

An elementary common emitter (CE) transistor amplifier will be designed from principles reviewed here. The amplifier will be constructed during the laboratory period and measurements carefully taken to verify that the design is correct and that all results agree with theoretical predictions. ***Extensive*** calculations must be made to insure that the amplifier data agrees accurately with theory ***before*** leaving the laboratory.

7.3. THEORY

7.3.1 THE BASIC CE EQUATIONS

The common emitter (CE) emitter amplifier configuration will be employed in this experiment. The basic CE circuit is shown in Figure 7.1.

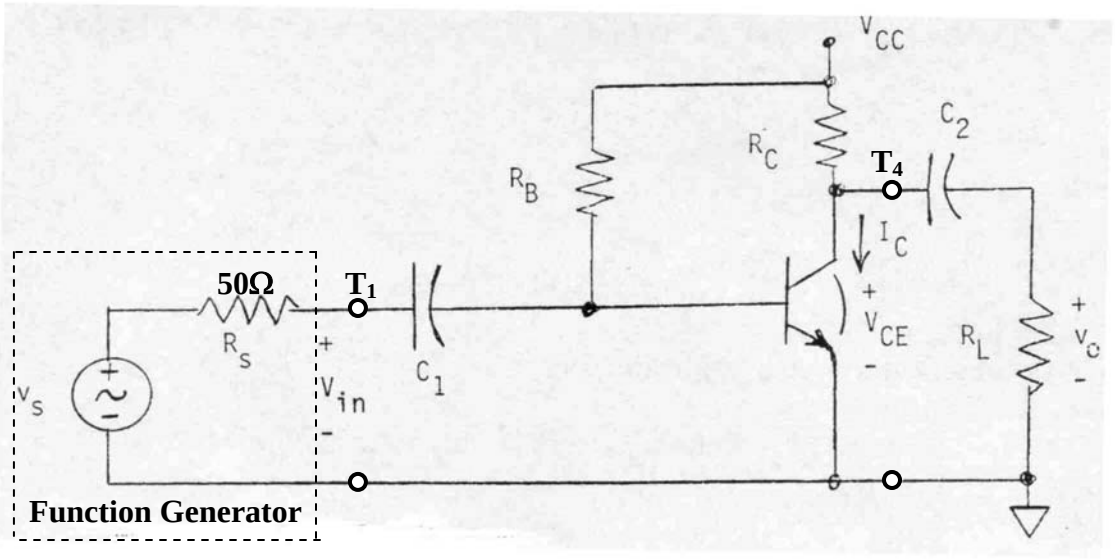


Figure 7.1. The Basic Common Emitter Amplifier

Figure 7.2 below is the small signal, midfrequency, incremental model corresponding to our CE circuit. Note that the midfrequency model assumes that the

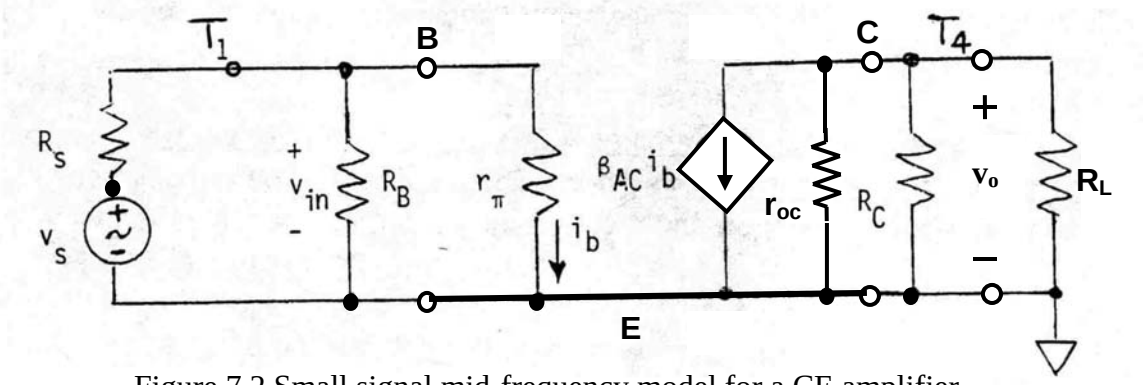


Figure 7.2 Small signal mid-frequency model for a CE amplifier

impedances due to C_1 and C_2 are negligible compared to the impedance of related components in the circuit. Using the *Voltage Amplifier* model shown in Section 7.6.1,

the various relations shown in Table 1 can be derived from the circuit of Figure 7.2. The "Remarks" column gives further insight relative to each equation.

Table I. Fundamental Design Equations for the Common Emitter Amplifier

Quantity	Equation	Eq. No.	Remarks
Theoretical BJT input resistance	$r_\pi = \frac{V_T(\beta_{AC})}{I_{CQ}}$	(7.1)	V_T = Thermal Voltage, r_π is in ohms.
Input resistance (T_1 to common)	$r_i = r_\pi // R_B$	(7.2)	$r_i \approx r_\pi$ if $R_B >> r_\pi$.
Output resistance (T_4 to common)	$r_o = R_C // r_{oc}$	(7.3)	$r_o \approx R_C$ if $r_{oc} >> R_C$.
No load incremental voltage gain	$a_{VO} = \frac{v_{OC}}{v_{in}} = -\frac{\beta_{AC} r_o}{r_\pi}$	(7.4)	Derived from Figure 7.2 with $R_L = \infty$ (Open Circuit.)
Collector bias Current	$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_C}$	(7.5)	$V_{CEQ} \equiv v_{CE}$ at transistor Q pt. See Fig. 7.4
Base bias resistor value	$R_B = \frac{(V_{CC} - v_{be}(on))(\beta_{DC})}{I_{CQ}}$	(7.6)	$v_{be}(on) \approx 0.7$ volt for Silicon BJT transistors
Input coupling capacitor value	$C_1 = 1/[\omega_{1i}(R_S + r_i)]$	(7.7)	$C_1 = \approx 1/(\omega_{1i} r_i)$ if $r_i >> R_S$ ω_{1i} = half power frequency
Output coupling capacitor value	$C_2 = 1/[\omega_{1o}(r_o + R_L)]$	(7.8)	$C_2 \approx 1/(\omega_{1o} R_L)$ if $R_L >> r_o$ ω_{1o} = half power frequency

Notes: (a) See Appendix 7.6.1 on page 7-17 for a standard Voltage Amplifier model.

(b) Equation (7.4) negative sign represents inversion, i.e., a 180° phase shift.

(c) Upper case letters represent quiescent or DC values, e.g., V_{CEQ}.

(d) Lower case letters represent incremental or AC values, e.g., v_{in} and v_o.

(e) $\beta_{DC} \equiv$ Common emitter quiescent current gain $= I_{CQ} / I_{BQ}$.

(f) $\beta_{AC} \equiv$ Common emitter incremental current gain $= \Delta i_C / \Delta i_B$ for V_{CEQ} constant.

(g) r_{oc} = output resistance = $\Delta v_{CE} / \Delta i_C$ at constant I_{BQ}.

This table contains many of the fundamental relations for the design of the CE amplifier. For example, if r_i, r_o, and a_v were given in a set of specifications, Equations (7.1) through (7.4) could be employed to find the β_{AC} required of the transistor for a satisfactory design. All of these equations will be employed later in our work.

7.3.2 THE INPUT COUPLING CAPACITOR

Figure 7.3 is a basic model for determining the lower cutoff frequency, f_{1i}, for the amplifier input coupling capacitor, C_1, but the form of the equation is the same for determining C_2. Note that v_s is the source voltage, v_{in} is the input voltage to the coupling capacitor, r_i is the input resistance of the amplifier, and v_r is the voltage across r_i.

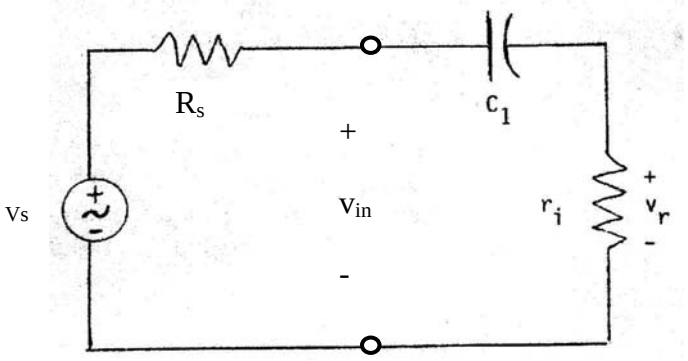


Figure 7.3: Equivalent circuit for coupling capacitor

Using phasors and applying the voltage divider rule we find that

$$\frac{V_r}{V_s} = \frac{r_i}{R_s + \dfrac{1}{j\omega C_1} + r_i} \tag{7.8}$$

where ω is the radian frequency of v_s. Equation (7.8) yields

$$\left|\frac{V_r}{V_s}\right| = \frac{r_i}{\left|(R_S + r_i) + \dfrac{1}{j\omega\, C_1}\right|} = \frac{r_i}{\sqrt{(R_S + r_i)^2 + \left(\dfrac{1}{\omega\, C_1}\right)^2}} \tag{7.9}$$

At radian frequencies well above cutoff, Equation (7.9) reduces to

$$\left|\frac{V_r}{V_s}\right| = \frac{r_i}{(R_S + r_i)} \tag{7.10}$$

From Equation (7.10), it is clear that the *lower cutoff frequency* or the *lower -3dB frequency* occurs when $\left|\frac{V_r}{V_s}\right| = \frac{r_i}{\sqrt{2}\,(R_S + r_i)}$. Denoting the lower cutoff frequency by ω_{1i}, we get

$$\left|\frac{V_r}{V_s}\right|^2 = \left(\frac{r_i}{\sqrt{2}(R_S + r_i)}\right)^2 = \frac{r_i^{\,2}}{\left(\frac{1}{\omega_{1i} C}\right)^2 + (R_S + r_i)^2} \qquad (7.11)$$

From Equation (7.11), we see that $\omega_{1i} = 2\pi f_{1i} = \frac{1}{(R_S + r_i)C_1}$ or, alternatively,

$$C_1 = \frac{1}{\omega_{1i}(R_S + r_i)} = \frac{1}{2\pi f_{1i}(R_S + r_i)} \qquad (7.12)$$

Note that $C_1 \approx \frac{1}{\omega_{i1} r_i} = \frac{1}{2\pi f_{1i} r_i}$ if $r_i >> R_S$. See Equation (7.7) in Table I.

As an example, if an amplifier has an input resistance r_i of 1 kΩ and it is desired to capacitively couple a low impedance input signal v_s to it so that the cutoff frequency, f_1, is 200 Hz, we substitute into Equation (7.7) and find

$$C_1 = \frac{1}{2\pi(200)(1000)} = \frac{10^{-5}}{4\pi} = 7.96(10)^{-7} = 0.796\ \mu F. \qquad (7.13)$$

7.3.3. THE LOAD LINE

The load line is a valuable design tool, particularly in determining the effect of large signals on transistor circuit performance. In Experiment 6, the emphasis was on the static load line with a slope = $-1/R_C$ and there was no capacitively coupled load. Equivalently, load was $R_L = \infty$. When $R_L \neq \infty$, the AC signal "sees" the dynamic load line described below.

Figure 7.4 shows idealized transistor characteristics with both static and dynamic of load lines. First, the static line is constructed in the usual way and the quiescent point established. Then, the dynamic line having a slope of $-1/(R_L||R_C)$ is placed on the graph with the new line also passing through the same Q point.

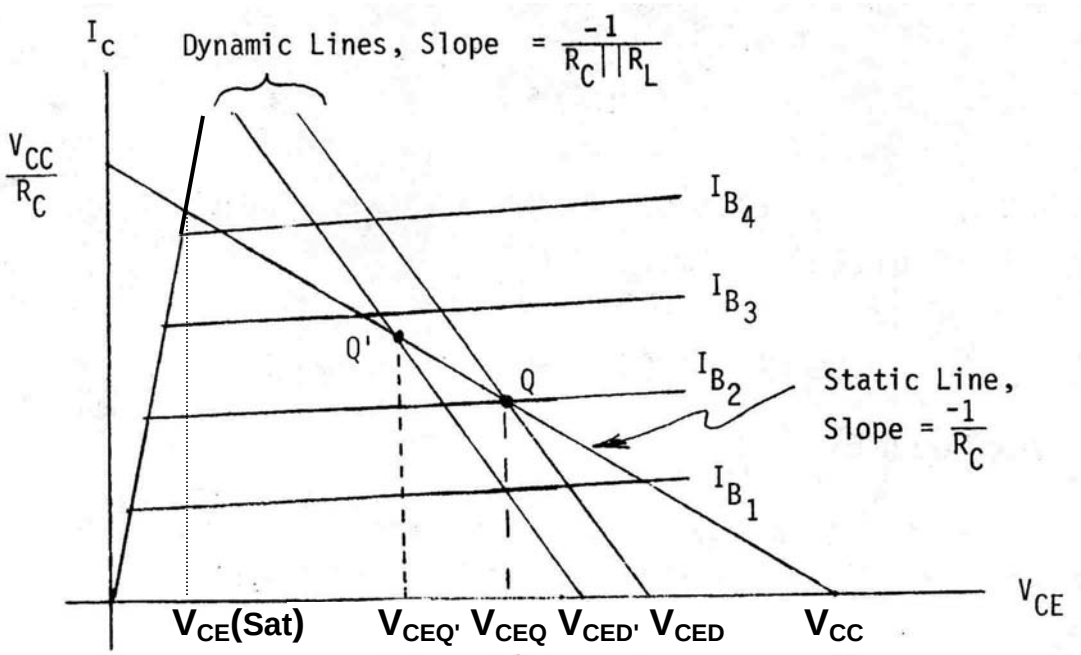
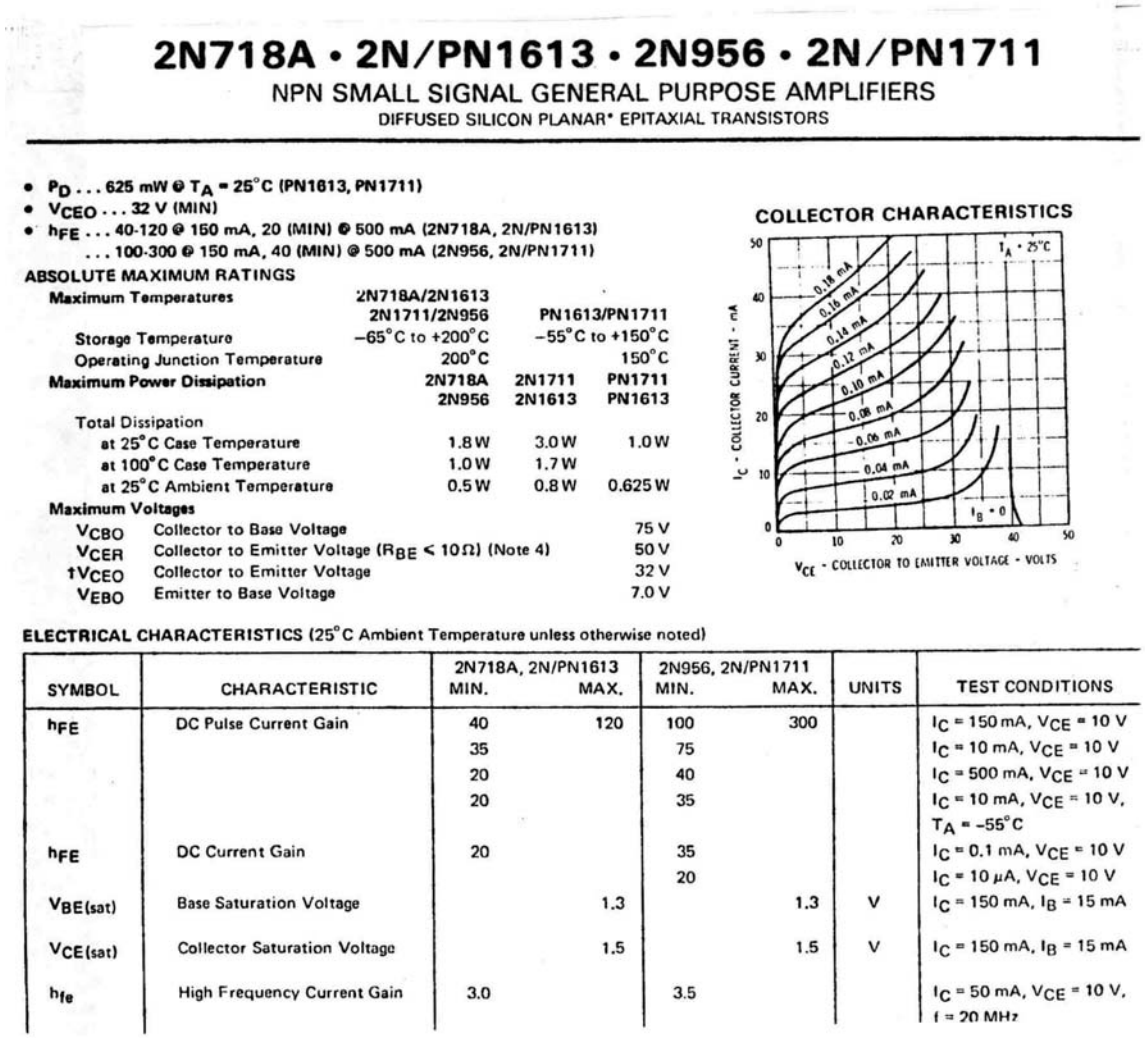


Figure 7.4: Static and Dynamic Load Lines

From the static line it is seen that $v_o = v_{CE}$ has a positive swing of $S^+ = (V_{CC} - V_{CEQ})$ before the transistor is cutoff and a negative swing of $S^- = (V_{CE}(Sat) - V_{CEQ}) \approx -V_{CEQ}$ before saturation. To get the maximum positive and negative voltage swings with a static line, the operating point is frequently placed near the center, i.e., $V_{CEQ} = 0.5\ V_{CC}$, which is termed midpoint biasing. In this case, the total peak-to-peak output voltage $v_{opp} = (S^+ - S^-) \approx 2\ V_{CEQ} = V_{CC}$. On the other hand, the dynamic line produces cutoff at a lower voltage and has a smaller positive swing of $S^+ = (V_{CED} - V_{CEQ})$ so that the maximum unclipped $v_{opp} = 2\ (V_{CED} - V_{CEQ})$. The positive swing S^+ for the dynamic line may be increased by establishing a new quiescent point called Q' at $V_{CEQ'}$ as shown in Figure 7.4. Observe that the slopes of both dynamic lines are the same, but the Q' point is moved to the left along the static line. This process can be done either analytically or by inspection of the graph. Usually, Q' is moved to a new point where a symmetric swing is established for both positive and negative going signals. The result is that $v_{opp} = 2\ V_{CEQ'}$ where $V_{CEQ'} = [R_L/(R_C + 2\ R_L)]\ V_{CC}$.

7.3.4 Nonlinear Response and Distortion

From the actual characteristic for the 2N718A transistor shown in Figure 7.5, it is seen that an actual transistor has a non-ideal family of curves. Equal increments in I_B are not uniformly spaced on the graph.



2N718A • 2N/PN1613 • 2N956 • 2N/PN1711

NPN SMALL SIGNAL GENERAL PURPOSE AMPLIFIERS

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- P_D . . . 625 mW @ T_A = 25°C (PN1613, PN1711)
- V_{CEO} . . . 32 V (MIN)
- h_{FE} . . . 40-120 @ 150 mA, 20 (MIN) @ 500 mA (2N718A, 2N/PN1613)
  . . . 100-300 @ 150 mA, 40 (MIN) @ 500 mA (2N956, 2N/PN1711)

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	2N718A/2N1613 2N1711/2N956		PN1613/PN1711
Storage Temperature	−65°C to +200°C		−55°C to +150°C
Operating Junction Temperature	200°C		150°C
Maximum Power Dissipation	2N718A 2N956	2N1711 2N1613	PN1711 PN1613
Total Dissipation			
at 25°C Case Temperature	1.8 W	3.0 W	1.0 W
at 100°C Case Temperature	1.0 W	1.7 W	
at 25°C Ambient Temperature	0.5 W	0.8 W	0.625 W

Maximum Voltages

V_{CBO}	Collector to Base Voltage	75 V
V_{CER}	Collector to Emitter Voltage ($R_{BE} \leq 10\Omega$) (Note 4)	50 V
†V_{CEO}	Collector to Emitter Voltage	32 V
V_{EBO}	Emitter to Base Voltage	7.0 V

COLLECTOR CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N718A, 2N/PN1613 MIN.	2N718A, 2N/PN1613 MAX.	2N956, 2N/PN1711 MIN.	2N956, 2N/PN1711 MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Pulse Current Gain	40	120	100	300		I_C = 150 mA, V_{CE} = 10 V
		35		75			I_C = 10 mA, V_{CE} = 10 V
		20		40			I_C = 500 mA, V_{CE} = 10 V
		20		35			I_C = 10 mA, V_{CE} = 10 V, T_A = −55°C
h_{FE}	DC Current Gain	20		35			I_C = 0.1 mA, V_{CE} = 10 V
				20			I_C = 10 μA, V_{CE} = 10 V
$V_{BE(sat)}$	Base Saturation Voltage		1.3		1.3	V	I_C = 150 mA, I_B = 15 mA
$V_{CE(sat)}$	Collector Saturation Voltage		1.5		1.5	V	I_C = 150 mA, I_B = 15 mA
h_{fe}	High Frequency Current Gain	3.0		3.5			I_C = 50 mA, V_{CE} = 10 V, f = 20 MHz

Figure 7.5: A brief data sheet for the 2N718A transistor.

Moreover, the pattern of the I_B curves changes with both V_{CE} and I_C. Thus, a load line on the graph with a Q point near the center presents a different effective β_{AC} to parts of a sinewave input signal falling some distance on either side of Q. The result is distortion in the output signal, i.e., it is no longer a pure sinewave.

7.3.5 Design Specifications

Specifications may occur in one of several classes. At one extreme is the situation where the amplifier is over specified; i.e., too many variables are constrained. Consider the following elementary set as a case of over specification: a_{vo} = -200, β_{AC} = 50, R_C = 2kΩ and r_π = 1kΩ. Substitute into Equation (7.4) to obtain

$$\left|a_{Vo}\right| = \left|\frac{(-50)(2k\Omega)}{1k\Omega}\right| = 100 \neq 200 \qquad (7.14)$$

The above is a trivial example of an invalid specification, but the designer must be alert to more subtle conflicting specifications. At the other extreme is a very common situation where the amplifier is under specified, e.g., a_{vo} = -200 and β_{AC} = 10 are the only constraints. Here the designer has a infinite number of satisfactory values for R_C and r_π for Equation (7.4). Nevertheless, the values selected for the free parameter(s) must first be consistent with good electronic engineering practices, and, beyond that, they must be the best possible fit within the context of the application as it is understood by the engineer. A common variation of under specification happens when one or more parameters are specified as "greater than or equal to". Since components have tolerances and values that often change with age, it is good practice to take advantage of the "inequality" specifications, but by "how much" involves judgment and knowledge of the application. For simplicity we do not consider cost here, but be aware that in practice it frequently is one of the most critical parameters.

7.3.6 A Design Example

6.1 Specifications. The desired design is a CE amplifier with the following specified parameters:

$$R_C = 2\ \text{k}\Omega,\ V_{CEQ} = 3\ \text{V},\ |\ a_{vo}\ | > 250, \text{ and } f_{1i} \le 200\ \text{Hz}.$$

The load resistance is to also be the collector resistor of the transistor circuit, i.e., C_2 is omitted and $R_L = \infty$. Characteristics given for the transistor are $\beta_{AC} = \beta_{DC} = 50$ and $I_{Cmax} = 9$ mA. Standard 5% resistors are to be employed. See Appendix II in Section 7.6.2.

6.2 The Design Process. The equations needed for our work are numbered sequentially and found in Table 1. From the above specification that $R_C = 2\ \text{k}\Omega$, which is a standard 5% resistor, and assuming that r_{oc} is very large, we get from Eq. (7.3) that $r_o = 2\ \text{k}\Omega$. Since $V_{CEQ} = 3$ V, then $V_{CC} >> 6$ V. Arbitrarily, try $V_{CC} = 9$ V. Then from Equations (7.5) and (7.1) we get

$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_C} = \frac{9-3}{2000} = 3mA\,. \tag{7.15}$$

and

$$r_\pi = \frac{(26)\beta_{AC}}{I_{CQ}} = \frac{(26)(50)}{3} = 433.3\Omega\,. \tag{7.16}$$

From Equation (7.4),

$$a_{Vo} = -\frac{\beta_{AC} R_C}{r_\pi} = -\frac{(50)(2)}{0.433} = -231 \tag{7.17}$$

which does not satisfy the specification. Thus, we must modify some of the previous values to get a satisfactory $a_{vo.}$

From the previous work, we observe that a larger V_{CC} will lead to a larger I_C, leading to a smaller r_π and finally to a larger a_{vo}. So, as a first iteration in the design, we will increase V_{CC} to 20 V.

Recomputing, from Equation (7.5),

$$I_{CQ} = \frac{20\,V - 3\,V}{2\,k\Omega} = 8.5\,mA\,; \tag{7.18}$$

and from Equation (7.1),

$$r_\pi = \frac{(26)(50)}{8.5} = 153\,\Omega\,; \tag{7.19}$$

and from Equation (7.4),

$$a_{Vo} = -\frac{(50)(2\,k\Omega)}{.153\,k\Omega} = -\,654\,. \tag{7.20}$$

Since a_{vo} is so much larger than the specification requires and since I_{CQ} is close to the specification limit, a reasonable approach is to select V_{CC} about midway between 9 V and 20 V, say at V_{CC} = 15 V. Trying this value and using the same set of equations, we find:

I_{CQ} = 6 mA, which is significantly less than the maximum.

r_π = 217 Ω, which is acceptable since its value is unspecified, and

a_{vo} = 461 V/V, which is well above the specified minimum.

The design is completed by finding R_B and C_1. From Equation (7.6),

$$R_B = \frac{(V_{CC} - 0.7)}{I_{CQ}}(\beta_{DC}) = \frac{(15\,V - 0.7\,V)(50)}{6} = 119\,k\Omega \approx 120\,k\Omega\,, \tag{7.21}$$

which is a standard 5% resistor. Note that 120kΩ >> r_i = 0.217kΩ; therefore, our original assumption of $R_B >> r_\pi$ is satisfied for Equation (7.2). The change to R_B = 120 kΩ has negligible effect on several previous parameters, e.g., I_{CQ} = 5.96 mA instead of 6 mA, but these are of no practical consequence for the design. Finally, from Equation (7.7),

$$C_1 = \frac{1}{\omega_{1i} r_i} = \frac{1}{2\pi(200)(217)} = 3.7\,\mu F. \tag{7.22}$$

The next largest standard sized capacitor would be suitable.

7.4 Experiment

7.4.1 Design Problem

7.4.1.1 Design Specifications

Design an open circuit ($R_L = \infty$) common emitter transistor amplifier to meet the following characteristics: $r_i \geq 1$ kΩ , $r_o < 2$ kΩ, $160 \leq |a_{vo}| \leq 240$, $f_{1i} \leq 400$ Hz, $v_{op\text{-}p} \geq 10$ V where $v_{op\text{-}p}$ is the unclipped peak-to-peak output voltage. Select an integer value for supply voltage V_{CC} and assume V_{CC} has an accuracy of ±2 %. A 2N2222A transistor with $\beta_{DC} = \beta_{AC} = 175 \pm 25$ and $r_{oc} > 25$ kΩ is to be used. The base and/or collector resistances may each use two standard ± 5% resistors combined in series

7.4.1.2 Initial Design

As a laboratory team, you are to design a capacitor coupled transistor amplifier that satisfies the design specifications based on the nominal transistor characteristics given in Section 7.4.1.1. The design must include a circuit diagram of the transistor amplifier and values must be defined for all components shown on the diagram. These may be shown directly on the circuit diagram or in a table. As a team, you must present the initial design to the instructor for approval prior to obtaining a 2N2222A transistor.

7.4.1.3 Revised Design

Obtain a 2N2222A transistor and use the Tektronix 571 Curve Tracer to obtain its characteristics. Draw the load line for your initial design on the transistor characteristics and mark the design Q point. For this Q point, calculate the β_{DC}, β_{AC}, and r_{oc} for the transistor. If the transistor meets the requirements, complete a revised design by modifying the base resistance and present it to the instructor. If the transistor does not meet requirements, obtain a different transistor and repeat the above steps.

7.4.1.4 Final Design

Your final design must operate at the initial design Q point, i.e., the initial design V_{CEQ} and I_{CQ}. Once you have assembled your amplifier per Section 7.4.4, turn on power, allow it to stabilize at operating temperature, and measure V_{CEQ} and I_{CQ}. If necessary, change the base resistance to obtain the correct Q point. Record any design changes made.

7.4.2 Warning

The transistor is a small device with little thermal capacity. Even an extremely brief over-voltage or over-current fault will destroy the device or permanently alter its properties. Therefore, you ***must not attempt to build a transistor circuit or alter any connections while the power is on.*** Also***, you must not apply any input signal voltage directly to the base of the transistor without a series resistor or capacitor***.

7.4.3 Equipment List

1	Transistor curve tracer
1	Motorola 2N2222A transistor (150 mA, 60 V) with $\beta_{DC} = \beta_{AC} = 175 \pm 25$
2	Capacitors – values determined by design calculations
4	Quarter watt, 5% resistors (Values selected from 10% list in Sect. 7.6.2.)
1	0 – 40 V DC power supply
2	10x Probes
1	Digital Oscilloscope
1	HP 33120A Function Generator
1	50Ω, 20dB signal attenuator
1	Decade resistor box
3	Digital multimeters (DMMs)

7.4.4 Experimental Procedure

7.4.4.1 General Guidelines

(a) A digital oscilloscope, with its sensitive measurement capability, high input resistance, and low input capacitance, can be used to make accurate signal voltage measurements and should be used in preference to the DMM for this purpose. To

accurately measure power supply or bias voltages, the DMM is preferable.

(b) Since the amplifier that is to be designed is relatively high gain, the ***LOW output of the HP33120A function generator and a 50Ω, 20dB signal attenuator must be used for the signal source***. Since the attenuator output impedance is 50Ω, its value can often be neglected in gain measurements, but should be taken into account in measuring r_i.

(c) Frequency can most conveniently be measured with the oscilloscope. Do not depend on the accuracy of the dial reading of the HP 33120A function generator.

7.4.4.2 Detailed Laboratory Steps

(a) Perform the initial and revised designs per paragraphs 7.4.1.2 and 7.4.1.3.

(b) Construct your amplifier circuit using 1 or 2 standard resistors for collector resistance (R_C) and a 1 kΩ shunt resistor and the decade box in series for the base resistance (R_B). See the circuit shown in Figure 7.1. Adjust the power supply voltage to the design V_{CC} value ± 2% before connecting the amplifier.

(c) With $v_s = 0$, measure the bias voltages and currents, e.g., V_{CEQ}, I_{CQ}, V_{BEQ}, and $I_{BQ.}$ Refer to Experiment 6 for the best ways to measure I_{CQ} and $I_{BQ.}$ If during this step the measured values of V_{CEQ} and I_{CQ} fail to agree with the design values, adjust the decade box resistance to change the base resistance as needed to achieve the Q point values. Be sure to record any changes made for this amplifier final design.

(d) Replace the base resistance with 1 or 2 standard resistors in series and verify that the correct Q point is obtained.

(e) With v_s set at mid-frequency value (40 kHz) and an output voltage v_o = 2 V RMS:

(1) Determine a_{vo} using the digital oscilloscope. Note $R_L = \infty$, and v_{in} is measured just to the source side of C_1. See Figure 7.1.

(2) Place a decade box with resistance R_{DB} = 0 Ω between the Function Generator and the coupling capacitor (See Figure 7.1) and measure v_o with the scope. Increase R_{DB} until v_o drops to one-half its original value, which is the "half voltage method" for determining r_i. (The decade box should yield at least three significant figures.) Now remove the decade box from the circuit and measure and record its value.

(3) Similar to step (e.2) directly above, measure r_o by placing a decade box in the R_L position with R_{DB} = 999,999 Ω. Be sure $C_2 = C_1$ is large enough so that its impedance has a negligible effect on the r_o measurement. Measure v_o with the scope while adjusting R_{DB} until v_o drops to one-half its original value, yielding the measured r_o value. Record r_o and return the circuit to $R_L = \infty$.

If any of the measured values fall outside the specification limits of paragraph 7.4.1.1, you must note this and check with the instructor before proceeding any further.

(f) Ranging from about 2 octaves below the lower cutoff up to 2 octaves above the upper cutoff, take appropriate frequency response data with the oscilloscope. For this run, $R_L = \infty$ and $R_S \approx 50$ Ω. **Note that v_{in} should be measured and recorded to be sure it stays essentially constant**. Use the scope's frequency measuring feature to set accurate frequency values, but check them using the function generator's frequency scale.

Frequency response testing can best be accomplished as follows. First, with v_{in} at a mid-frequency value, set v_o to 5.66 V peak-to-peak (2 V RMS) by observing v_o on the scope and adjusting the magnitude of $v_{in.}$ Next, increase and decrease the frequency of v_s in order to determine the lower cut-off frequency (f_1) and the upper cut-off fequency (f_2), respectively. Since the cut-off frequency is defined as the half-power point, then it follows that v_o = 0.707 (5.66 V) = 4 V peak-to-peak at the respective cut-off frequencies.

To obtain adequate data points near the two cut-off frequencies, record the peak-to-peak values of v_o and v_{in} at the following frequencies without adjusting v_s:

$f_1 / 4$	two octaves down from the lower cut-off frequency
$f_1 / 2$	one octave down from the lower cut-off frequency
f_1	lower cut-off frequency
$2 f_1$	one octave up from the lower cut-off frequency
$4 f_1$	two octaves up from the lower cut-off frequency
$10 f_1$	one decade up from the lower cut-off frequency
$f_o/4$	two octaves down from the mid-range frequency
f_o	mid-range frequency where $f_o = \sqrt{f_1 f_2}$
$4 f_0$	two octaves up from the mid-range frequency
$f_2 /10$	one decade down from the upper cut-off frequency
$f_2 / 4$	two octaves down from the upper cut-off frequency
$f_2 / 2$	one octave down from the upper cut-off frequency
f_2	upper cut-off frequency
$2 f_2$	one octave up from the upper cut-off frequency
$4 f_2$	two octaves up from the upper cut-off frequency

(g) Return to a mid-frequency value, i.e., f_o, and take data, v_o vs. v_{in} with the scope to determine the linearity of the amplifier from v_o = 0.5 V RMS until obvious clipping occurs. When clipping occurs, instead of being a pure sinusoid, v_o will have a significant flattening, either on the top due to cutoff or on the bottom due to saturation or both. Monitor v_{in} and v_o with separate oscilloscope channels. Record where distortion starts by noting the value of v_o where the gain ($a_{vo} = |v_o/v_{in}|$) begins to noticeably decrease. Also, record the value of v_o where clipping occurs.

(h) Connect a load resistor $R_L = 2R_C$ using a coupling capacitor $C_2 = C_1$. Now record the value of v_o where clipping occurs. This value should be noticeably smaller than that of Section (g). Also, draw the dynamic load line on the transistor characteristics and compare measured and predicted results.

(i) Graphically determine a new Q' point that will lead to the largest total possible output voltage swing with $R_L = 2R_C$. Plot the dynamic load lines through Q and Q'. Note that it will be necessary to change the value of base resistance R_B when implementing the new operating point, Q'. Now repeat part (h) for a new dynamic quiescent point Q'.

7.5. Report

7.5.1 Present the curve tracer characteristics for your 2N2222A transistor and show the construction of your static load line. Be sure to label your Q point including I_{BQ}, V_{CEQ}, and $I_{CQ.}$ Show all the data points used to determine β_{DC}, $\beta_{AC,}$ and r_{oc} on the characteristics and also show your calculations for β_{DC}, $\beta_{AC,}$ and r_{oc}.

7.5.2 Present the initial and revised designs that were approved by the instructor. Present all pertinent information, e.g., r_i, r_o, a_{vo}, v_{op-p} (output voltage swing), f_{1i}, R_B, R_C, C_1, V_{CC}, V_{CEQ}, I_{CQ}, I_{BQ}, β_{DC}, $\beta_{AC,}$ r_π, r_{oc}, etc., on the table provided.

7.5.3 Present a comparison showing your approved amplifier initial, revised, and final design values and the actual measurements made during test. Include all pertinent information, e.g., r_i, r_o, a_v, v_{op-p} (output voltage swing), f_{1i}, R_B, R_C, C_1, V_{CC}, V_{CEQ}, I_{CQ}, I_{BQ}, β_{DC}, $\beta_{AC,}$ r_π, r_{oc}, etc., on the table provided.

7.5.4 Make a graph showing the measured frequency response of your amplifier by plotting $|a_{vo}| = |v_o|/|v_{in}|$ versus frequency. Use a log scale for frequency. Indicate the half power points and the amplifier bandwidth.

7.5.5 Make a graph for the linearity measurements made at mid-frequency by plotting v_o versus v_{in}. Indicate on your graph where distortion and clipping each begin.

7.5.6 Show the construction of your dynamic load lines with the Q & Q' point(s) included as related to Sect 7.4.4.2 (h) and (i) and calculate v_{opp} for each case.

7.5.7 The v_{opp} is described on page 7-6 and measurements are taken in experiment steps (g), (h), and (i) of Section.7.4.4.2. Make a table presenting the calculated and measured data for v_{opp} (1) without R_L and (2) with R_L using both the Q and Q' operating points.

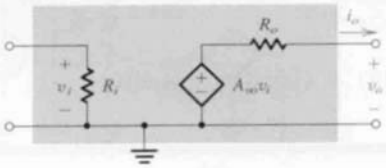
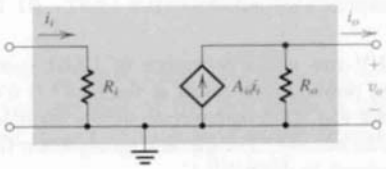
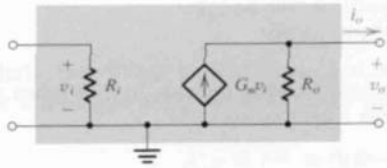
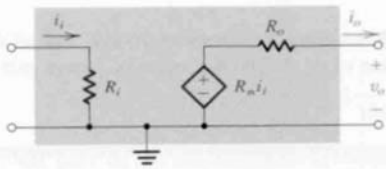
7.5.8 Derive Equation (7.4) in Table I on page 7-3 from basic principles.

7.6 Appendices

7.6.1 Appendix I - Standard Amplifier Models

There are four standard amplifier models as shown in the table below. Even though the transistor is a current controlled device, we will make use of the Voltage Amplifier for this experiment since it is the most often used model.

Table 1.1 THE FOUR AMPLIFIER TYPES

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} = \left.\frac{v_o}{v_i}\right\|_{i_o = 0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} = \left.\frac{i_o}{i_i}\right\|_{v_o = 0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m = \left.\frac{i_o}{v_i}\right\|_{v_o = 0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m = \left.\frac{v_o}{i_i}\right\|_{i_o = 0}$ (V/A)	$R_i = 0$ $R_o = 0$

7.6.2 Appendix II - Resistor Value Multipliers

These values all apply to ± 5% tolerance resistors. Resistors with ± 10% tolerance are only available in values marked by a *. The multipliers are:

1.0*	1.5*	2.2*	3.3*	4.7*	6.8*
1.1	1.6	2.4	3.6	5.1	7.5
1.2*	1.8*	2.7*	3.9*	5.6*	8.2*
1.3	2.0	3.0	4.3	6.2	9.1

7.7 References

1. Sedra, Adel S. and Smith, Kenneth C., **Microelectronic Circuits,** 5th Edition, Oxford University Press, New York, 2004
2. Boylestead, Robert and L. Nashelsby, ***Electronic Devices and Circuit Theory*** (4th ed.), Prentice-Hall, Englewood Cliffs NJ, 1987.
3. Chirlian, Paul M., ***Analysis and Design of Integrated Electronic Circuits***, Harper and Row, Cambridge MA, 1981.
4. Grinich, Victor H., and H. G. Jackson, ***Introduction to Integrated Circuits***, McGraw-Hill, New York NY, 1970.
5. Millman, Jacob, ***Microelectronics - Digital and Analog Circuits and Systems***, McGraw-Hill, New York NY, 1979.
6. Mitchell, Jr., F. H., and F. H. Mitchell, ***Introduction to Electronics Design***, Prentice-Hall, Englewood Cliffs NJ, 1988.