Delta-Sigma ADC

(Download Houser Handout from Web Page)

What if the Quantization Noise isn’t flat like it is for a Conventional ADC?

- We saw that we could improve our SNR (increase the number of bits in our converter) by Low Pass Filtering (Decimating) the Quantization noise.
- What if the Quantization Noise had this shape?
  - Then, our Low Pass Filter would take out much more of the Quantization Noise, especially if the corner were around 20KHz.
  - If the Bandwidth of the Input Signal is much less than the Bandwidth of the Quantization Noise, then Decimating down to the Input Signal Bandwidth will remove a lot of the Quantization Noise.
  - Delta-Sigma ADCs do just that. The Modulator shapes the Quantization Noise as in the above graph and the Decimator removes most of it.
  - For a 2nd order Delta-Sigma Modulator you pick up about 2 ½ bits per octave of oversampling (Eq. 28 from Hauser). You only pick up ½ bit per octave if the Quantization Noise is flat. (Eq. 8 from Hauser)
Delta-Sigma ADCs have 2 parts
  ○ Noise Shaping Modulator
  ○ Digital Decimation Filter

**Block Diagram of a Delta-Sigma Converter**

![Block Diagram](image)

Fig. 7. Generic noise-shaping feedback loop. Block \( H(z) \) — discrete-time analog filter containing one or more integrations.

1\textsuperscript{st} and 2\textsuperscript{nd} Order Modulators from Figure 14 in Hauser:

Fig. 14. Common delta–sigma modulator configurations of (a) first order (one integrator) and (b), (c) second order (two integrators). All time delay in these diagrams is explicit in the unit-sample delay blocks, labeled $z^{-1}$. The rightmost blocks are called 1-bit quantizers in communication theory and comparators in circuit design. Configurations (b) and (c) differ in circuit timing and other practical details but yield similar OSADC SNR performance.
AIWN Model for Figure 14(a) from Hauser

1st Order Modulator

Analyzing $H(z)$:

$v[n] = v[n-1] + u[n-1]$

$V(z) = z^{-1}V(z) + z^{-1}U(z)$ (Time-Shifting property of the Z-Transform)

$H(z) = \frac{V(z)}{U(z)} = \frac{z^{-1}}{1-z^{-1}}$

$= \frac{1}{z-1}$

Equations for Block Diagram:

$Y(z) = [X(z) - Y(z)]H(z) + Q(z)$

$Y(z) + Y(z)H(z) = X(z)H(z) + Q(z)$

$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z)$

Substituting for $H(z)$:

$Y(z) = \frac{1}{z-1}X(z) + \frac{1}{1+\frac{1}{z-1}}Q(z)$

$Y(z) = \frac{1}{z}X(z) + \frac{z-1}{z}Q(z)$

$F_x(z) = \frac{1}{z} = z^{-1}$ Pure Delay (Hauser Eq.17)

$F_Q(z) = \frac{z-1}{z}$ First Order Highpass Filter (Hauser Eq.18)
Pole-Zero plot for $F_Q(z)$

Magnitude Spectrum for $F_Q(\omega)$

Similar to Figure 8 from Hauser.
AIWN Model for Figure 14(b) from Hauser

2nd Order Modulator

Analyzing $H_1(z)$:

\[ y[n-1] + x[n] = y[n] \]
\[ z^{-1}Y(z) + X(z) = Y(z) \]
\[ H_1(z) = \frac{1}{1 - z^{-1}} \]
\[ = \frac{z}{z - 1} \]

Analyzing $H_2(z)$:

\[ y[n-1] + x[n-1] = y[n] \]
\[ z^{-1}Y(z) + z^{-1}X(z) = Y(z) \]
\[ H_2(z) = \frac{z^{-1}}{1 - z^{-1}} \]
\[ = \frac{1}{z - 1} \]
Equations for Block Diagram:

\[
W(z) = H_1(z)[X(z) - Y(z)] - Y(z)
\]

\[
Y(z) = Q(z) + W(z)H_2(z)
\]

\[
W(z) = \frac{[Y(z) - Q(z)]}{H_2(z)}
\]

\[
\frac{[Y(z) - Q(z)]}{H_2(z)} = H_1(z)[X(z) - Y(z)] - Y(z)
\]

\[
Y(z) - Q(z) = H_1(z)H_2(z)X(z) - H_1(z)H_2(z)Y(z) - H_2(z)Y(z)
\]

\[
Y(z) = \frac{H_1(z)H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)}X(z) + \frac{1}{1 + H_1(z)H_2(z) + H_2(z)}Q(z)
\]

\[
F_x(z) = \frac{H_1(z)H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = \frac{z}{z-1} \frac{1}{1+\frac{z}{z-1}} = \frac{z}{z-1} + \frac{1}{z-1}
\]

\[
= \frac{1}{z}
\]

\[
F_Q(z) = \frac{1}{1 + H_1(z)H_2(z) + H_2(z)} = \frac{1}{1+\frac{z}{z-1}} + \frac{1}{z-1}
\]

\[
= \frac{1}{(z-1)^2 + z + z-1} = \frac{(z-1)^2}{z^2 - 2z + 1 + 2z-1}
\]

\[
= \frac{(z-1)^2}{z^2}
\]

Pole-Zero plot for \(F_Q(z)\)
Double Pole at \(z=0\), Double 0 at \(z=1\).

Magnitude Spectrum for \(F_Q(\omega)\)
Analyzing the SNR for a 1 bit Delta-Sigma using the AIWN model for the 2nd order modulator from Hauser Fig 14b:

$N_0$ is the single sided PSD for AIWN. The 1 bit converter has 2 values, $+\Delta$ and $-\Delta$. So the step size is $\Delta$.

$$N_0 = \frac{\Delta^2}{12 \omega_s} \quad \omega_s = 2\pi$$

$N_0 = \frac{\Delta^2}{12\pi}$

$P_Q$ is the Quantization Noise Power. To calculate this, integrate the Power Spectral Density over the final bandwidth. This is the best case estimate of the Noise Power after Decimation.

$$P_Q = \int_0^{BW} \left| F_Q(\omega) \right|^2 \cdot N_0 \, d\omega = \int_0^{BW} \left| F_Q(\omega) \right|^2 \, d\omega$$

$P_X$ is the Maximum Signal Power. The maximum amplitude is $\Delta$, the same as the swing of the 1 bit comparator.

$$P_X = \frac{\Delta^2}{2}$$

$$\text{SNR} = 10 \log \left( \frac{P_X}{P_Q} \right) = 10 \log \left[ \frac{\frac{\Delta^2}{2}}{\int_0^{BW} \left| F_Q(\omega) \right|^2 \, d\omega} \right] = 10 \log \left[ \int_0^{BW} \left| F_Q(\omega) \right|^2 \, d\omega \right]$$

$$\text{SNR(BW)} := 10 \log \left[ \int_0^{BW} \left| F_Q(\omega) \right|^2 \, d\omega \right]$$

$$\text{NumBits(BW)} := \frac{\text{SNR(BW)} - 1.76}{6.02}$$
Checking against Equation (28) in Hauser:

Quantization Noise for the 1 Bit Converter:

\[
10 \log [\text{SNR}_{1\text{Bit}}] = 10 \log \left( \frac{\Delta^2}{2 \Delta^2 + 12} \right) + 10 \log(6)
\]

\[\text{SNR}_{1\text{Bit}, \text{dB}} = 7.78\]

\[\text{SNR}_{\text{Eq28}}(L) := \text{SNR}_{1\text{Bit}, \text{dB}} + \text{SNR}_{\text{Enhancement}}(L)\]

\[\log_2(x) := \frac{\ln(x)}{\ln(2)}\]

\[D(\omega) := \frac{\pi}{\omega}\]

\[\text{SNR}(D(64)) = 100.246\]

\[\text{SNR}(D(32)) = 70.148\]
These 2 graphs match Fig. 13 from Hauser.
Summary:

- Delta-Sigma ADCs have 2 parts
  - Noise Shaping Modulator
    - High Pass Filters the Quantization Noise
    - Analyze the Modulator by itself first. Integrate the Power Spectral Density from of the Modulator Output from 0 to the Decimated $F_s/2$. This simulates a brick wall filter for the Decimator. That is, we are assuming there is no Noise Power between the Decimated $F_s/2$ and the Modulator $F_s/2$.
  - Digital Decimation Filter
    - Low Pass Filter the output of the Modulator. The corner should be at the Decimated $F_s/2$. However, you might have to do this in 2 stages of decimation.
    - Downsample the Low Pass Filter output to the Decimated $F_s$. That is, pick every Nth sample of the Low Pass Filter. Throw the rest away.
    - There is no reason to calculate the Low Pass Filter outputs that are going to be thrown away.
    - When measuring the Noise Power here, make sure to integrate to the Decimated $F_s/2$, and not just to the end of the Signal Bandwidth.

- In order to reduce the variance of the Power Spectral Density, Average multiple trials. For each iteration, vary the phase of the input.
- Integrate the PSD to get the Noise Power. Use the maximum amplitude sine wave for the Signal Power.
- Calculate the effective number of bits from SNR using Equation (3) from the Hauser paper.
- Equation (28) from the Hauser paper assumes that the Quantization Noise is AIWN. Figure 13 from the Hauser paper shows the difference between that assumption and reality.

References:

- Dr. Morley’s EE437 Lecture Notes, Fall 2003.