Lecture 16
Physical Design, Part 2

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http://classes.engineering.wustl.edu/ese461/
Placement

• Place logic cells within the flexible blocks

• Ideal objectives
  - guarantee the router can complete the routing step
  - minimize all the critical net delays
  - make the chip as dense as possible
  - minimize power, crosstalk between signals

• Realistic objectives
  - minimize total estimated interconnect length
  - meet the timing requirement for critical nets
  - minimize the interconnect congestion
Placement Terms

- Over the cell routing (OTC)
- Channel capacity
- Feedthroughs (feedthrus)
- Jumper (unused vertical track in a cell)
Placement Terms

- Manhattan distance vs Euclidean distance
- Minimum Rectilinear Steiner Tree (MRST)
Placement Algorithms

- **Constructive placement method**
  - **Min-cut algorithm**
  - cut the placement area into two pieces
  - swap logic cells to minimize cut cost
  - repeat and cut smaller pieces till all cells placed
Placement Algorithms

- **Constructive placement method**
  - Eigenvalue placement algorithm
    - cost matrix or weighted connectivity matrix
    - quadratic optimization problem
- **Iterative placement method**
  - take existing placement and improve it
  - pairwise interchange algorithm
  - force-directed algorithm
Physical Design Flow

- Design entry
  - logic description with no physical information
- Logic synthesis
- Initial floorplan
- Synthesis with load constraints
- Timing-driven placement
- Synthesis with in-place optimization
- Detailed placement
- Global routing
- Detailed routing
Global Routing

• Two types of areas to global route
  - inside the flexible blocks
  - between blocks

• Objectives
  - start from a floorplan and placement
  - minimize the total interconnect length
  - maximize the probability that the detailed router can complete the routing
  - minimize the critical path delay
Measurement of Interconnect Delay

- Elmore delay model
  - after placement, the logic cell position fixed
Global Routing Between Blocks

- Numbering channels
- Channels form the edge of a graph
- Each channel has a capacity
Global Routing Between Blocks

- Find terminals of nets
- Find minimum-length tree
- Minimum-length tree $\neq$ Minimized delay between terminals (A1 to D1)
Detailed Routing

• Goal
  - complete all connections between logic cells

• Objectives
  - minimize total interconnect length and area
  - minimize # of layer changes (vias)
  - minimize delay of critical paths
Detailed Routing

- Routing pitch rules
  - via-to-via (VTV) pitch
  - via-to-line (VTL) pitch
  - line-to-line (LTL) pitch

- Waffle via
- Stacked via
Router’s View of the Cell

- **Phantom**

1. electrically equivalent connectors; router can connect to top or bottom and use connectors as a feedthrough
2. equivalent connectors; router can connect to top or bottom but cannot use as a feedthrough
3. must-join connectors, router *must* connect to top *and* bottom
4. internal connector
5. track location blocked by $m_2$ inside cell
6. off-grid connector
7. connector with no equivalent
8. feedthrough between equivalent connectors with internal jog
9. routing grid
10. cell abutment box
Terms in Detailed Routing

- **Trunks**
  - running in parallel to the channel

- **Branches**
  - connecting trunk to terminals

- **Tracks**
  - horizontal track spacing

- **Terminal**
  - column spacing
Terms in Detailed Routing

(a) 4 horizontal tracks

horizontal track pitch = 8 \( \lambda \)

expanded view of channel

4 \( \lambda \)

(b) cell abutment box

4 \( \lambda \)

(c) vertical track pitch = 8 \( \lambda \)

vacant terminal

unused terminal

logic cell

m1

m2

branch

trunk or segment

dotted line

pseudo-terminal

net exiting channel

via1

connector, terminal, port, or pin

via1 = m1 + m2 + contact

1 2 0 1 4 0 0 6 0 6 0 8 9 0 9
Channel Density

- Global density
- Local density
Detailed Routing

- Manhattan routing
  - preferred direction
  - preferred metal layer
  - logic cell connectors on 1 metal only
2-Layer Routing

• Left-edge algorithm
  - 1. sort the nets from the leftmost edge
  - 2. assign first net to the first free track
  - 3. assign next net that can fit to the track
  - 4. repeat step 3 until no more net can fit
  - 5. repeat step 2-4 until all nets assigned
Left-Edge Algorithm Example

Segments sorted by their left edge.

(a) Left edge of segment 7 connects to top of channel.

Net 6 has 3 terminals.

(b) Segments assigned to tracks by their left edges.

(c)
Multi-Layer Routing

• Polysilicon + 2-level metal
  - 2.5-layer routing
  - poly only for short connections

• 3-layer routing
  - M1 horizontal, M2 vertical, M3 horizontal (HVH)
  - M1 vertical, M2 horizontal, M3 vertical (VHV)
  - M3 pitch is multiples of M1
3-Layer Routing Example
Final Routing Steps

• Timing-driven detailed routing
  - reduce # of vias
  - alter interconnect width
  - minimize overlap capacitance

• Unroutes
  - leave problematic nets unconnected
  - complete interconnects with violation

• To resolve
  - discover the reason and revisit synthesis and floorplan
  - return to global router, change bin size
  - engineering change orders (ECO)
  - via removal and routing compaction
Special Routing

- **Clock Routing**
  - minimize clock skew
  - clock tree synthesis
  - clock-buffer insertion

- **Activity-induced skew**
  - supply noise
Special Routing

- Power Routing
  - electromigration
  - size the power buses according to the current

<table>
<thead>
<tr>
<th>Layer/contact/via</th>
<th>Current limit</th>
<th>Metal thickness</th>
<th>Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>m1</td>
<td>1 mA m m⁻¹</td>
<td>7000 Å</td>
<td>95 m W /square</td>
</tr>
<tr>
<td>m2</td>
<td>1 mA m m⁻¹</td>
<td>7000 Å</td>
<td>95 m W /square</td>
</tr>
<tr>
<td>m3</td>
<td>2 mA m m⁻¹</td>
<td>12,000 Å</td>
<td>48 m W /square</td>
</tr>
</tbody>
</table>

- tap-cell
- end-cap cell
- de-cap cell
Notes

- Encounter tutorial to be discuss next lecture
- Detailed class project description
  - to be release by Friday
  - behavioral code to be submitted
  - account for 30% of the project
  - by 11/22 before thanksgiving
  - if late, by 11/28, discount by 40%
Questions?

Comments?

Discussion?