Lecture 8
Overview of VLSI Design Flow

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http://classes.engineering.wustl.edu/ese461/
Application Specific Integrated Circuit (ASIC) Type

- **Full-custom**
  - transistors are hand-drawn
  - best performance (although almost extinct)
  - still using to optimized standard cell
- **Gate Array (for small volumes)**
  - use sea of gates (mask-programmable gate arrays)
  - FPGA (reconfigurable)
- **Standard Cell**
  - only use standard cell from the library
  - dominate design style for ASIC (what we are going to use)
Standard Cell ASICs

- Also called Cell-based ICs (CBIC)
- Fixed library of cells
- Design style
  - cells synthesized from Verilog
  - schematic based on interconnection of cells
  - place and routed automatically
Standard Cell Design Flow

- **Behavior**
  - define function and specification
  - hardware algorithms

- **Structural: Front end design**
  - verilog coding
  - simulation
  - logic synthesis
  - simulation again
  - verified by FPGA testing

- **Physical: Back end design**
  - floor planning, placement, routing
  - post simulation
  - tape-out
Standard Cell Design Flow
Example: IBM Standard Cell

- **Document**
  - /IBM-7RF/digital_kit/ibm_cmos7rf_std_cell_20111130/std_cell/v.20111130/doc

- **Schematic**
  - /IBM-7RF/digital_cdslib/ibm_cmos7rf_cdslib/cdslib

- **Symbol**
  - /IBM-7RF/digital_kit/ibm_cmos7rf_std_cell_20111130/std_cell/v.20111130/symbol_61

- **Layout**
  - /IBM-7RF/digital_kit/ibm_cmos7rf_std_cell_20111130/std_cell/v.20111130/gds2

- **Verilog**
  - /IBM-7RF/digital_kit/ibm_cmos7rf_std_cell_20111130/std_cell/v.20111130/verilog
Example: IBM Standard cell

- Clock rail
- Power rail
- Well
- Cell I/O
- Ground rail

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Tools

- **Synopsys**
  - VCS, for verilog simulation
  - Design Compiler, for front end design
  - IC Compiler, for back end design

- **Cadence**
  - NC Sim, for verilog simulation
  - RTL Complier (RC), for front end design
  - SOC Encounter, for back end design
RTL Complier

- Netlist
- Timing report
- Area report
- Power report
SOC Encounter
Outline

Overview

Tcl Basics
Tcl Script

- **Tools command language (Tcl, tickle)**
  - script language
  - used for synthesis, rapid prototyping, GUI
  - easy to learn but powerful

- **Features**
  - everything is a command, including structure
  - everything can be dynamically redefined and overridden
  - full unicode (3.1) support
  - platform independent: Win32, UNIX, Linux, Mac, etc.
My First Tcl Script

- Hello world

```tcl
#hello.tcl
set s "hello world!"
puts "* $s *
exit 0
#end of hello.tcl

$ tclsh hello.tcl
* hello world! *0
```
Questions?

Comments?

Discussion?