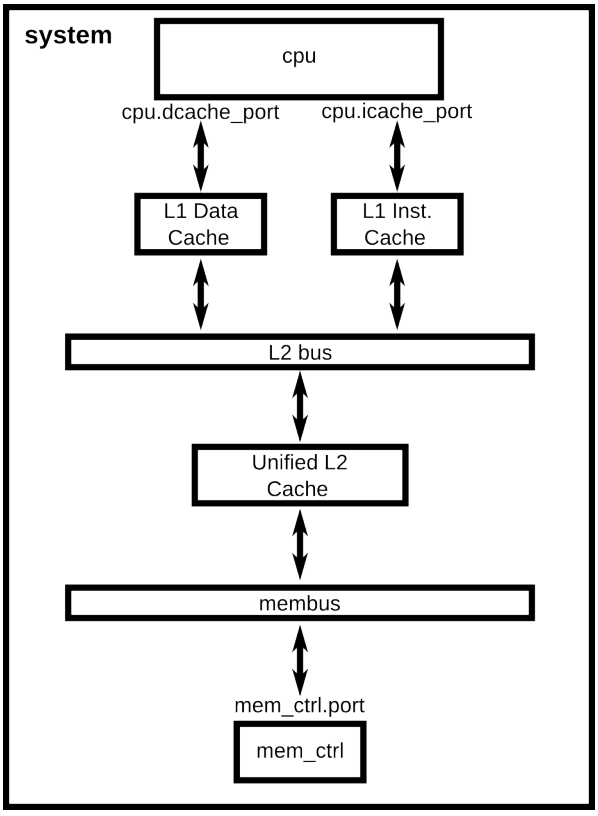
CSE 560M Computer Systems Architecture I

Assignment 4, due Friday, Nov. 8, 2024

In this lab assignment we will explore using the `gem5` simulator to look at cache simulation and program statistics.

1. In this exercise, we will be simulate the following system, which was built during assignment 2:



   Copy your configuration file from assignment 2, `assignment2.py`, into a new file, in this case `assignment4.py`, in the folder `hw4`.

   ```
   cp ../hw2/assignment2.py assignment4.py
   ```

   Also copy your Caches.py file from assignment 2:

   ```
   cp ../hw2/Caches.py Caches.py
   ```

   Now in your `hw4` directory, test your `assignment4.py` configuration file using the command:

```
$GEM5/build/ARM/gem5.opt --outdir="daxpy_arm" assignment4.py --prog="daxpy"
--l1d_size="128kB" --l1d_assoc="8" --clock_freq="0.8GHz"
```

Include a screenshot of the console output in your writeup.

2. Now that we have a working system let's change some parameters and get some measurements! Change your simulation so that the following parameters are implemented and run a simulation for each. Create a table for using the `ARM` ISA of the following parameters and record the value of the parameter for each cache configuration. Pick a parameter (an interesting one that is either listed here or that you've found on your own) and create a graph making it a function of the cache size, use two lines to represent the different clock and association sets. As an answer to this question show the graph and table that you have created.

Clock Speed	L1D$ Association	L1D$ Size
1.0 GHz	1	8 kB
1.0 GHz	1	16 kB
1.0 GHz	1	32 kB
1.0 GHz	1	64 kB
0.8 GHz	2	8 kB
0.8 GHz	2	16 kB
0.8 GHz	2	32 kB
0.8 GHz	2	64 kB

Parameters to record.
Instructions Committed
Average Gap Between Requests
L1D$ Overall Hits
L1D$ Number of replacements
L1D$ Overall Miss Rate
L1I$ Overall Miss Rate
L2 $ Overall Miss Rate
Number of CPU Cycles

3. Pick two configurations from the previous problem and calculate their CPI as a function of the number of instructions and total number of CPU cycles. Show your work! Compare their CPI's. Is there a difference between the CPI of these two configurations? Why or why not?