CSE 560 – Practice Problem Set 7

We are interested in assessing the performance impact of two different data cache organizations on the performance of a single-issue, in-order processor with a 5-stage pipeline that uses 32-bit addresses for memory references. Assume that the CPI with a perfect cache is 2.0, the clock cycle time is 1 ns (i.e., 1 GHz clock rate), and there are 0.2 memory references per instruction (20% of instructions are loads or stores).

The size of the two caches is 64 KB, and both have a block size of 64 bytes. One cache (cache A) is direct mapped and the other (cache B) is two-way set associative.

To accommodate the additional complexity of a set-associative cache, the processor cycle time must be stretched 1.25 times its value with a perfect cache. The direct mapped cache does not impact the processor's clock rate. The cache miss penalty is 75 ns for either cache organization. Assume the hit time for both caches is 1 cycle, the miss rate of the direct-mapped cache is 1.4%, and the miss rate of the set-associative cache is 1.0%.

(a) If the memory is byte-addressable, how many address bits represent the offset within the cache block for cache A? For cache B?

(b) How many blocks fit (total) in cache A? In cache B?

(c) How many address bits are used to select the index for cache A? For cache B?

(d) How many tag bits are required per cache block in cache A? In cache B?

(e) What is the average memory access time (in ns) for cache A? For cache B?

(f) What is the CPI for the machine with cache A? With cache B?

(g) For an application with 10^9 instructions, what is the total execution time for the machine with cache A? With cache B?

(h) Which machine completes the application faster?