CSE 560
Computer Systems Architecture

Exam 1 Review

Logistics

- Date and Time
  - Wednesday, Oct 16, in class, 5:30pm to 6:50pm, starting right at 5:30!

- Location is in-person in Green Hall L0120
  - Read questions carefully (e.g., pipeline diagrams)

Style

- Questions
  - Question 1 will be a collection of short answer things (e.g., true/false, fill in the blank, quick definition)
  - Questions 2 through N will be longer (going more in depth on a particular subject)
- Closed book, closed note, NO partners!
- One-page “crib sheet” is allowed
  - 8.5 x 11 sheet, front and back, whatever you want to include (content-wise)
- Calculator is not allowed (not needed), so show your work

Instruction Set Architecture

- Definition
- Components
  - Machine instructions
  - Programmer-level memory model
  - Operating Modes
- What isn't part of the ISA, e.g.,
  - Pipelined execution
  - Branch predictors
  - Caches

Qualities of a Good ISA

- Programmability
- Implementability
- Compatibility

Specifics of ISAs

- Instruction Format
- Register File
- Main Memory
  - Little endian, big endian
- Addressing Modes
- Conditional Branching
  - Condition Codes
  - Test and Branch
- RISC vs. CISC

Performance

- Metrics
  - Latency
  - Throughput
- Fundamental Equation

$$\frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

  - Calculation of CPI accounting for stalls
- Benchmarks
- Architectural Simulation

Technology

- Moore's Law

- Transistor Properties
  - Implications of scaling
    - Cost
    - Speed
    - Power and Energy
    - Reliability

Pipelining

- 5-stage example pipeline
  - What happens where
  - Data dependencies
  - Hazards
  - Bypassing (forwarding)
- Pipeline diagrams
- Multi-cycle operations
  - Pipelined functional units (e.g., multiplier)

Branch Prediction

- Why?
- How?
  - Classic types
- Where?
  - Esp. in context of 5-stage pipeline
- Performance implications?

Parallel Pipelines

- Superscalar
  - In-order execution
- Scheduling
  - By the compiler
  - Single issue and multiple issue
  - Loop unrolling
- Pipeline diagrams
  - Emphasis on when does the X stage happen

Time for Q&A

- We'll start right at 5:30pm
- Closed book, closed notes, NO partners
- One page "crib sheet" allowed (both sides), it does not have to be handwritten
- Calculator not required
- Read questions carefully (esp. pipeline diagrams)