Project 2b: DSP in Verilog

Design and build a co-processor that interfaces to the Leon that implements an FIR filter. Use memory mapped registers on the AMBA APB bus device 12 to communicate with the co-processor. Your C program (and Modelsim Testbench) will transmit the 16 bit filter coefficients and the 16 bit filter inputs to the co-processor, and receive the 16 bit results computed by the co-processor. Assume that the maximum length of the filter is 163. Verify that your co-processor is working correctly in simulation and in hardware. Measure the MAC/s rate that this system can sustain. Compare this to software DSP in part 2a. Report required that covers both parts a) and b) of this project.

Hints:

1) Create a memory mapped register in the PSel12 space with the following format:
      i. InitRAM
      ii. Convolve
      iii. Load Coefficient
      iv. Load Number of Taps
   b. [18:3] – 16 bit data to be passed to FSM – InitRAM value, coefficients, filter inputs
   c. [31] – Ready bit asserted by FSM indicating status – ready or busy.
2) Use the bubble diagram below as a starting point.

3) Make sure you check to make sure that your peripheral synthesizes cleanly in ISE before attempting to synthesize top.
Graphing Waveforms in Modelsim

To view a signal as an analog wave highlight the signal and right click and select **Properties**... and then select the **Format** tab. The “Height” field is the total height in pixels, set this to something like 256. Then select **Format -> Analog**... and choose either interpolated for a smooth graph or step for the discreet steps. Then, set the offset to half of the range of values, in the case of a 16 bit number, 32768. Then set the scale to the height / number of steps in the signal, in this case 256 / 65536 or .0039. To view two waves overlaid on each other leave the second wave’s height as 17 and add that divided by the scale to the offset.