Lecture 5 – LTC1654 (DAC) and LTC1865L (ADC)

   a. DAC (page 18)
      i. 2 mistakes on page 18 (NOT L and settling times in uSec)
      ii. LTC 1654 datasheet (NOT 1654L)
      iv. RefLo = 0V, RefHi = 3.3V
      v. X/X1/2A = VOut, VOutA = 0 to 3.3V/2
      vi. X/X1/2B
         1. 0V via J6, VOutB = 0 to 3.3V
         2. Open - VoutB undefined (see note on p. 6 "These pins should not be left floating")
         3. I guess we better set X/X1/2B to 0V.
      vii. Switching Characteristics diagram on p. 3/6 (2.7V to 5.5V).
   b. ADC (page 17)
      i. J10 – DC or J9 input to ADC0
      ii. LTC1865L datasheet
      iv. Recommended Operating Conditions and Timing Characteristics (p. 4/8/10)
   c. leon.ucf – Timing Constraints (assume no board delay)
   d. Interface Board Schematic
   e. Complete Schematic of Nu-Horizons SP3-1500 Board
   f. Critical Timing Summary
   g. Timing Diagram

2. Hardware considerations
   a. Register all signal to the outside world – SCK shouldn’t glitch
   b. Synchronizers – all asynchronous inputs to the FPGA need to be synchronized to our Clk
      i. Timing Violation/Metastability
      ii. In this case, SDO is really a synchronous signal.