Lecture 4 - Finite State Machines (FSM) in Verilog

Combinational Logic in Verilog (review)

- Simulation Model – Code executes from top to bottom sequentially whenever an input in the sensitivity list changes.

Sequential Logic in Verilog (review)

- Simulation Model – On the rising edge of Clk, code executes in parallel. Right hand side of the <= takes on the value just prior to the rising edge.

Finite State Machines

- Shown below is a block diagram of a Mealy State Machine
    - Outputs are a function of Inputs and Current State.

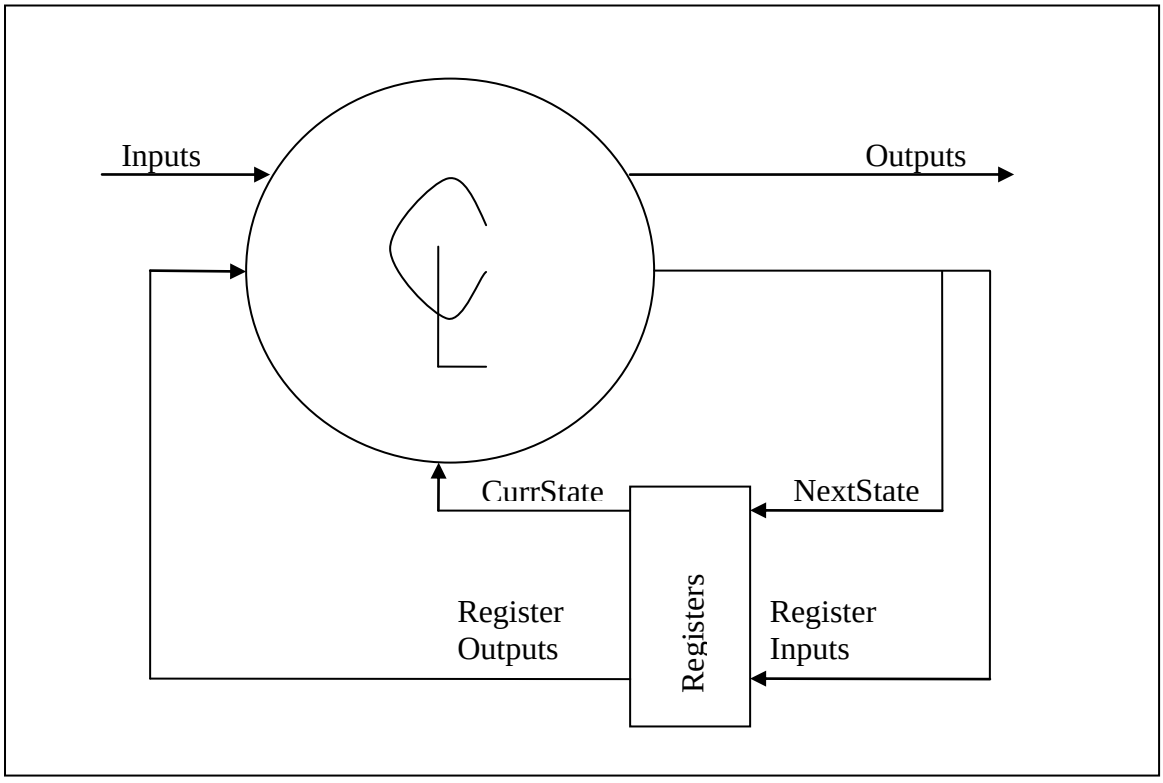
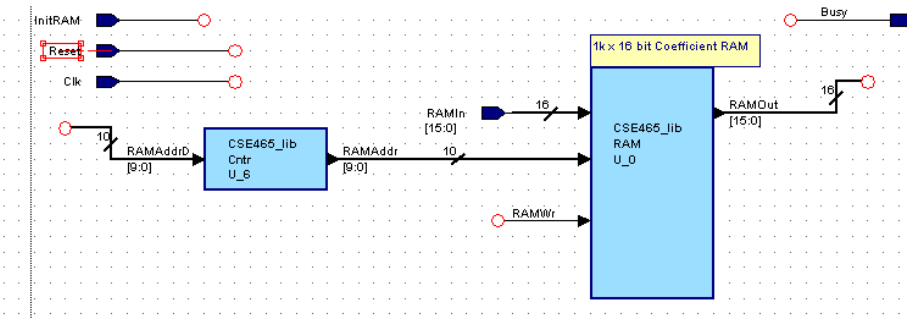
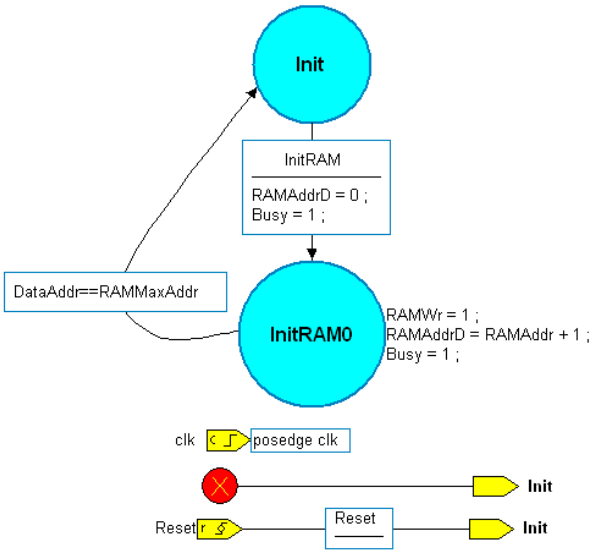


Figure 3: Block Diagram for Mealy Machine

- Describe your FSM with 2 **always** blocks
  - Combinational Logic
  - Registers including State Register.
- For example, consider the following block and bubble diagrams:





Verilog Files (available here)

1. ram.v – Infers a distributed RAM – easier to use than block ram.
2. FSMExample.v – FSM and Structure shown above
3. FSMExample_tb.v – Testbench to drive FSMExample
   a. InitRAM.tb – File that is used as input to the testbench.