CSE 464 – Final Exam

Spring 2007

No books, no notes (except three 8.5” x 11” sheets, handwritten, both sides). Write in the spaces provided. Be neat. Show all work necessary and explain any assumptions. Answers with no work shown that are not obvious will get no credit. Do not use any additional paper for your work. Do not use the back of the sheets for any work you want graded. If you use the back for work, transfer all final work to the front of the exam. The backs will not be graded.

Please circle all final answers. Hunting for answers does not make the grader happy.

The problems are in no particular order. If you are having trouble with a problem, move on and come back later.

Exam Number

NAME

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1. (10 points) Calculate the BER (Bit Error Rate) for a digital transmission system specified as:

- Gaussian noise is the sum of two sources: 5 mV and 20 mV,
- Signal swing is 1 V, \( G_n = \frac{1}{2} \)
- Power supply noise is 25 mV, and
- \( K_n \) (proportional noise coefficient) is 0.2

\[
V_g = \sqrt{5^2 + 20^2} \text{ mV} = 20.62 \text{ mV}
\]

\[
V_m = \frac{1}{2} - 0.2 - 0.015 = 2.75 \text{ mV}
\]

\[
BER = e^{-\frac{1}{2} \left( \frac{2.75}{20.62} \right)^2}
\]

\[
= 2.38 \times 10^{-39}
\]
2. (10 points) Given a logic element (assume an inverter if you want, but it makes no difference what the logic function actually is) that has an input impedance of 1 MΩ (10^6 Ω), an output impedance of 30 Ω, an output voltage swing of 0 V to 1 V (for a rising signal, it would be 1 V to 0 V for a falling signal), V_{IH}=0.8V and V_{IL}=0.2 V, how would you propose to terminate signals that travel across a 50 Ω transmission line between such devices? Give your reasoning and any assumptions that you make.

Diagram:

- Want 2.8 V or rising edge
- IMN = F or open circuit compared to 50 Ω line (voltage changes)
- Terminate source or to reflections
  a) for and doesn't change for 1st case
  b) we see ±V at input to line

Terminate with 20 or more like 15 V goes in, 1 V comes out
3. (15 points) A five foot long transmission line is measured with a capacitance meter and found to have 270 pF of capacitance. The dielectric material has a relative dielectric constant of 4. Find:

   a. the one-way delay of this line (from source to end),
   b. the inductance of the line,
   c. and the characteristic impedance of the line.

\[
\text{a) } V = \frac{1 \text{ ft/s}}{\sqrt{\epsilon_r}} = \frac{1 \text{ ft/s}}{2.3} \\
\text{for 5 ft } \rightarrow 10 \times 5 \text{ delay} \\
\text{b) } V = \sqrt{1 \frac{\text{ft}}{\text{C} \cdot \text{L}}} \\
L = \frac{1}{CV^2} \\
= \frac{1}{3 \times 10^{12} \cdot (\frac{1}{2.3})} = \frac{1}{370 \times 10^{-12}} \\
= 370 \text{ nH} \ \approx 169 \mu\text{H} \\
\text{c) } Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{370 \times 10^{-9}}{270 \times 10^{-12}}} \approx 24,652}
\]
4. (15 points) A digital system is being designed for use in a wireless mouse for a PC. It’s not important to have really good reliability in this application, but a MTBF of at least one (1) hour should be achieved. Events subject to metastability occur at up to 100 Hz, the clock for the circuit runs at 10 MHz and it uses flip-flops with an aperture time of 250 ps and a $\tau_e$ of 10 ps. What waiting time ($t_w$) would you recommend for your synchronizer that you will most certainly need for this system?

$$MTBF = 3600 \text{ sec} = \frac{C}{100 \text{ Hz} \cdot 10 \text{ MHz} \cdot 250 \text{ ps}}$$

$$t_w = 68 \text{ ps}$$
5. (10 points) For the following circuit:
   a. the clock-to-output delay for each flip-flop ranges from 2 ns to 4 ns,
   b. The setup time for each flip-flop is 2 ns,
   c. The hold time for each flip-flop is 0 ns,
   d. The delay for each logic gate ranges from 1 ns to 3 ns (regardless of the type of gate)
   e. The maximum clock skew is 500 ps.

How fast could you clock this circuit and ensure correct operation? 
When must A be stable to ensure correct operation?

\[ \tau_{C} = \tau_{C0} + 2\tau_{C1} + \tau_{S} + \tau_{L} \]

\[ = 4 + 6 + 2 + 1.5 = 13.5 \text{ ns or } 80 \text{ MHz} \]

A stable:
before clock: \[ \tau_{S} + 2\tau_{C1} + \tau_{L} = 2 + 6 + 1.5 = 8.5 \text{ ns} \]
after clock: \[ \frac{\tau_{L}}{2} + \tau_{C1} + \tau_{L} = 0 - 2 + 1.5 = -1.5 \text{ ns} \]
6. (10 points) An IC has a steady state current of 10 A. Maximum allowed ΔV_{dd} is 0.05 V (5% of the 1 V which I assume V_{dd} to be). In order to simplify power supply bypassing, the IC has been designed to have constant I_{dd} while operating (that is, it’s zero or 10 A). The second stage bypass capacitors have parasitic inductance (L2) of 200 pH. What value is required for C1?

\[ C_1 > L_2 \left( \frac{\Delta I}{\Delta V} \right)^2 \]

\[ = 100 \times 10^{-12} \left( \frac{10}{0.05} \right)^2 \]

\[ = 8 \text{ mF} \]
7. (15 points) Devise a circuit, consisting of only resistors, that would allow you to connect a 50 \( \Omega \) coax cable to a 75 \( \Omega \) coax cable with no reflections in either direction.

\[
50 = \frac{R_1}{\left(R_2 + 25\right)} \quad \quad \quad \quad \quad 75 = R_2 + \left(\frac{R_1}{50}\right)
\]

\[
= \frac{R_1 R_2 + 75 R_1}{R_1 + R_2 + 25}
\]

\[
= R_2 + \frac{SO R_1}{SO + R_1}
\]

\[
\left(75 - R_2\right)\left(R_1 + 50\right) = 50 R_1
\]

\[
50 R_1 + 50 R_2 + 3750 = R_1 R_2 + 75 R_1
\]

\[
3750 = R_1 R_2 - 15 R_1 + 50 R_2
\]

\[
2750 = R_1 R_2 + 25 R_1 - 50 R_2
\]

\[
\text{Subtract}
\]

\[
0 = 50 R_1 - 100 R_2 \quad \Rightarrow \quad R_1 = 2 R_2
\]

\[
50 \cdot 3750 = 2 R_2^2 + 50 R_2 - 50 R_2
\]

\[
R_2 = \sqrt{\frac{3750}{2}} = 43.3 \Omega
\]

\[
R_1 = 86.6 \Omega
\]
8. (15 points) Short answers.

a. If I gave you two black boxes, one with a 50 Ω resistor between the terminals and the other with a 1 foot long transmission line (Z₀ = 50 Ω, v = 1 ft/2ns) terminated with a 50 Ω resistor between the terminals, can you tell which is which? If so, how? If not, why?

A TDR would show the same pulse for both so no I cannot tell.

b. If you were building a printed circuit board with many high speed signals, packed closely together, and all traces were several inches long, would you rather place these traces on the top, bottom or inside layers of the PCB or does it not matter to you. You should assume every signal layer is separated from adjacent signal layers with a power plane.

Inside layers have lower delay so no cross talk (and propagation delay is less /100)

c. If I give you a synchronous circuit that was designed to operate at some maximum clock frequency that is not exceeded, do you have to consider metastability issues if there are no external inputs to this circuit?

No (assuming it was designed properly)
9. (15 points) For the following statement, think about how each of the three listed items will be affected. That is, will they increase, decrease, or stay the same? Justify your answers, but short answers are fine. No long equations or number crunching is required (i.e. magnitudes are not important if not obvious). State any other assumptions you feel you need to make.

If a transition time of an aggressor signal is changed from 1 ns to 0.5 ns on a pair of 6 inch long wires,

a. How will the signal return crosstalk (also known as coupling) change?
   
   * Doubles as we are inversely proportional to rise time

b. How will the reverse crosstalk be affected?
   
   Since \( \eta < \frac{2L}{V} \)
   
   No change \( \beta_{RX} \) is negligible

c. How will the forward crosstalk be affected?
   
   Also doubles (and causes the return signal)
   
   \[ \beta_{FX} = \frac{V_{RI}}{2} \]
   
   \[ \beta_{FY} = \frac{V_{RI} + \beta_{RX}}{2} \]
   
   \[ \beta_{FY} = \frac{V_{RI} - \beta_{RX}}{2} \]