CSE 464 – Exam 1

Spring 2007

No books, no notes (except one 8.5” x 11” sheet, handwritten, both sides). Write in the spaces provided. Be neat. Show all work necessary and explain any assumptions. Answers with no work shown that are not obvious will get no credit. Do not use any additional paper for your work. Do not use the back of the sheets for any work you want graded. If you use the back for work, transfer all final work to the front of the exam. The backs will not be graded.

Please circle all final answers. Hunting for answers does not make the grader happy.

The problems are in no particular order. If you are having trouble with a problem, move on and come back later.

Exam Number __________________________

NAME ______________________________

<table>
<thead>
<tr>
<th>Problem</th>
<th>Possible</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>110</td>
<td></td>
</tr>
</tbody>
</table>
1. (10 points) In a homework problem we looked at a clock distribution IC (MPC9448). This device has multiple outputs based on a single clock. As you are probably already aware (and will certainly be in a few weeks) we desire to reduce clock skew in our systems. This device has a maximum skew of 150 ps per output. If we wish to keep the skew between any clock received from this device to less than 200 ps, what is the difference in PC board trace lengths we could tolerate so that all devices see the clock within 200 ps of each other? Assume your PCB uses FR4 material with $\varepsilon_r = 4$. Please report your answer in inches.

$$\text{Line is } \frac{1 \text{ ft}}{\text{ns}}$$

We have 50 ps length and speed $\frac{1 \text{ ft}}{\text{ns}}$.

So, $50 \text{ ps} \cdot \frac{1 \text{ ft}}{2 \text{ ns}} = 0.025 \text{ ft} = 1.2''$.
2. (15 points) A signal conductor has a propagation velocity of 1 ft/2 ns and a characteristic impedance of 50 Ω. What is the maximum capacitance per foot that can be added by distributed loads and still keep the loaded characteristic impedance at least 20 Ω (≥ 20 Ω)?

\[ C = \frac{1}{50} \left( \frac{\text{ft}}{\text{ns}} \right) = 0.04 \text{ pf/ft} = 40 \text{ pF/ft} \]

\[ Z_0' = Z_0 \sqrt{\frac{1}{1 + \frac{C_{\text{add}}}{C}}} = 50 \sqrt{1 + \frac{C_{\text{add}}}{C}} \]

\[ 20 = 50 \sqrt{\frac{\frac{\omega C}{\eta_0}}{\eta_0 + C_{\text{add}}}} \]

\[ .16 \left( \frac{\omega_0 + C_{\text{add}}}{\eta_0} \right) = 40 \text{ pF} \]

\[ C_{\text{add}} = 210 \text{ pF} \]
3. (20 points) Assuming an output driver with a 3.3 V output swing and a series resistance of 50Ω drives a 50 Ω line. The output can switch from 0 to 3.3 V in 5 ns. If these are used to form a 16-bit data bus, and they all share a common ground return with an inductance of 10 nH, how much signal return crosstalk do you expect? Briefly comment on if you feel this is acceptable or not, and why.

\[
\text{For one line, assume } V_L \text{ (return voltage) is small.}
\]

\[
I = \frac{3.3V}{100\Omega} = \frac{3.3V}{100} = 3.3V = 6.6 \times 10^{-6} A/s
\]

\[
V_L = L \frac{dI}{dt} = 66mV
\]

\[
\text{For 16 lines simultaneously,}\]
\[
V_{L_{\text{rms}}} = 1.056V
\]

This is about 32% of the total voltage swing and probably causes the noise margin.
4. (15 pts) For the following circuit, how long do you have to wait (in ns) until the voltage $V_1$ is within 0.01% of its final value? What is that final value?

\[ Error = \left( \frac{1}{k_T} \right)^{N+1} \]

\[ k_T = \frac{400}{600} \quad k_{rs} = -\frac{90}{110} \]

\[ Error = \left( 0.666 \right)^{N+1} = 0.001 \]

\[ N+1 = 15.2 \]

So \( N = 15 \)

\[ \left( \frac{2N+1}{4} \right)^{1/2} \leq \alpha \leq \left( 2N+3 \right)^{1/2} \]

So \( 31.15 \)

The final voltage is \( 2 \cdot \frac{500}{510} = 1.96 \text{ V} \).
5. (20 pts) A system is designed with series-terminated drivers and a bidirectional bus that (foolishly) couples the transmit and receive lines as shown, below. I want to determine the characteristic impedances of the lines by driving one line while the other is “quiet” and seeing the induced voltages. What you see on the diagram are my results. Now I ask you to do the math and determine the characteristic impedances $R_1$ and $R_2$.

\[ V_2 = V_1 \frac{R_1}{R_1 + R_2} \Rightarrow \frac{1}{\frac{11}{11}} = \frac{R_1}{R_1 + R_2} \]

so

\[ R_2 = 10R_1 \]

\[ \left( \frac{R_1 + R_2}{2} \right) \parallel R_1 = \frac{12}{21} \]

\[ \frac{11R_1}{2} \parallel \frac{11R_1}{2} = \frac{11R_1}{2} = \frac{12}{21} \]

\[ \frac{11R_1}{2} \parallel \frac{11R_1}{2} = \frac{11R_1}{2} \]

\[ R_1 = \left( \frac{50}{2} + \frac{11}{2} R_1 \right) \frac{12}{21}, \frac{12}{11} \]

\[ R_1 = \frac{21}{2} \frac{11}{21} \left( 50 + \frac{11}{2} R_1 \right) \]

\[ 2 \frac{21}{2} + \frac{11}{2} R_1 \]

\[ R_1 = 22.6 \Omega \]

\[ \Rightarrow R = 72.6 \Omega \]
6. (15 pts) For the following circuit

a. What is the maximum $R_s$ that would allow a voltage at the receiving end of at least 0.85V?

b. Is there a minimum $R_s$ that would guarantee the same 0.85V at the receiving end and why or why not? (You do not have to calculate the minimum $R_s$ if there is one.)

\[ V_0 \left| \tau = 0 \right. = \frac{Z_0}{Z_0 + R_s} \]

So

\[ V \left| \tau = 2\lambda_s = \frac{2Z_0}{Z_0 + R_s} \]

\[ > 0.85V \]

\[ \frac{2Z_0}{1.85} > 0.85 \frac{Z_0}{1.85} + 1.85R_s \]

\[ R_s < \frac{101.5}{1.85} \]

This is a minimum. But if $R_s < \frac{Z_0}{2}$

\[ V < \frac{2Z_0}{Z_0 + 2R_s} \]

Must keep $V$ up enough
7. (15 pts) Plot $V_I$ for the following circuit for $t < 5$ ns

$V_0 = \frac{100}{55} = 1.82 \text{ V}$

$V_{L_{2.5}} = 1.91 \text{ V} \left(1 - e^{-\frac{t}{RC}}\right)$

$\tau = RC = 25 \text{ ns}$, so $F = 2 \times 10^{10} \text{ ps}$

\[\text{Ans.} 4 \text{ ns}\]