Homework 3, Due February 16

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text and class notes/discussion. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in this course. It has no effect on your grade.

1. For all of the following transmission lines, \( V_s \) is a one volt step at \( t=0 \), \( R_s \) and \( R_t \) are the source and load termination resistors, and \( Z_0=100 \, \Omega \). For each configuration, find \( V_t \) (receiving end voltage) for \( t \leq 7(l/v) \). Draw the waveforms for \( V_t \). If any configurations have the same waveform, you can draw the waveform once and then simply indicate which configurations produce that waveform. (Feel free to use a simulator to check your results, but draw them by hand; do not give me the output from a simulator.)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>( R_s ) (( \Omega ))</th>
<th>( R_t ) (( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100</td>
<td>( 10^{12} )</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>100</td>
</tr>
<tr>
<td>C</td>
<td>90</td>
<td>( 10^{12} )</td>
</tr>
<tr>
<td>D</td>
<td>0</td>
<td>90</td>
</tr>
<tr>
<td>E</td>
<td>( 100/1.1 )</td>
<td>( 10^{12} )</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>110</td>
</tr>
<tr>
<td>G</td>
<td>10</td>
<td>110</td>
</tr>
<tr>
<td>H</td>
<td>( 100/1.1 )</td>
<td>1000</td>
</tr>
<tr>
<td>I</td>
<td>( 100/0.9 )</td>
<td>( 10^{12} )</td>
</tr>
<tr>
<td>J</td>
<td>0</td>
<td>( 100/0.9 )</td>
</tr>
</tbody>
</table>

2. Sketch the waveform at the input and output of a transmission line for a series terminated transmission line with \( R_s=Z_0, R_t=\infty \), and a source voltage generating a 1V pulse of width equal to \( \frac{1}{2} \) the transmission line one-way delay: \( 1/(2v) \).
3. Repeat problem 2 for a square-wave voltage source which alternates between 0V and 1V with the time at each level equal to the round-trip delay $2(1/v)$ of the transmission line. You should be surprised at the waveforms (at least at sending end) for this problem.

4. A transmission line with $Z_0$ of 100 Ω ± 10% is driven with a 0V to 1V source with output resistance ($R_s$) of 10 Ω. The receiving end has a resistance to ground of $R_t$ ± 10%. What is the maximum and minimum allowed nominal value of $R_t$ in order for the receiving end voltage to remain at or above 0.8V after the incident wave from the 0V to 1V source transition? Put another way, 0.2V of noise (reduction in $V_{\text{high}}$) is to be allowed. Note that for one case (max or min resistance) the initial wave will be the limiting condition, and for the other case the first reflected wave (after three times the one-way delay) will be the limiting condition.

5. Use HSPICE to simulate a simple transmission-line circuit. A link to a sample file is next to this homework assignment on the website. Confirm the resistor values found in problem 4 for steady state values. Note that the capacitance at the receiving end produces spikes in the waveform that may give invalid levels for short intervals. This is one disadvantage of terminating at the receiving end when capacitance to ground is present at the receiver (it always is, capacitance is part of the receiver input). The spikes would increase in magnitude if $C_t$ was increased or the rise/fall time was decreased. Increasing rise/fall time would decrease the amplitude of the spikes.

6. A Design Problem: You have been assigned the task of designing an interconnection from an oscillator ($V_{\text{dd1}}$=3.3V) to a clock driver ($V_{\text{dd2}}$=2.5V).

- The oscillator operates from a $V_{\text{dd}}$ of 3.3V ± 5% and can be modeled as a voltage source of 0V (L), or $V_{\text{dd}}$ (H), both in series with a resistor with value 5 to 15 Ω.
- The clock driver input is high impedance with $V_{i_{\text{L,max}}}$=0.6V and $V_{i_{\text{H,min}}}$=1.8V.
- The max input voltage at the clock driver input is $V_{\text{dd2}}$ (2.5V). Hence, it is not allowed to connect the oscillator output directly to the clock driver input since this max input voltage will be exceeded. (This limit on input voltage comes from protection diodes from input to $V_{\text{dd}}$ in the clock driver that prevent damage to the device due to static electricity discharges.)
- The distance between the two circuits is 1 foot
- A 50 Ω ± 10% transmission line is available with 2ns/ft propagation delay. You may ignore resistance of this transmission line and treat it as lossless.
- You may use any resistors (ideal, no tolerance) that you may need.
- The clock signal is 500Mhz square wave with 500ps transitions.

It is important to have good signal integrity for this connection since it’s key to the entire system. Design the interconnect including any termination resistors required and give the worst case waveforms at the receiver input. In keeping with this being a real design problem, it may not be completely debugged yet. It may be impossible to solve with given conditions.