

**Spring Semester 2021**

**CSE463M-563M: Digital Integrated Circuit Design and Architecture**

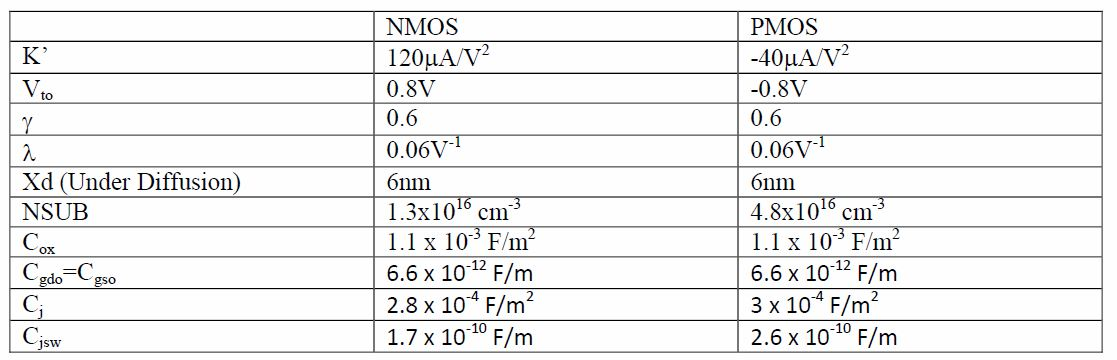
**Homework #3**

**Reminder - Cadence wiki tutorial is located here:**

[**https://eda.engineering.wustl.edu/wiki/index.php/Cadence**](https://eda.engineering.wustl.edu/wiki/index.php/Cadence)

**1) Inverter design problem (including layout) - 80 points**

**Design a CMOS inverter with the following specifications: device threshold of Vth = 3V, rise time trise < 2ns and fall time tfall < 2ns if the load capacitance is 100fF. Also VDD = 5V. Here is transistor data for AMI Semiconductor 0.5 micron process:**

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**Present the following for your homework:**

**1.1) Show all hand calculations that you used to get the aspect ratios (W/L) of all transistors. In addition calculate propagation delay times PHL and PLH of the inverter.**

**1.2) Draw the schematic of the inverter in Cadence. Print the schematic.**

**1.3) Simulate the DC and transient behavior of the inverter schematic. Make any adjustments on the circuit in order to meet the above specifications. Plot the DC and transient characteristics. Show that your design meets requirements for Vth, trise and tfall.**

**1.4) Draw the layout of this inverter. Try to make the layout as small as possible. Measure the size of the layout and use the ruler in layout to show the dimensions.**

**1.5) Run a DRC, extract the layout and LVS the design. Cut and Paste the messages generated in the CIW (the main Cadence window) when the DRC is executed. Print the LVS result – make sure it has successfully passed LVS.**

**1.6) Simulate the inverter extracted view. Again, the online tutorial explains how to simulate extracted view of the inverter. Plot the DC and transient characteristics of the inverter. If there are discrepancies (Vth, trise and tfall) between the schematic and extracted simulations, explain why there are differences between the two simulations? Comment on both DC and transient simulations.**

**2) (80 points)**

**Create a ring oscillator by connecting 11 inverters in a loop. Use your inverter design from the Problem 1 as the starting point. Simulate the ring oscillator in Cadence Spice. Create the layout of the ring oscillator, run a DRC and LVS. Simulate the extracted view of the ring oscillator. Note: If you do not see any transient behavior at the output, you should set up output of the first inverter to be initially equal to 3V.**