Digital IC Design and Architecture

Third Edition

CMOS
Digital Integrated
Circuits
Analysis and Design

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Yusuf Leblebici
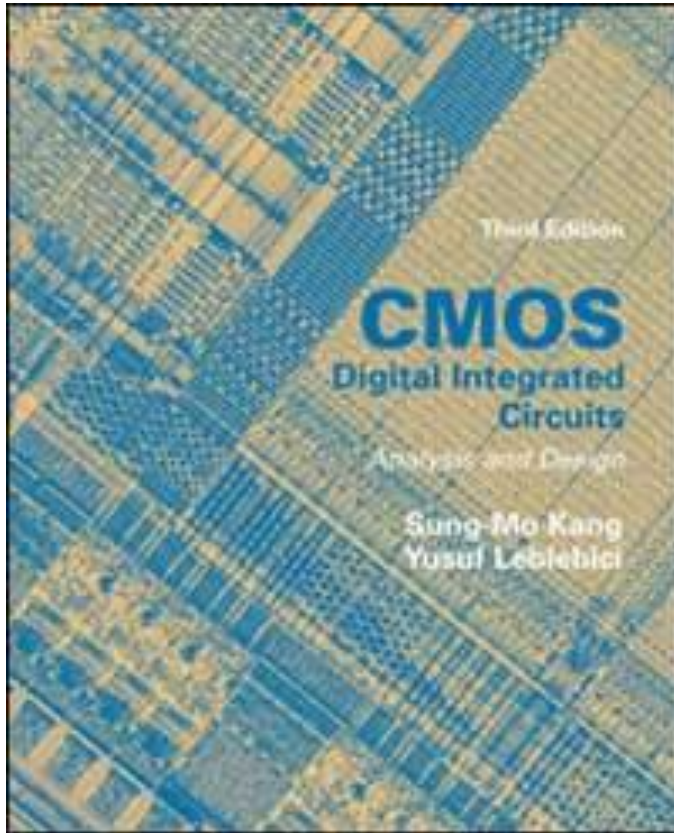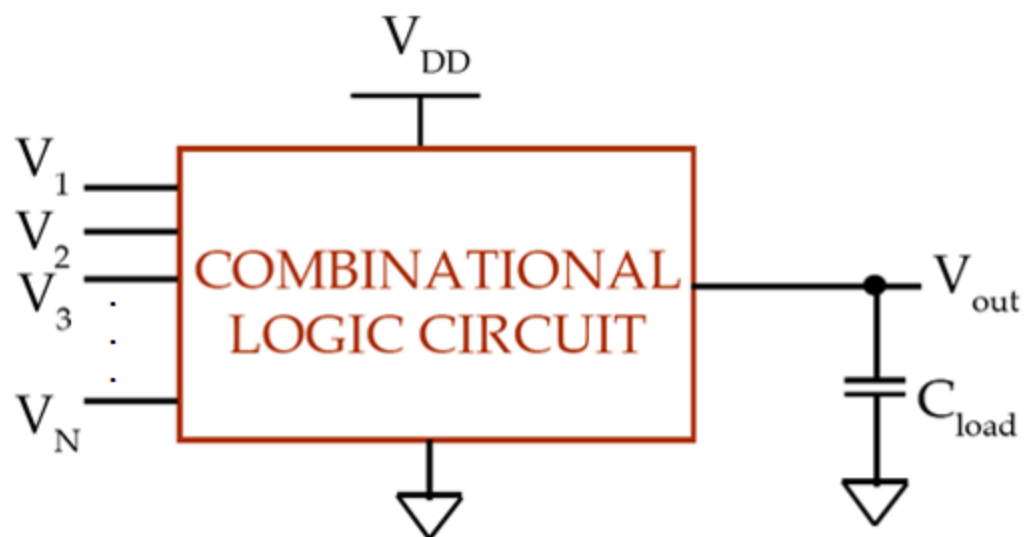
Combinational Logic and Circuits

Static CMOS Circuit

At every point in time (except during the switching transients) each **gate output is connected to either V_{DD} or V_{ss}** via a low-resistive path.
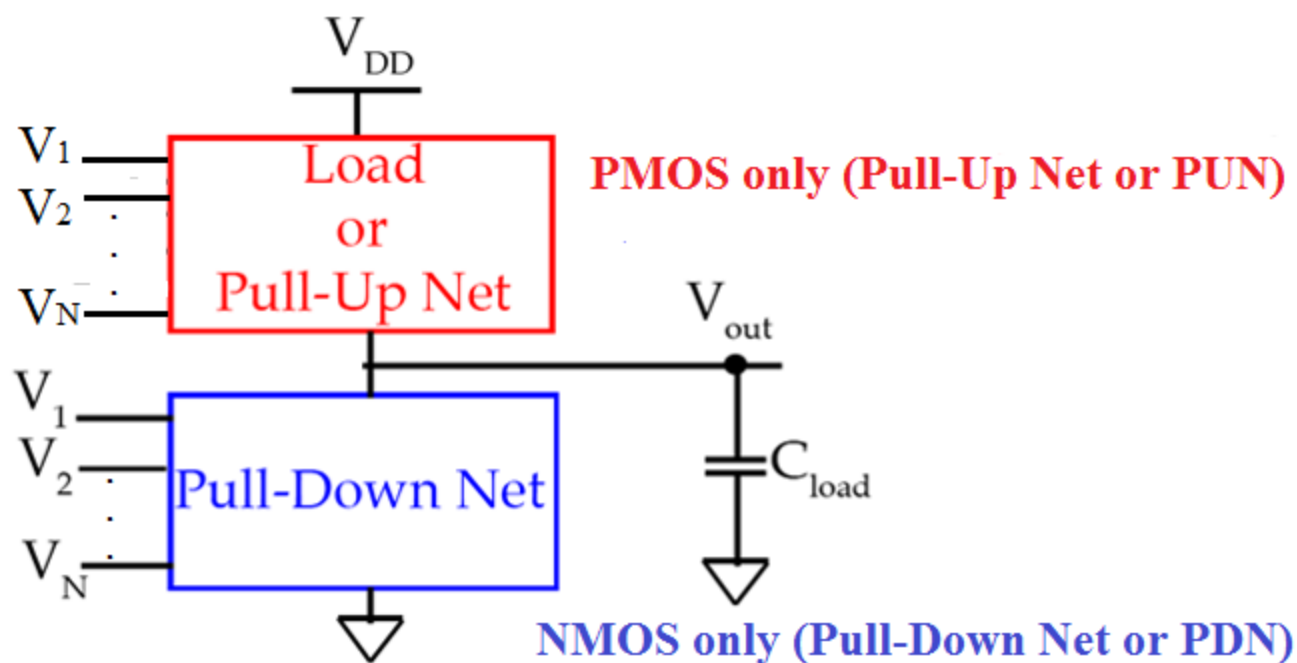
The outputs of the gates **assume at all times the value of the Boolean function**, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

This is in contrast to the **dynamic** circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.
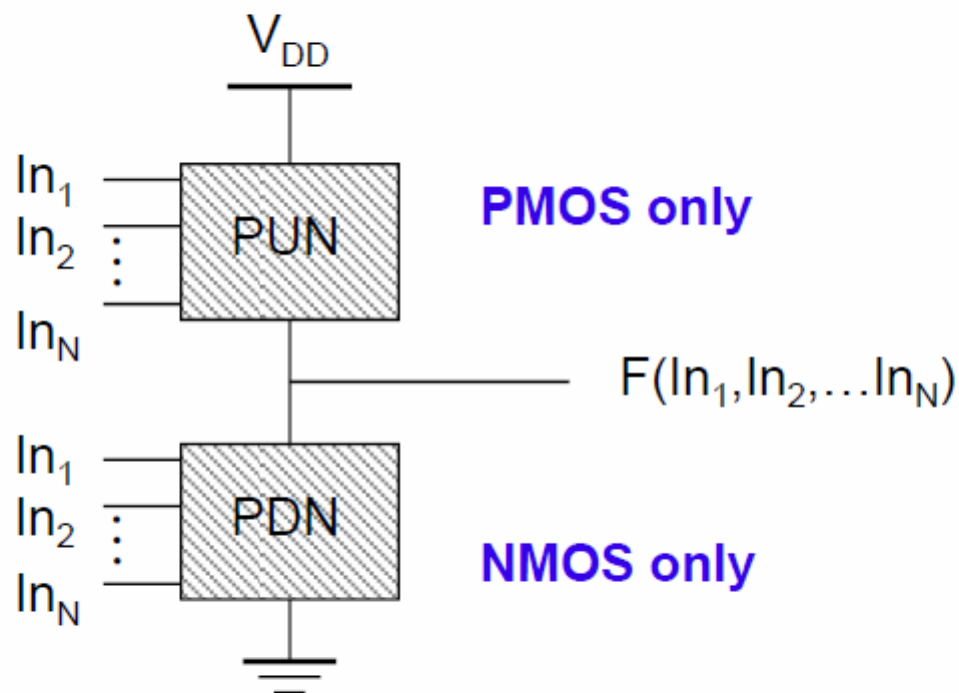
V_{DD}

V_1
V_2
V_3
.
.
.
V_N

COMBINATIONAL
LOGIC CIRCUIT

V_{out}

C_{load}

V_{out} is Boolean
function of inputs ,
V_1, V_2, V_3, ..., V_N.

"1" => V_{DD}
"0" => 0

V_{DD}

V_1
V_2
.
.
.
V_N

Load
or
Pull-Up Net

PMOS only (Pull-Up Net or PUN)

V_{out}

V_1
V_2
.
.
.
V_N

Pull-Down Net

C_{load}

NMOS only (Pull-Down Net or PDN)

Static Complementary CMOS

V_{DD}

In_1
In_2 ⋮
In_N

PUN

PMOS only

$F(In_1, In_2, \ldots In_N)$
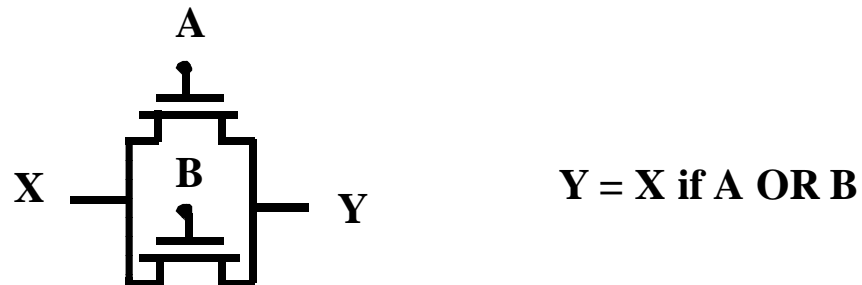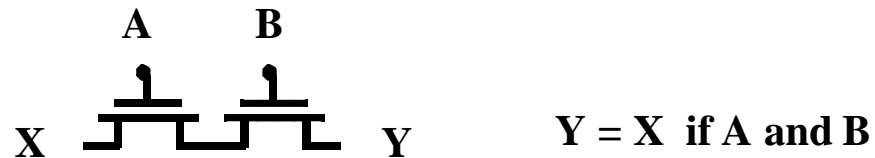
In_1
In_2 ⋮
In_N

PDN

NMOS only

- PUN and PDN are **dual** logic networks
- PUN and PDN functions are **complementary**

NMOS Transistors
in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

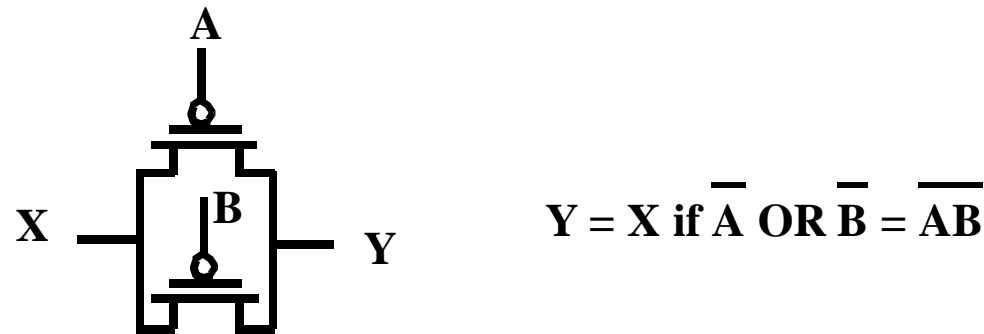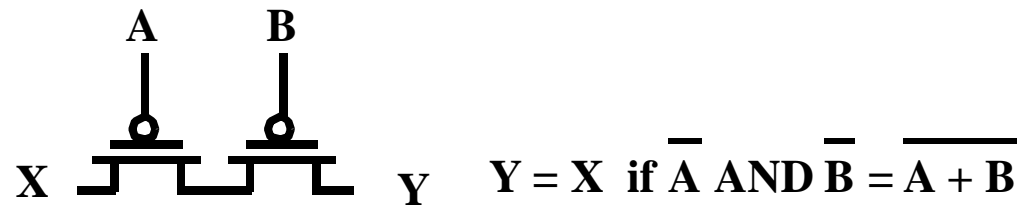**NMOS switch closes when switch control input is high**

$$Y = X \text{ if A and B}$$

$$Y = X \text{ if A OR B}$$

NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors
in Series/Parallel Connection
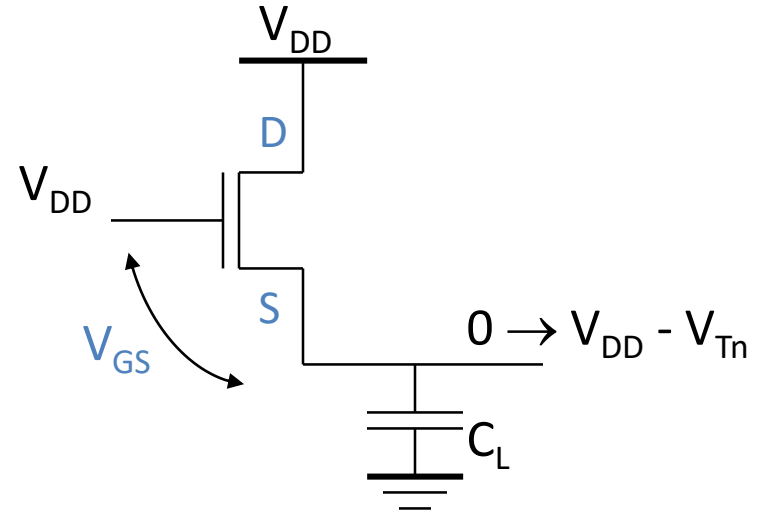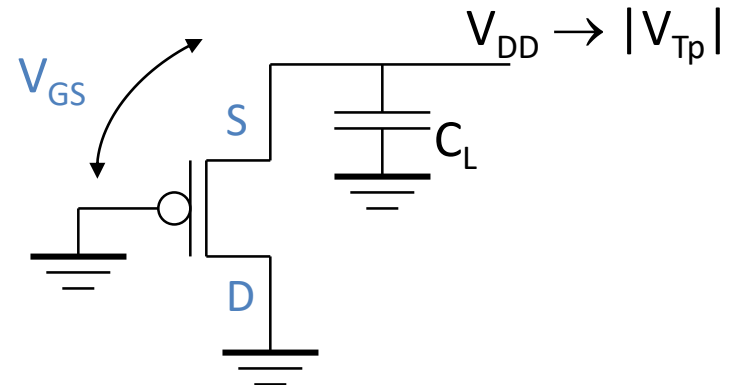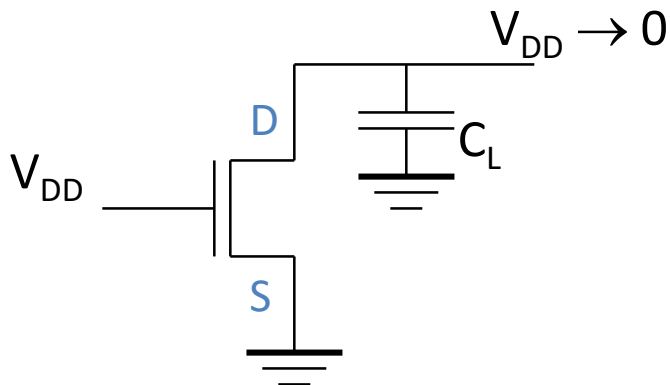**PMOS switch closes when switch control input is low**

$$Y = X \text{ if } \overline{A} \text{ AND } \overline{B} = \overline{A + B}$$

$$Y = X \text{ if } \overline{A} \text{ OR } \overline{B} = \overline{AB}$$

PMOS Transistors pass a "strong" 1 but a "weak" 0

Threshold Drops

PUN – Pull Up Network

$$0 \rightarrow V_{DD}$$

V_{GS}

$$0 \rightarrow V_{DD} - V_{Tn}$$
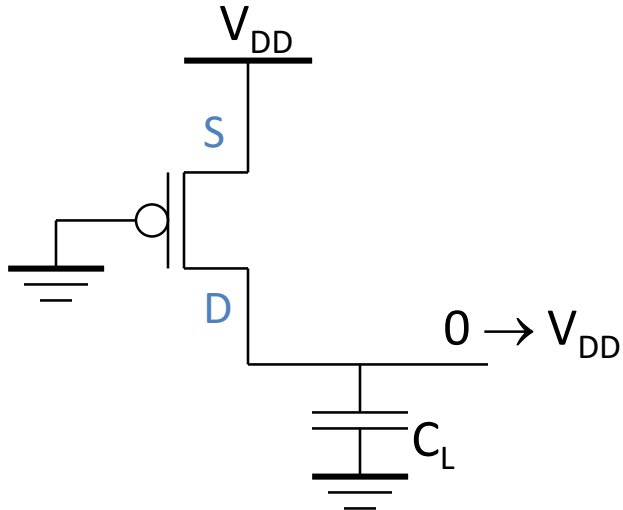
PDN – Pull Down Network

$$V_{DD} \rightarrow 0$$

V_{GS}
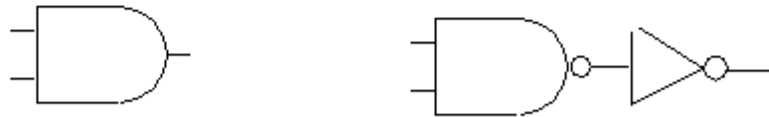
$$V_{DD} \rightarrow |V_{Tp}|$$

Complementary CMOS Logic Style

- **PUP is the <u>DUAL</u> of PDN**

  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

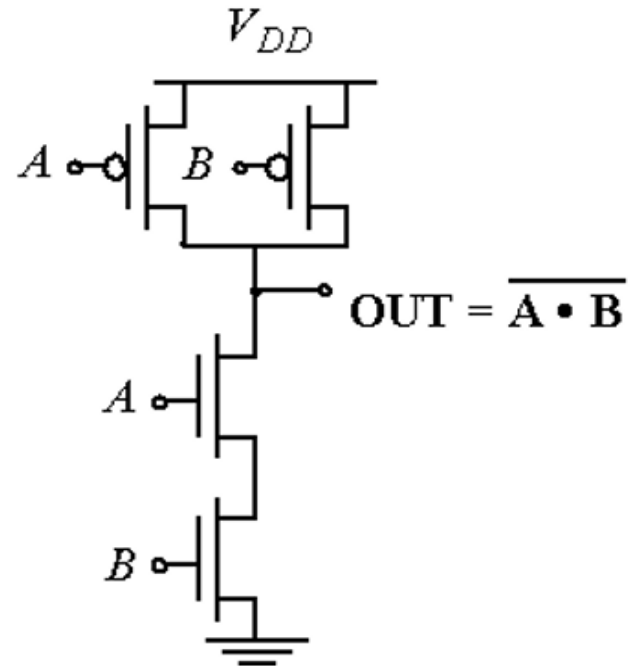- **The complementary gate is inverting**

AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

$$OUT = \overline{A \cdot B}$$

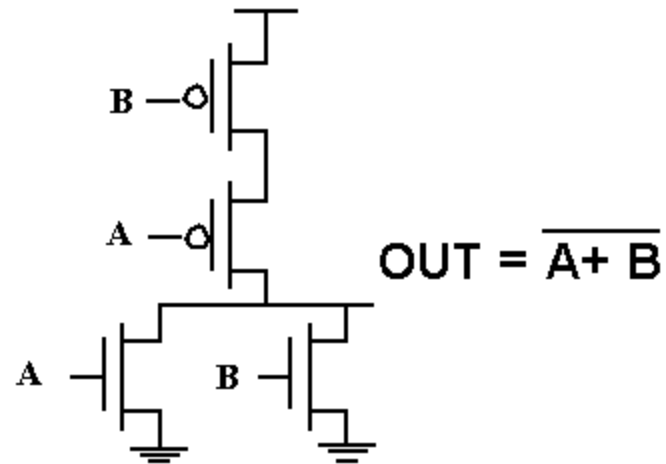**PDN: G = A B** $\Rightarrow$ **Conduction to GND**

PUN: F= $\overline{A}$ + $\overline{B}$ = $\overline{AB}$ $\Rightarrow$ **Conduction to V_{DD}**

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$
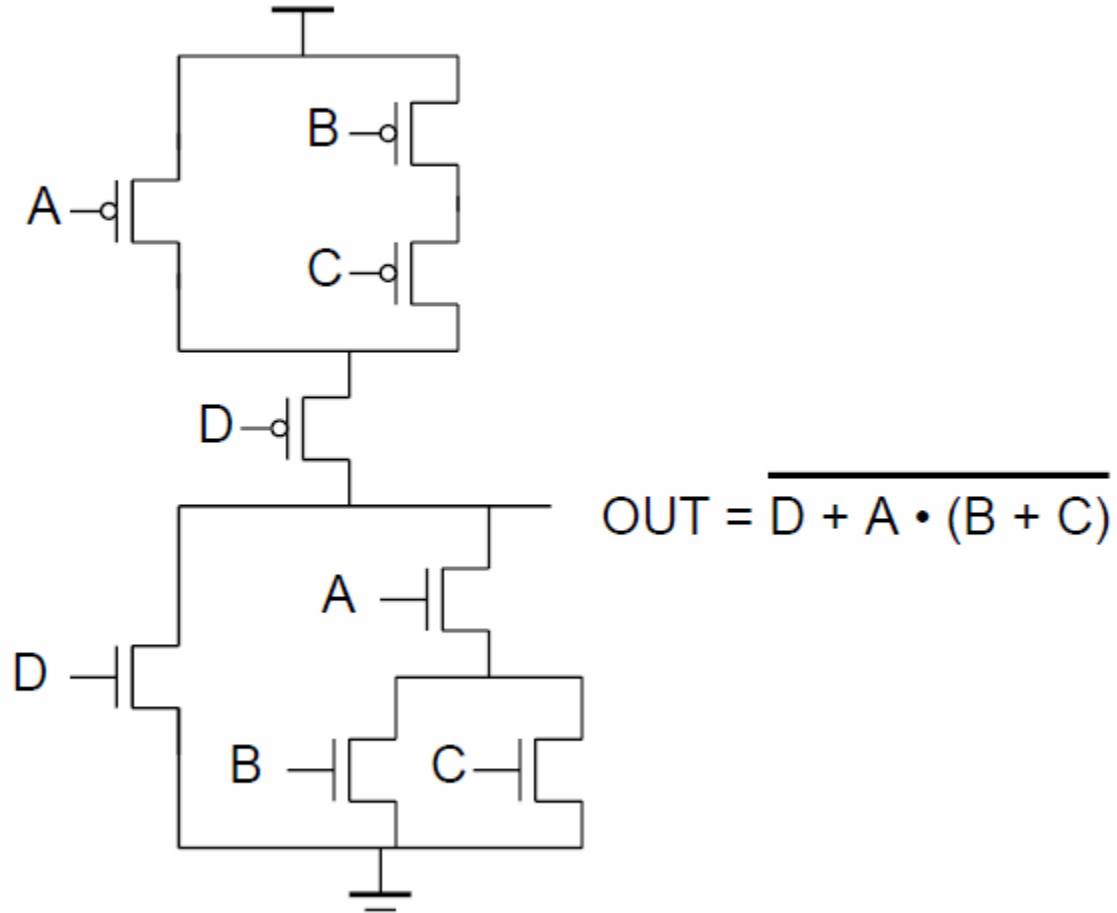
Example Gate: NOR

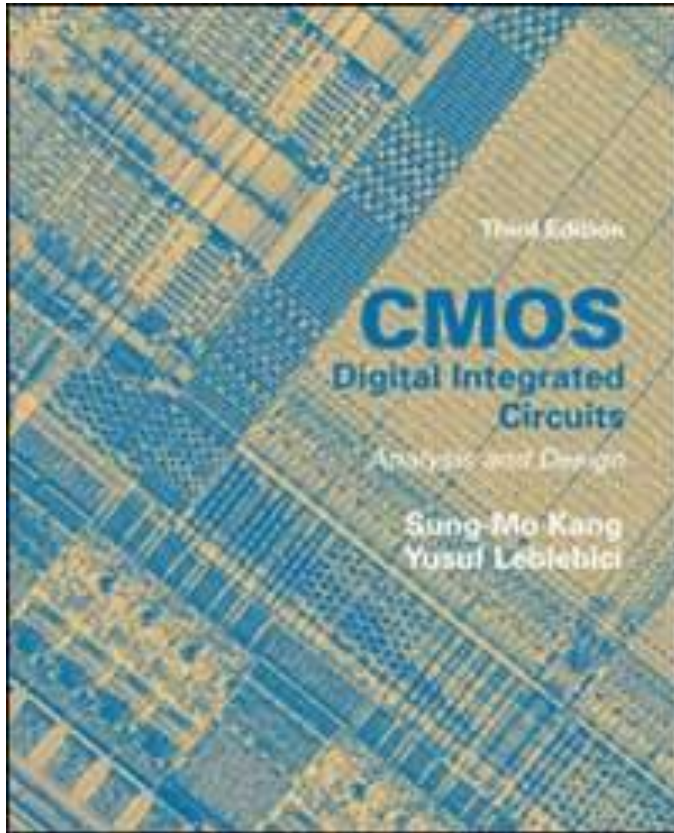| A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

B —○|

A —○|

$OUT = \overline{A + B}$

A

B

Complex CMOS Gate

$$OUT = \overline{D + A \cdot (B + C)}$$

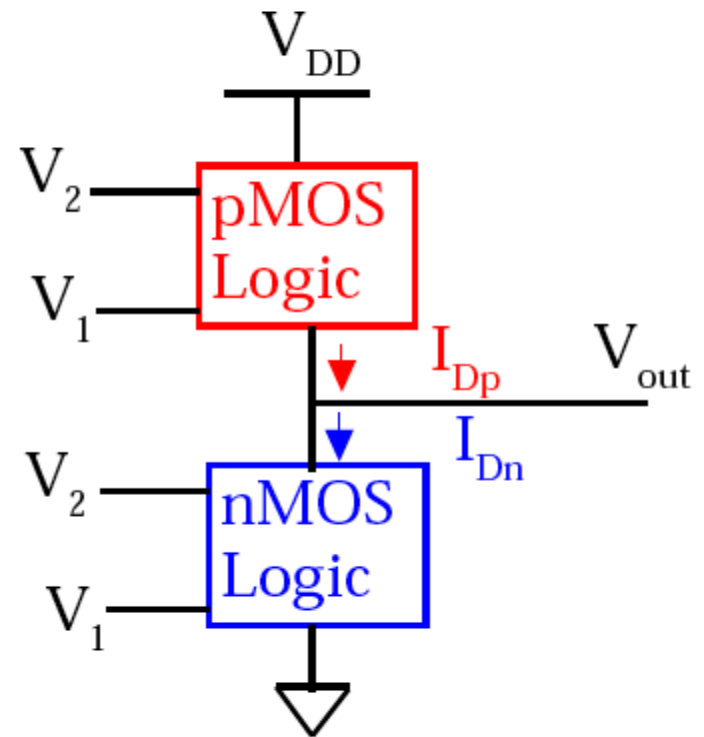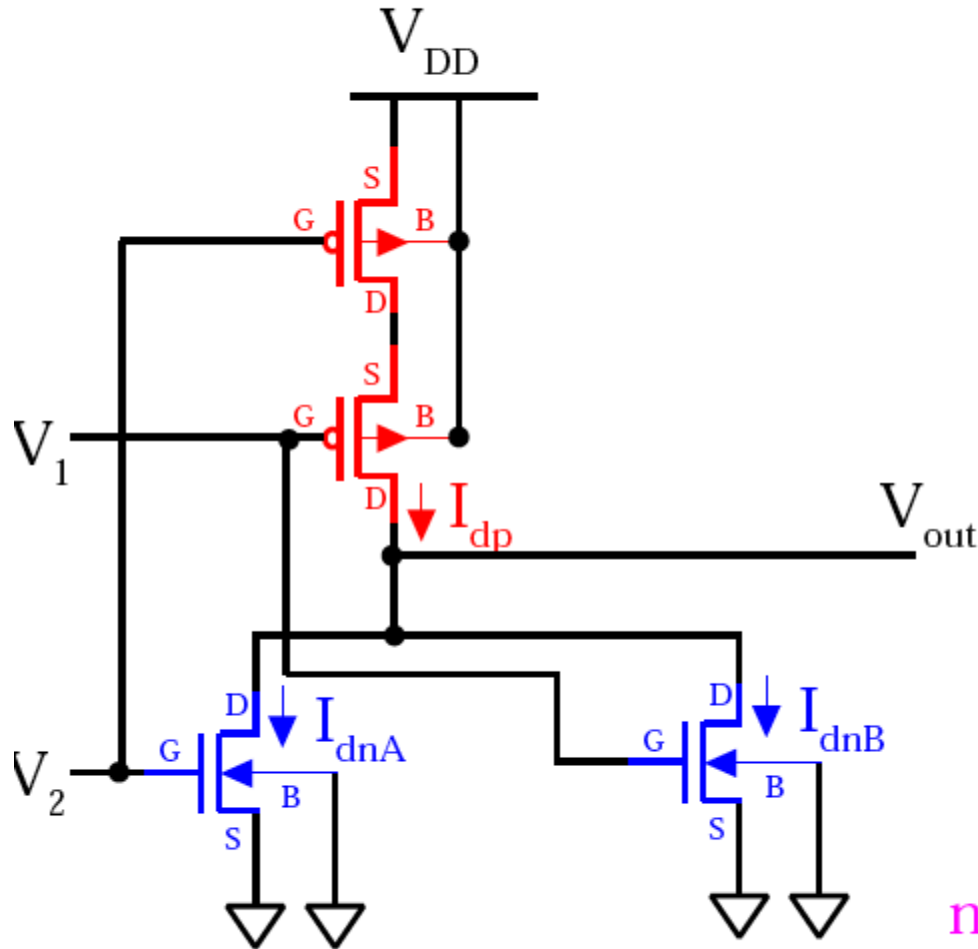# Digital IC Design and Architecture

Combinational Logic: CMOS Implementation
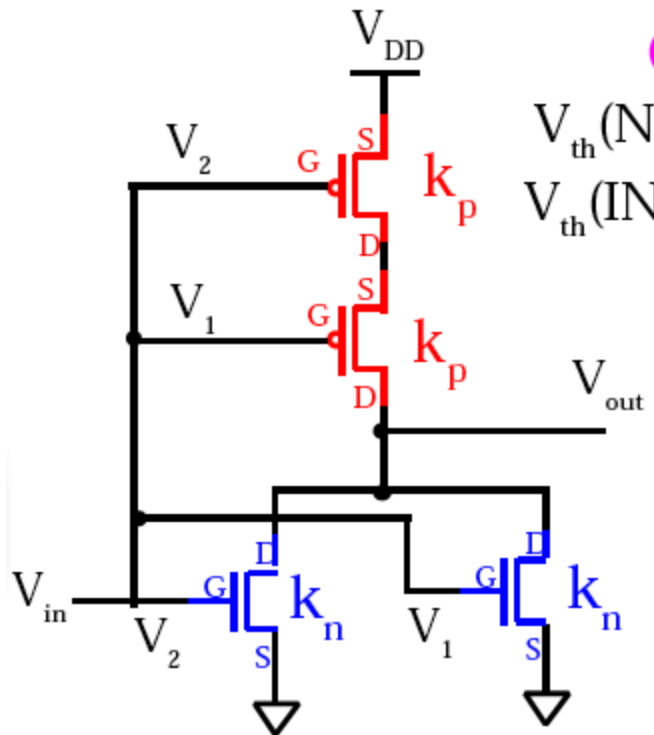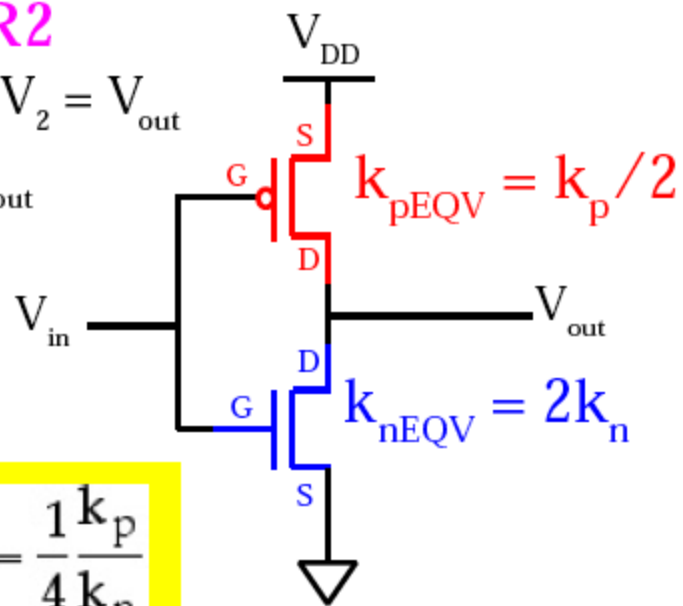
2-INPUT NOR (NR2)

nMOS Net ON, pMOS Net OFF
or
nMOS Net OFF, pMOS Net ON

CMOS NR2

$$V_{th}(NR2) => V_1 = V_2 = V_{out}$$

$$V_{th}(INV) = V_{in} = V_{out}$$

$$k_{pEQV} = k_p/2$$

$$k_{nEQV} = 2k_n$$

$$\frac{k_{pEQV}}{k_{nEQV}} = \frac{1}{4}\frac{k_p}{k_n}$$

$$V_{th}(NOR2) = \frac{V_{Tn} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$$
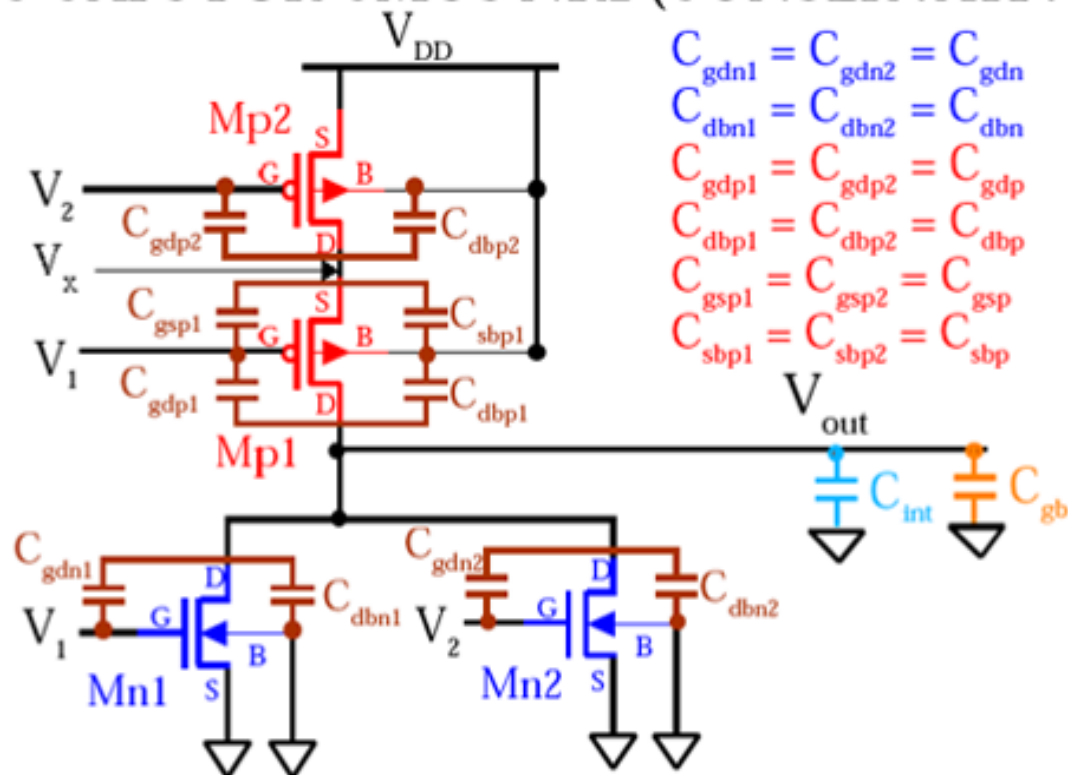
$$V_{th}(INV) = \frac{V_{Tn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$

Symmetrical EQUIV INV

$k_{pEQV} = k_{nEQV}$ or $k_{pEQV}/k_{nEQV} = 1$ and $V_{Tn} = |V_{Tp}| => V_{th}(INV) = V_{DD}/2$

$V_{th}(NR2) = V_{DD}/2 => k_p = 4k_n$

$$C_{gdn1} = C_{gdn2} = C_{gdn}$$
$$C_{dbn1} = C_{dbn2} = C_{dbn}$$
$$C_{gdp1} = C_{gdp2} = C_{gdp}$$
$$C_{dbp1} = C_{dbp2} = C_{dbp}$$
$$C_{gsp1} = C_{gsp2} = C_{gsp}$$
$$C_{sbp1} = C_{sbp2} = C_{sbp}$$

WORST CASE for PULL-UP => $V_1 = 0$, $V_2 = V_{DD} \rightarrow 0$ & $V_x = $ low -> high

$$C_{load-NR2} \approx 2C_{dbn} + 2C_{dbp} + C_{sbp} + C_{int} + C_{gb} = 2C_{dbn} + 3C_{dbp} + C_{int} + C_{gb}$$

WORST CASE for PULL-DOWN => $V_1 = 0$, $V_2 = 0 \rightarrow V_{DD}$ & $V_x = $ high -> low

$$C_{load-NR2} \approx 2C_{dbn} + 2C_{dbp} + C_{sbp} + C_{int} + C_{gb} = 2C_{dbn} + 3C_{dbp} + C_{int} + C_{gb}$$

NRn: $C_{load-NRn} \approx nC_{dbn} + (2n-1)C_{dbp} + C_{int} + C_{gb}$

NR2:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(NR2) = V_{DD}/2 \Rightarrow k_p = 4k_n$$

2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-NR2} \approx \frac{C_{load-NR2}}{2kn(VDD-VT0n)}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-NR2} \approx \frac{C_{load-NR2}}{\frac{kp(VDD-|VT0p|)}{2}}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

NRn:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:
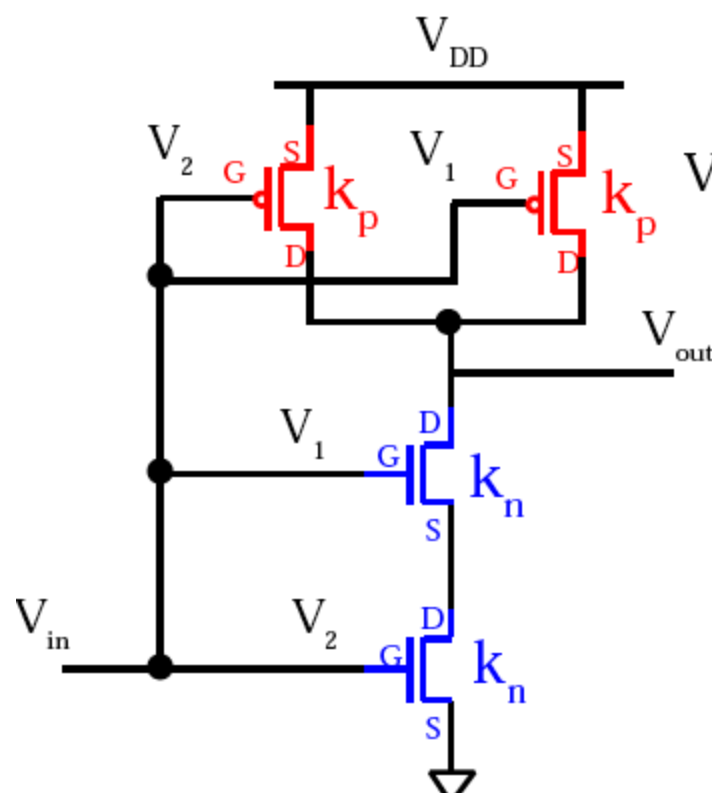
$$V_{th}(NRn) = V_{DD}/2 \Rightarrow k_p = n^2 k_n$$

2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-NRn} \approx \frac{C_{load-NRn}}{nkn(VDD-VT0n)}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-NRn} \approx \frac{C_{load-NRn}}{\frac{kp(VDD-|VT0p|)}{n}}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$
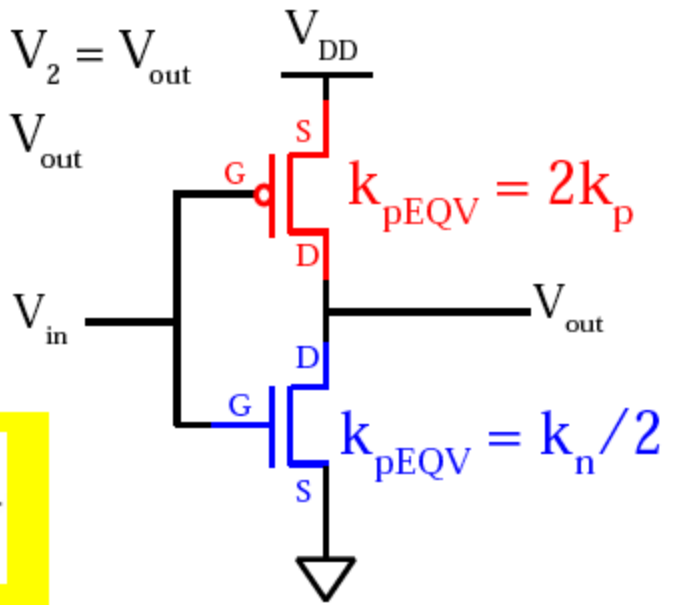
CMOS ND2

$$V_{th}(ND2) \Rightarrow V_1 = V_2 = V_{out}$$

$$V_{th}(INV) = V_{in} = V_{out}$$

$$\frac{k_{pEQV}}{k_{nEQV}} = 4\frac{k_p}{k_n}$$

$$k_{pEQV} = 2k_p$$

$$k_{pEQV} = k_n/2$$

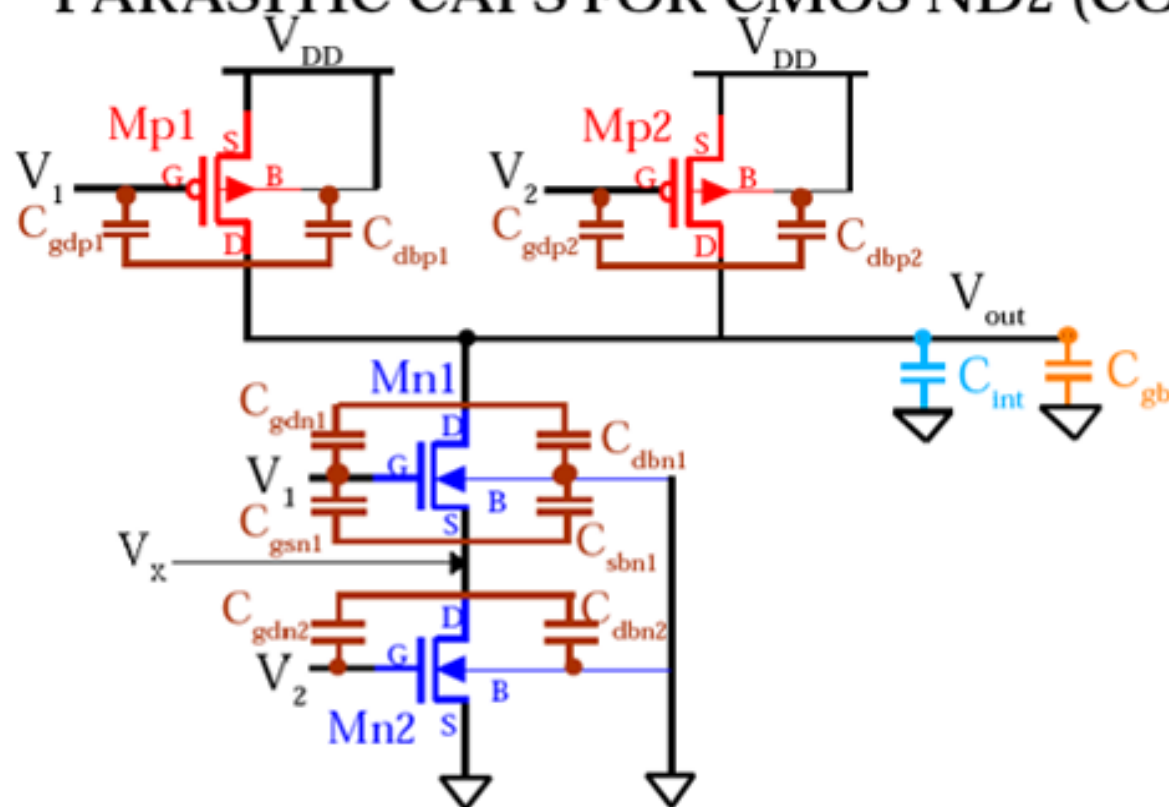$$V_{th}(NAND2) = \frac{V_{Tn} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

$$V_{th}(INV) = \frac{V_{Tn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$

Symmetrical EQUIV INV

$$k_{pEQV} = k_{nEQV} \text{ and } V_{Tn} = |V_{Tp}| \Rightarrow V_{th}(INV) = V_{DD}/2$$

$$V_{th}(ND2) = V_{DD}/2 \Rightarrow k_n = 4k_p$$

$$C_{gdn1} = C_{gdn2} = C_{gdn}$$
$$C_{dbn1} = C_{dbn2} = C_{dbn}$$
$$C_{gdp1} = C_{gdp2} = C_{gdp}$$
$$C_{dbp1} = C_{dbp2} = C_{dbp}$$
$$C_{gsp1} = C_{gsp2} = C_{gsp}$$
$$C_{sbp1} = C_{sbp2} = C_{sbp}$$

WORST CASE for PULL-UP => $V_1 = V_{DD}$, $V_2 = V_{DD} \to 0$ & $V_x = $ low -> high

$$C_{load-ND2} \approx 2C_{dbn} + C_{sbn} + 2C_{dbp} + C_{int} + C_{gb} = 3C_{dbn} + 2C_{dbp} + C_{int} + C_{gb}$$

WORST CASE for PULL-DOWN => $V_1 = V_{DD}$, $V_2 = 0 \to V_{DD}$ & $V_x = $ high -> low

$$C_{load-ND2} \approx 2C_{dbn} + C_{sbn} + 2C_{dbp} + C_{int} + C_{gb} = 3C_{dbn} + 2C_{dbp} + C_{int} + C_{gb}$$

NDn: $C_{load-NDn} \approx (2n-1)C_{dbn} + nC_{dbp} + C_{int} + C_{gb}$

CMOS ND DESIGN STRATEGIES

ND2:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(ND2) = V_{DD}/2 => k_n = 4k_p$$

2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-ND2} \approx \frac{C_{load-ND2}}{\frac{k_n(VDD-VT0n)}{2}} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH-ND2} \approx \frac{C_{load-ND2}}{2k_p(VDD-|VT0p|)} \left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1 \right) \right]$$

NDn:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(NDn) = V_{DD}/2 => k_n = n^2 k_p$$

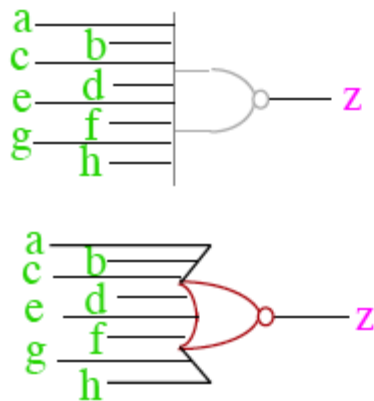**2. Propogation delay τ_{PHL} or τ_{PLH}:**

$$\tau_{PHL-NDn} \approx \frac{C_{load-NDn}}{\frac{k_n(VDD-VT0n)}{n}} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH-NDn} \approx \frac{C_{load-NDn}}{nk_p(VDD-|VT0p|)} \left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1 \right) \right]$$

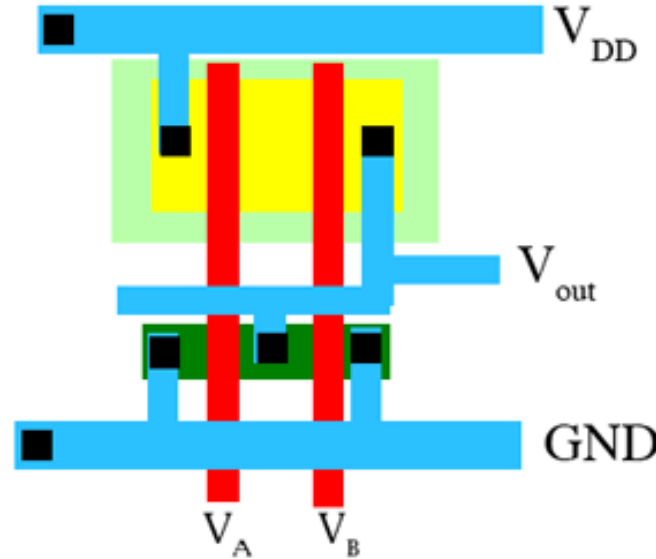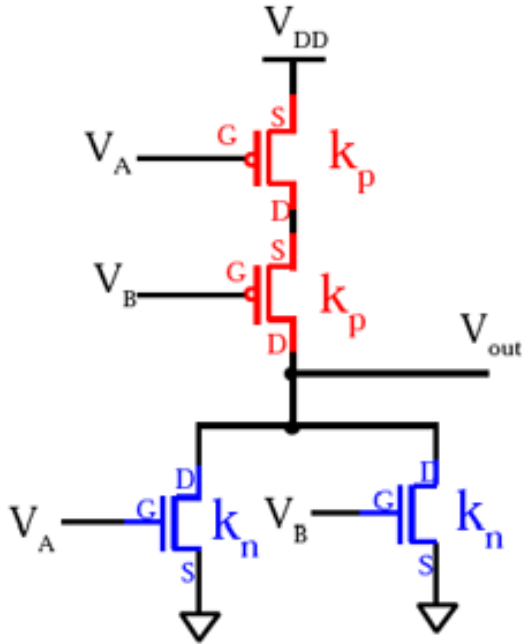# TYPICAL CMOS NAND AND NOR DELAYS

Delays for a Family of NAND & NOR gates

1. $W_n = 6.4\ \mu m,\ L_n = 1\ \mu m,$ and $W_p = 12.8\ \mu m,\ L_p = 1\ \mu m.$

2. $t_{input\text{-}rise/fall} = 0.1\ ns$ and $C_{load} = 0 \rightarrow 1\ pF.$
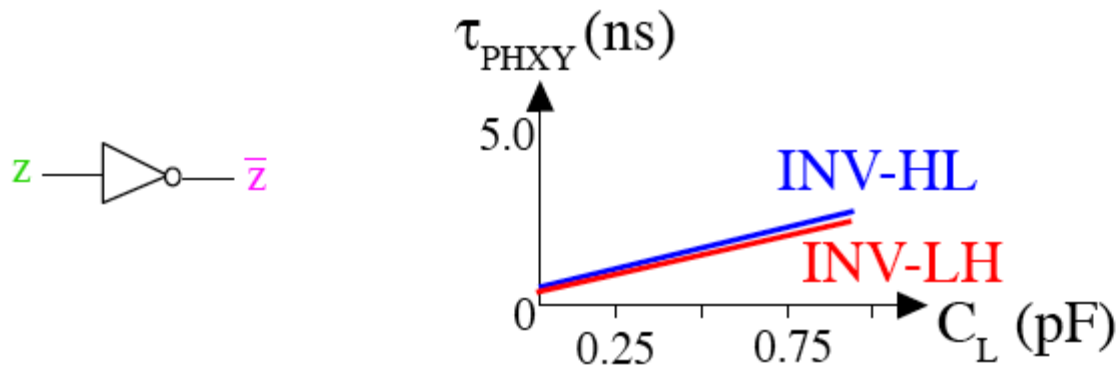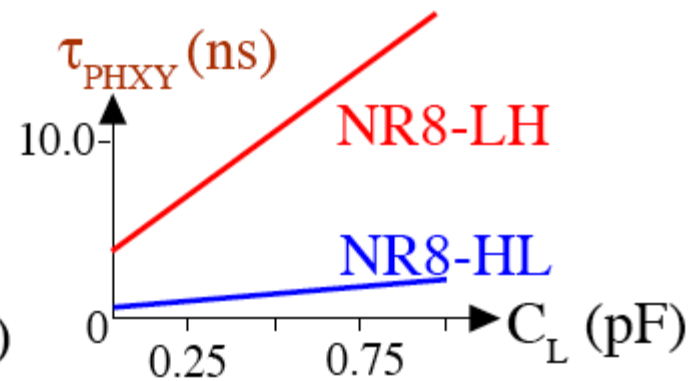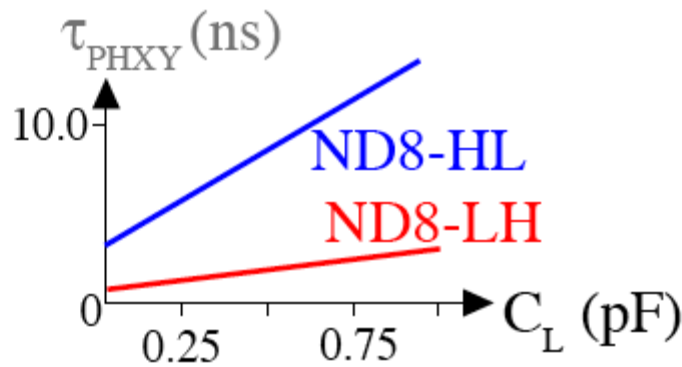
NR2 Layout Example

COLOR LEGEND

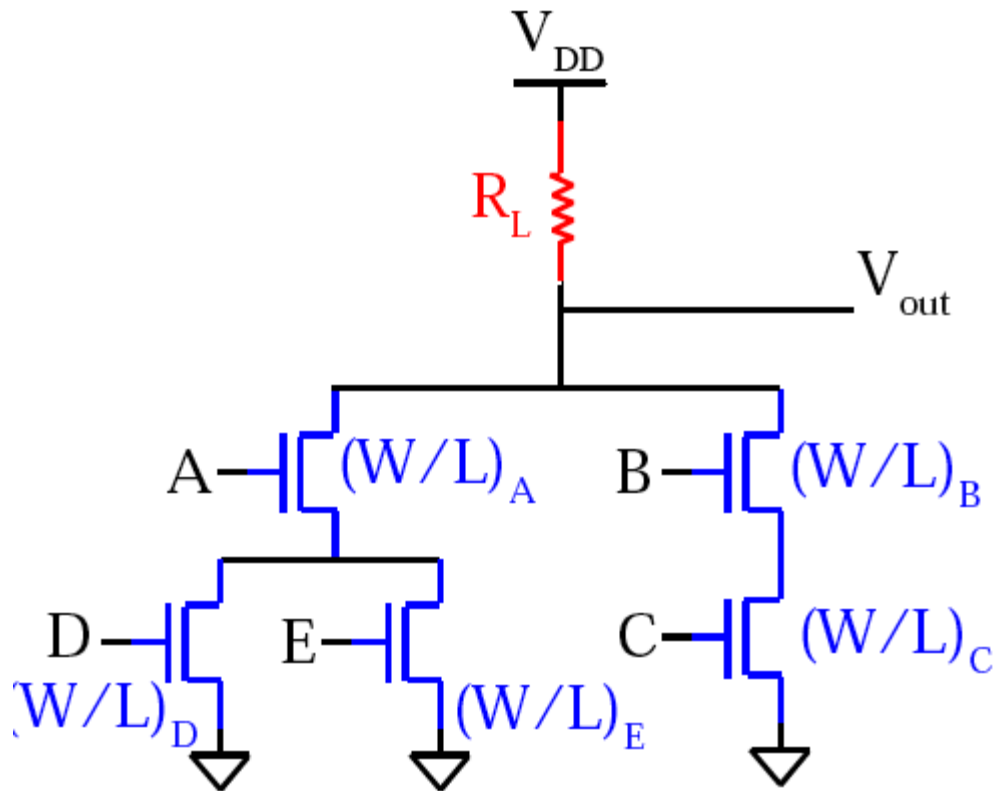|	
n-Well	
p-Well	
n+	
Polysilicon	
p+	
Gate Oxide	
Field Oxide	
Metal 1	
Metal 2	
Metal 3	
■ Contact/via	

STICK DIAGRAM →

ND2 Layout Example
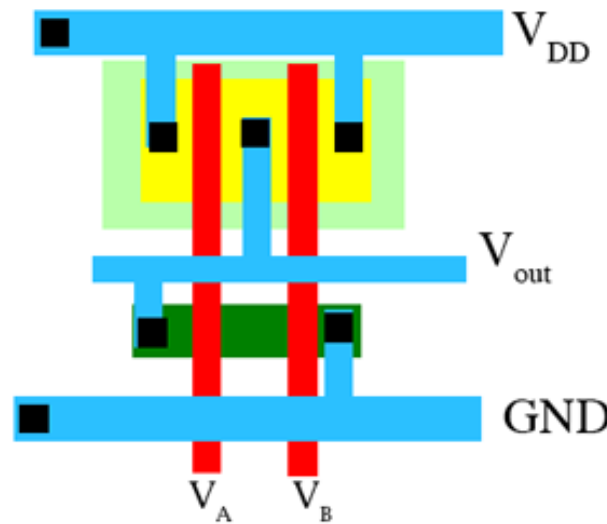
COMPLEX LOGIC GATES

$$Z = \overline{A(D + E) + BC}$$

"OR" OPS PERFORMED BY PARALLEL CONECTED DRIVERS.
"AND" OPS PERFORMED BY SERIES CONNECTED DRIVERS.
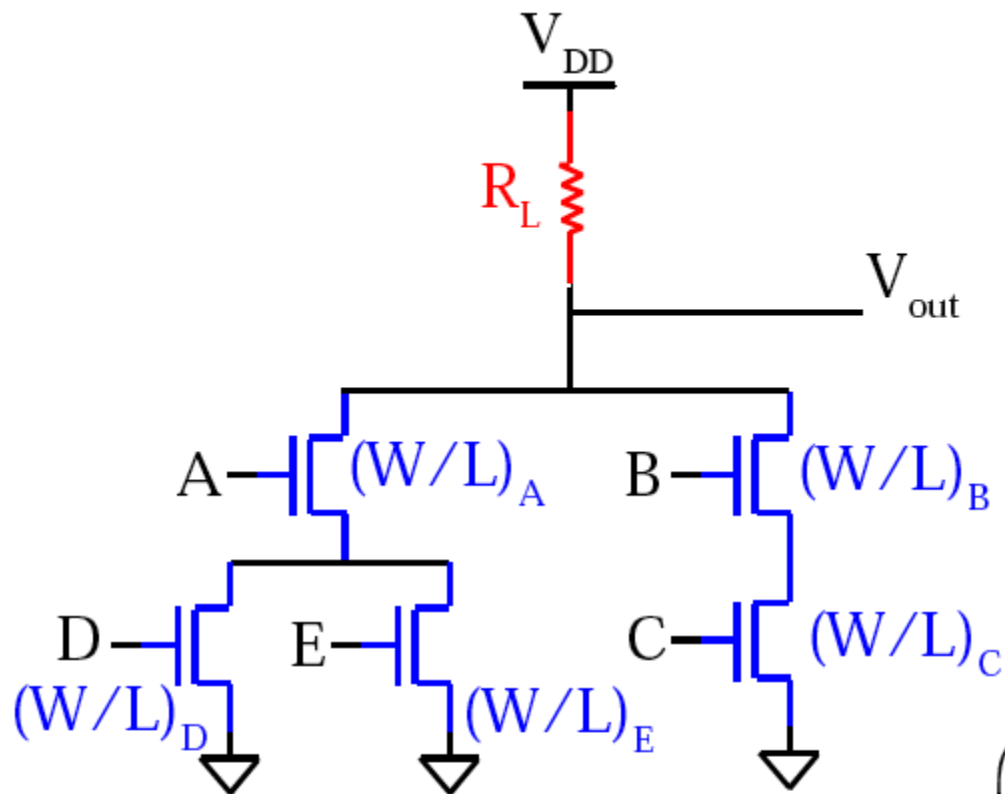"INVERSION" IS PROVIDED BY NATURE OF MOS CIRCUIT OP.

V_{DD}

R_L

V_{out}

A — $(W/L)_A$ B — $(W/L)_B$

D — E — C — $(W/L)_C$

$(W/L)_D$ $(W/L)_E$
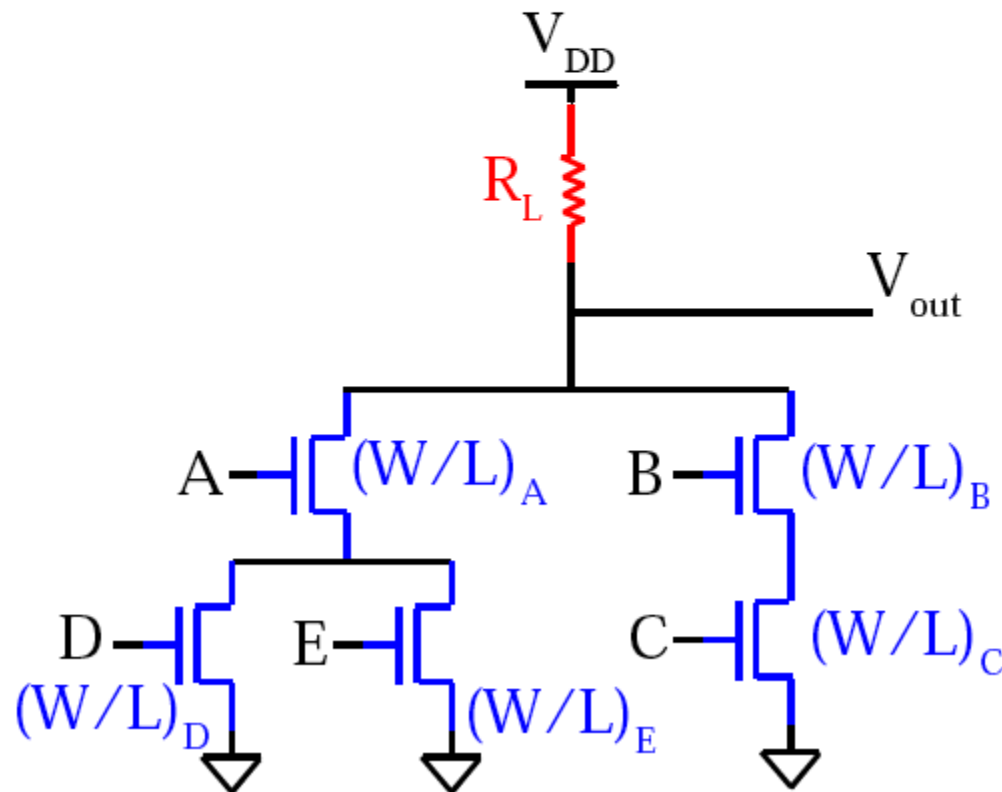
ON Drivers	Out-GND Path
A-D	Class 1
A-E	Class 1
B-C	Class 1
A-D-E	Class 2
A-D-B-C	Class 3
A-E-B-C	Class 3
A-D-E-B-C	Class 4

$$G1 < G2 < G3 < G4$$

$$V_{OL1} > V_{OL2} > V_{OL3} > V_{OL4}$$

EQV INVERTER (for case G4 where A = B = C = D = E = 1)

$$\left(\frac{W}{L}\right)_{EQV} = \cfrac{1}{\cfrac{1}{\left(\frac{W}{L}\right)_B} + \cfrac{1}{\left(\frac{W}{L}\right)_C}} + \cfrac{1}{\cfrac{1}{\left(\frac{W}{L}\right)_A} + \cfrac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E}}$$

DESIGN STRATEGY:
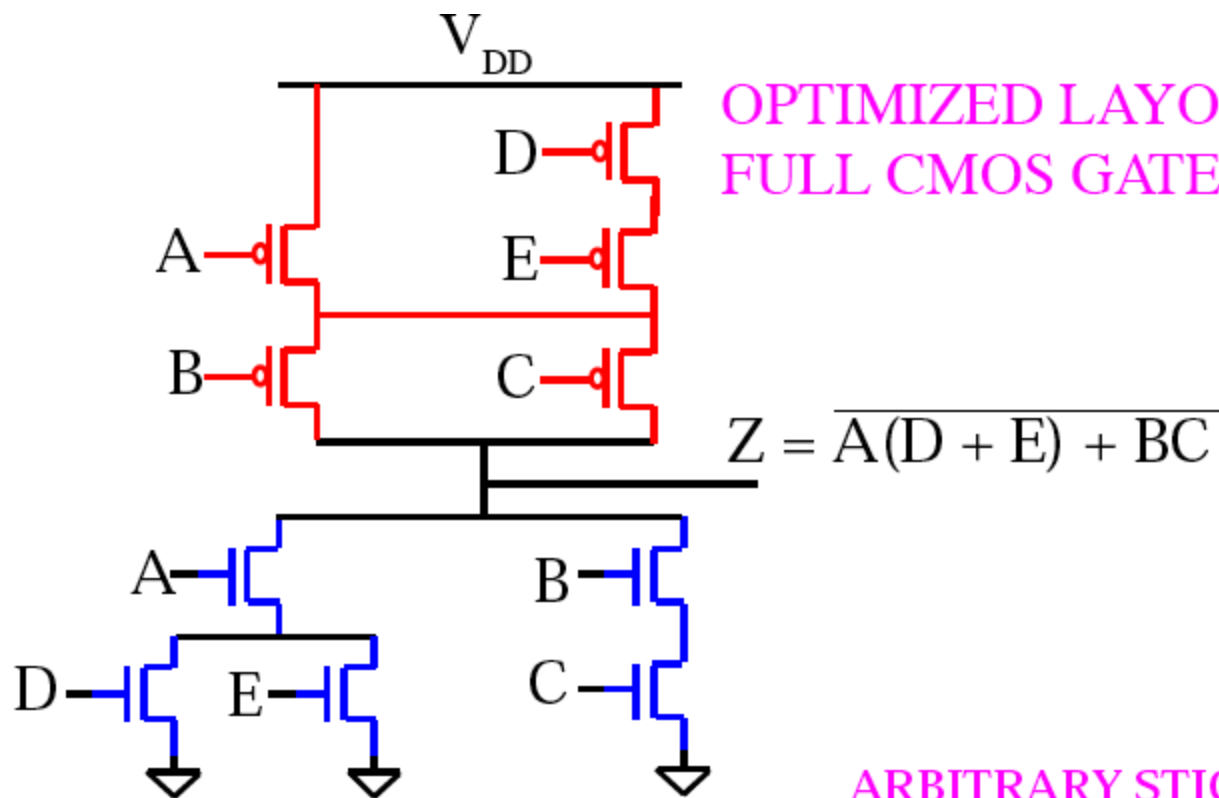1. Identify all WORST CASE Paths (e.g. Class 1).
2. Determine nMOS transistor sizes such that each Class 1 path has $(W/L)_{EQV}$.

$$\left(\frac{W}{L}\right)_{EQV-ND2} = \frac{1}{2}\left(\frac{W}{L}\right)$$

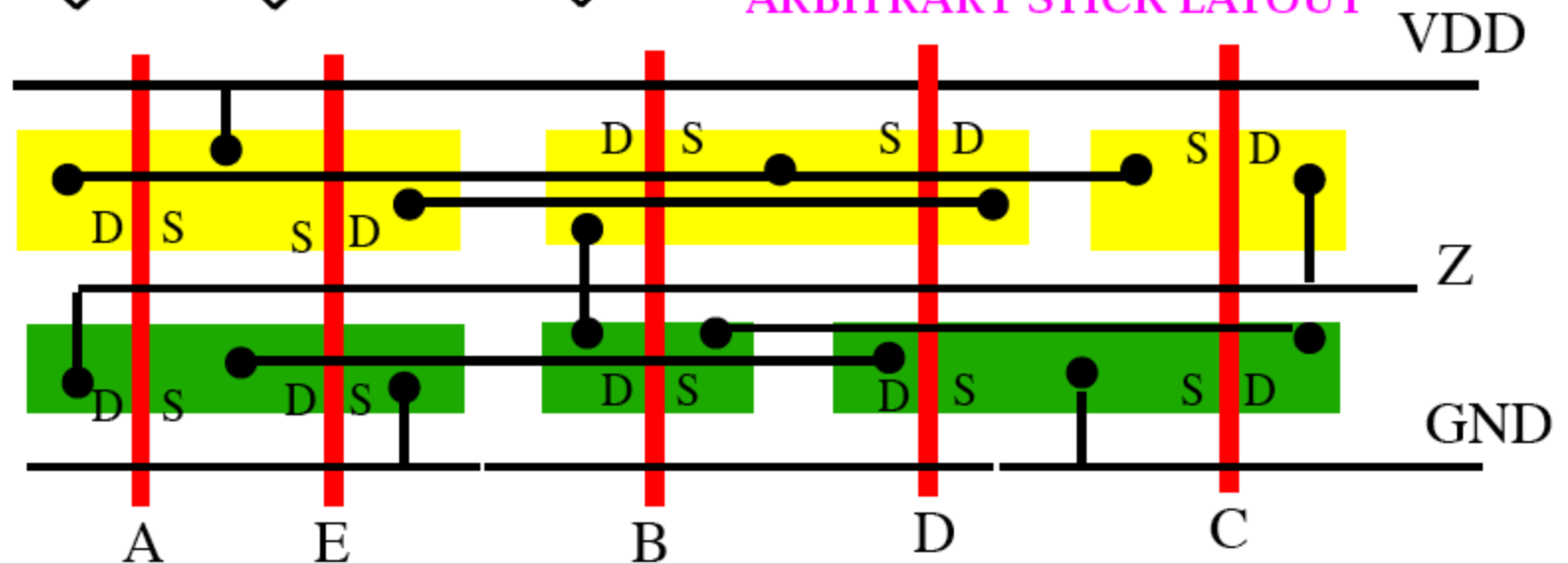$$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_D = 2\left(\frac{W}{L}\right)_{EQV}$$

$$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_E = 2\left(\frac{W}{L}\right)_{EQV}$$
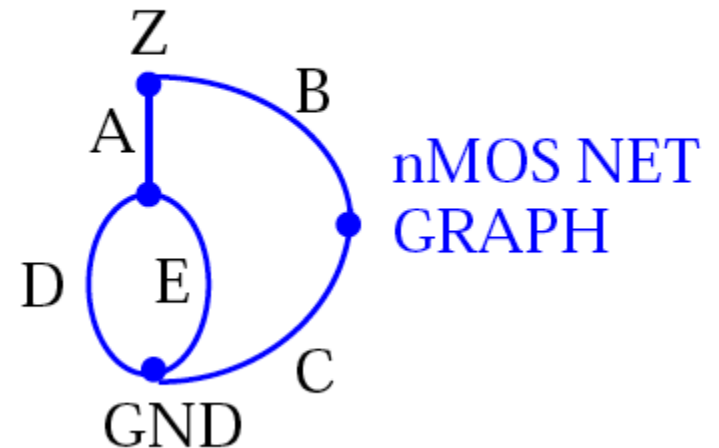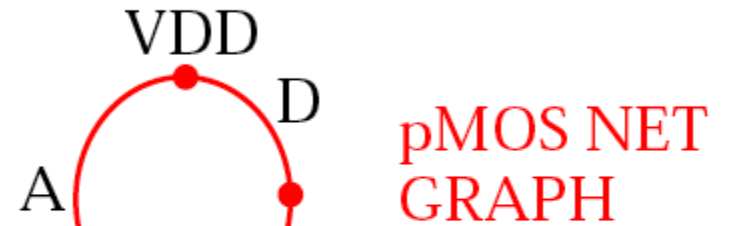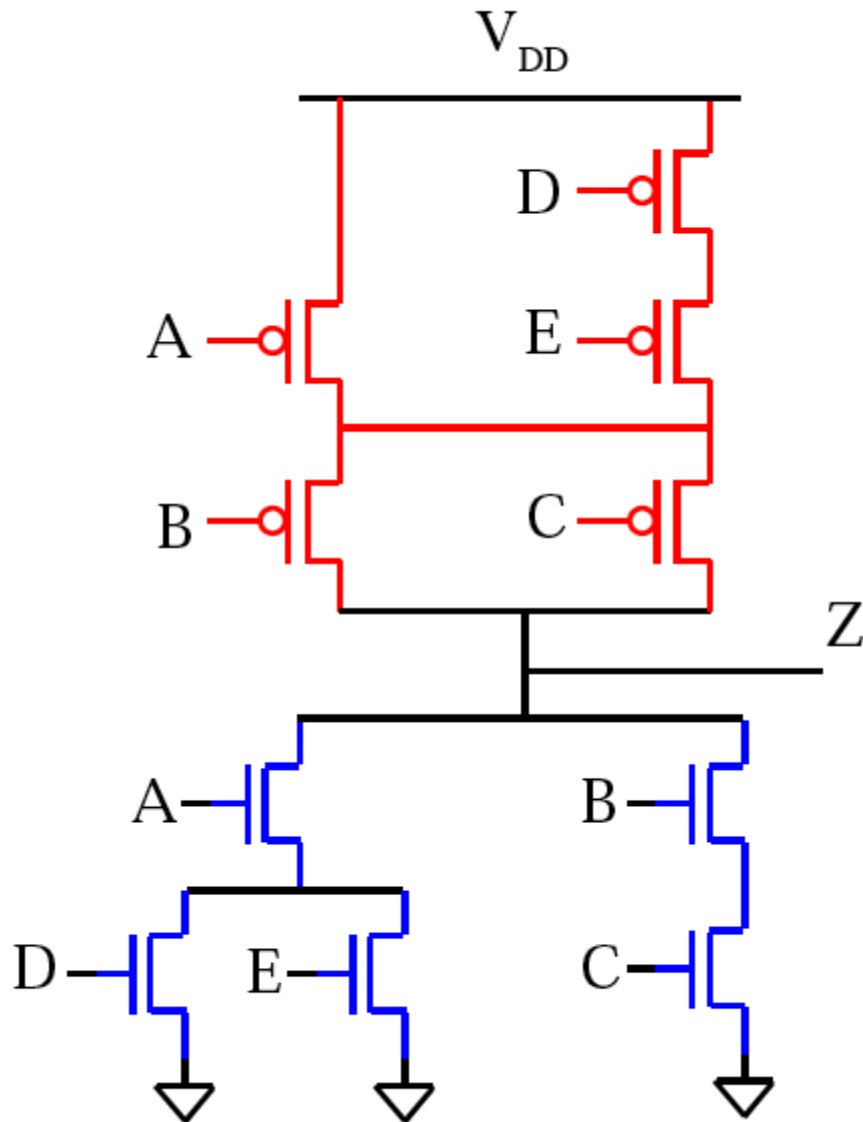
$$\left(\frac{W}{L}\right)_B = \left(\frac{W}{L}\right)_C = 2\left(\frac{W}{L}\right)_{EQV}$$

OPTIMIZED LAYOUT OF COMPLEX
FULL CMOS GATES

$$Z = \overline{A(D + E) + BC}$$
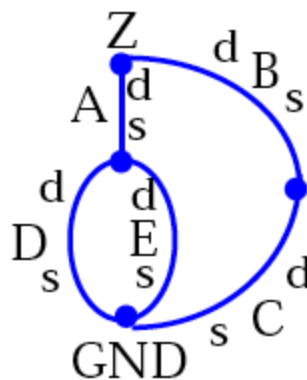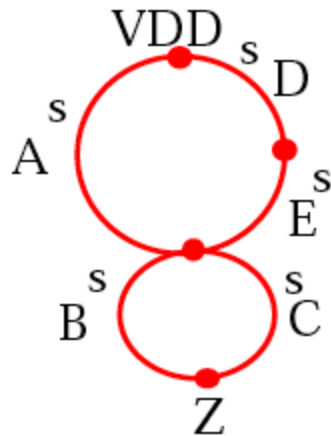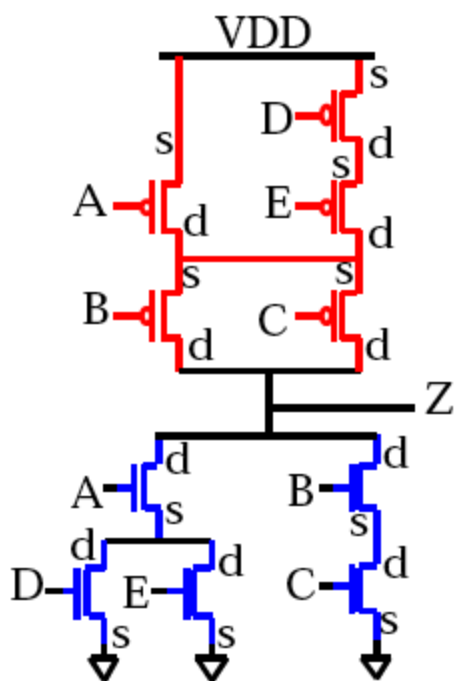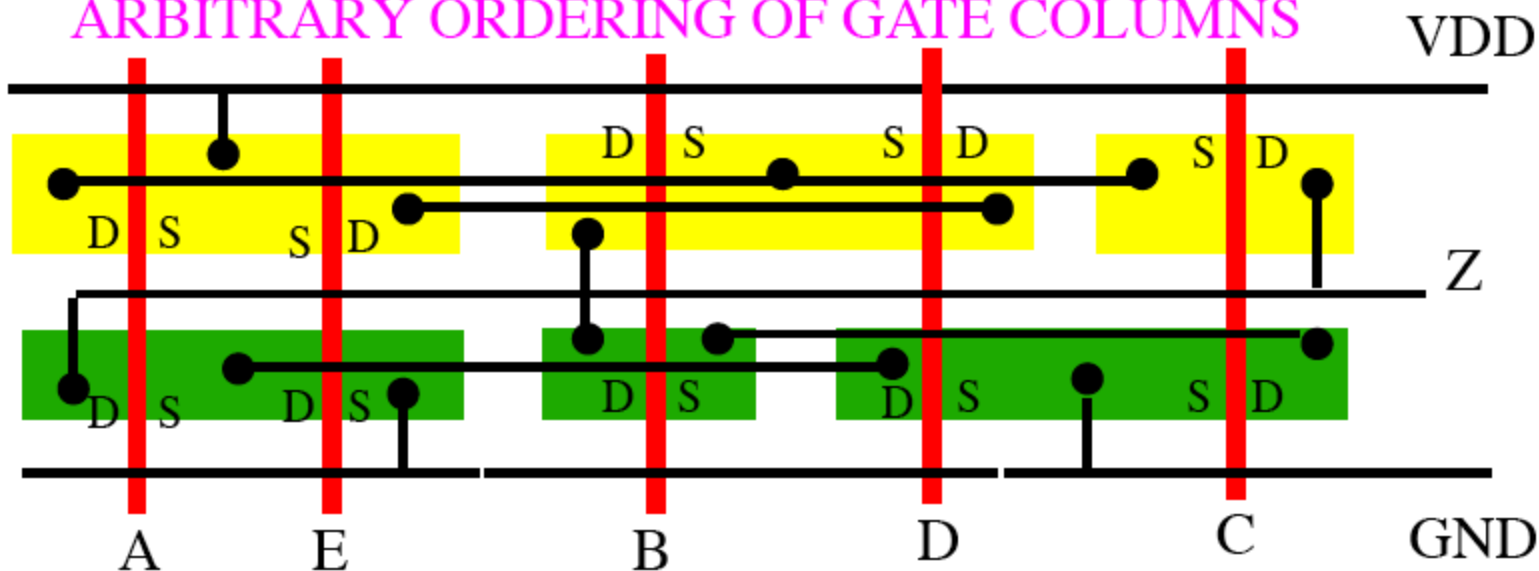
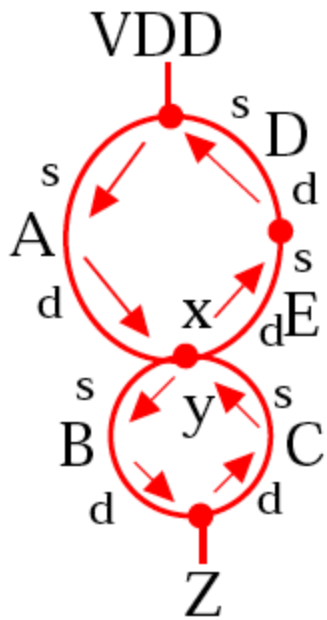ARBITRARY STICK LAYOUT

OTIMIZED LAYOUT OF COMPLEX FULL CMOS GATES

pMOS NET GRAPH

nMOS NET GRAPH

Euler path - connected sequence of edges

n, p diffusions for common Euler paths have layouts with no diffusion breaks.

COMMON
EULER PATH:
E-D-A-B-C

Is A-D-E-C-B a
common Euler
path?
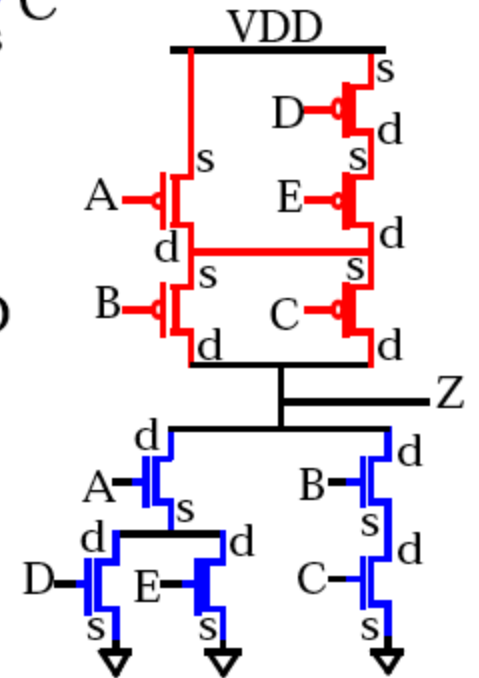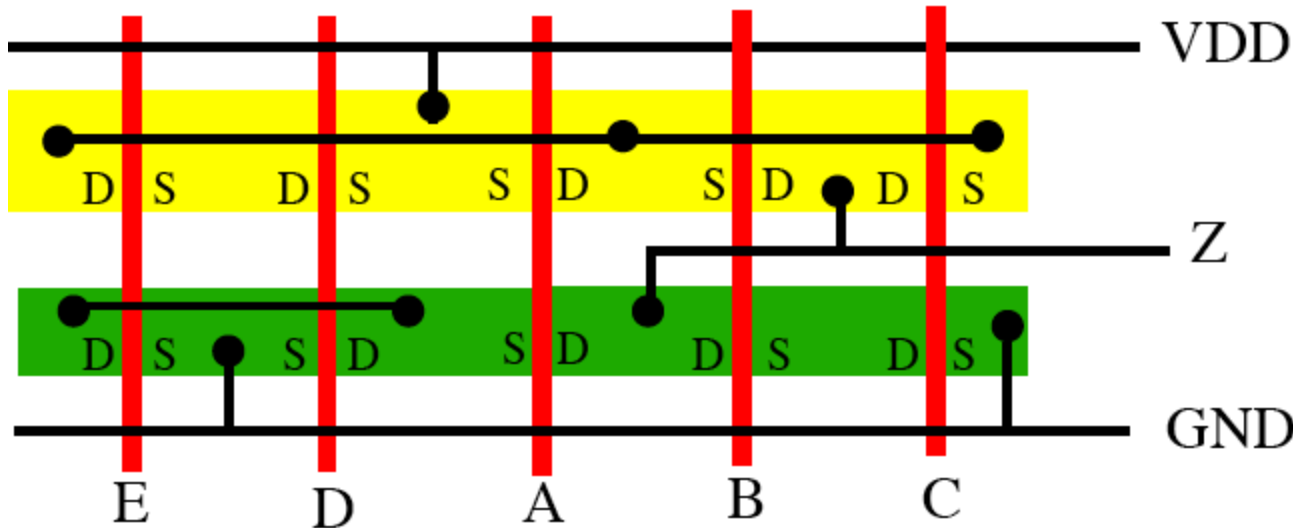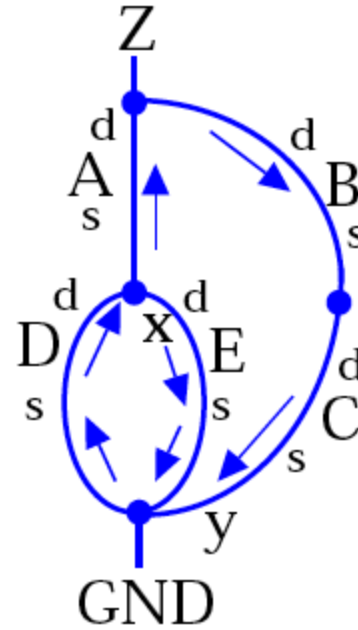
Arbitraty Stack

Optimized Stack

ALGORYTHYM FOR LINE OF GATES LAYOUT STYLE

1. Find all Euler paths that cover the graph.

2. Find common n- and p- Euler paths.

3. If no Euler paths are found in step 2, break the gate in the minimum number of places that to achieve step 2 with separate common Euler paths.

FULL CMOS XOR GATE

$$A \oplus B = \overline{A}B + A\overline{B}$$

V_{DD}

$\overline{A}$

$\overline{B}$
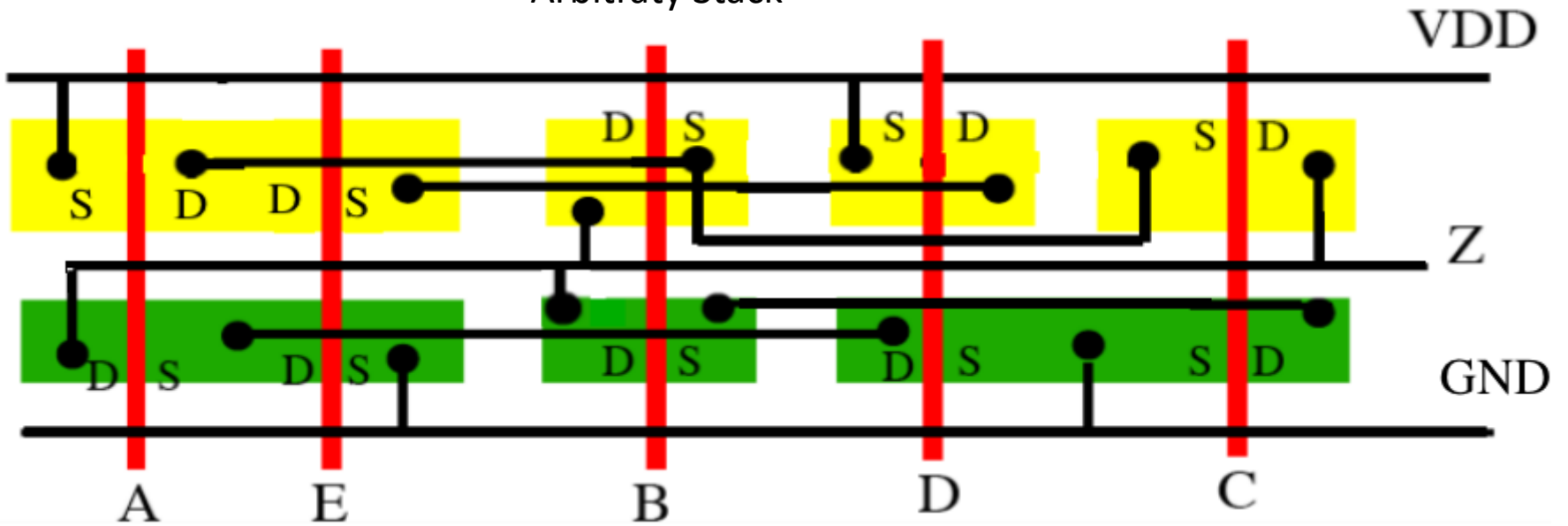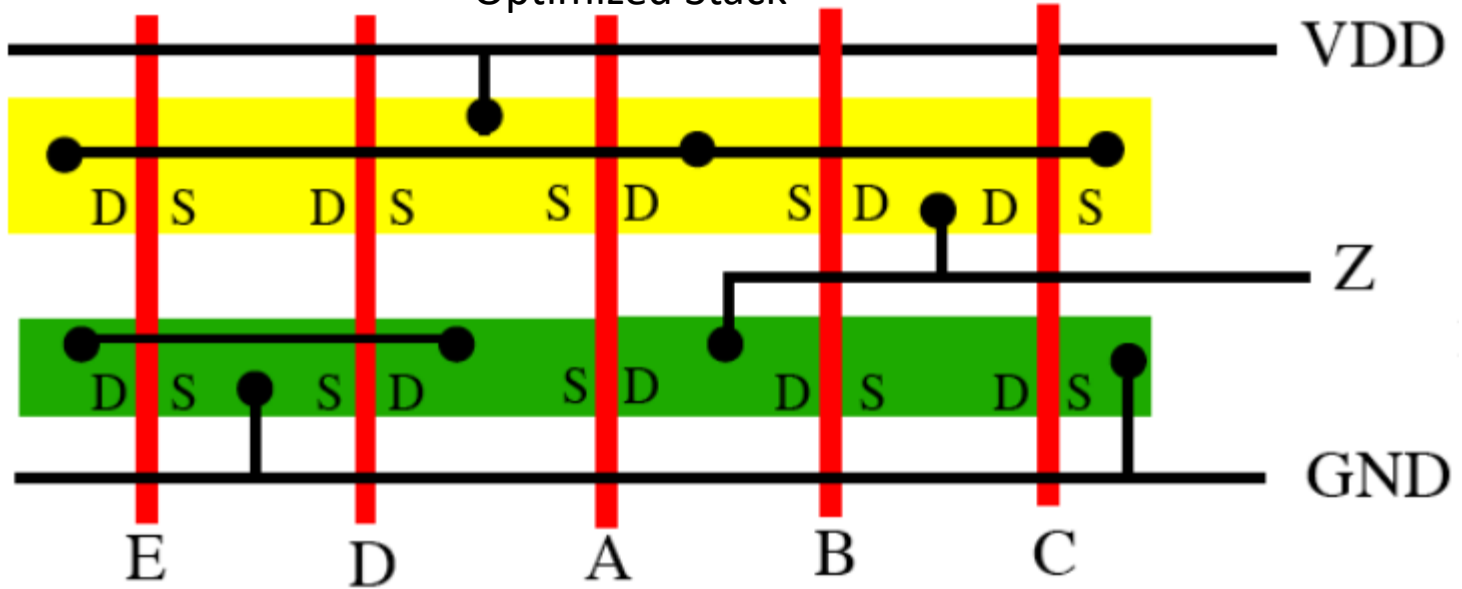
A

B

V_{out}

$\overline{A}$

A

$\overline{B}$

B

$A \oplus B$

A

B

$$\overline{(\overline{A}\cdot\overline{B})+(A\cdot B)}=\overline{(\overline{A}\cdot\overline{B})}\cdot\overline{(A\cdot B)}=(A+B)\cdot(\overline{A}+\overline{B})$$

$$(A+B)\cdot(\overline{A}+\overline{B})=A\cdot\overline{A}+\overline{A}\cdot B+A\cdot\overline{B}+B\overline{B}=\overline{A}\cdot B+A\cdot\overline{B}$$
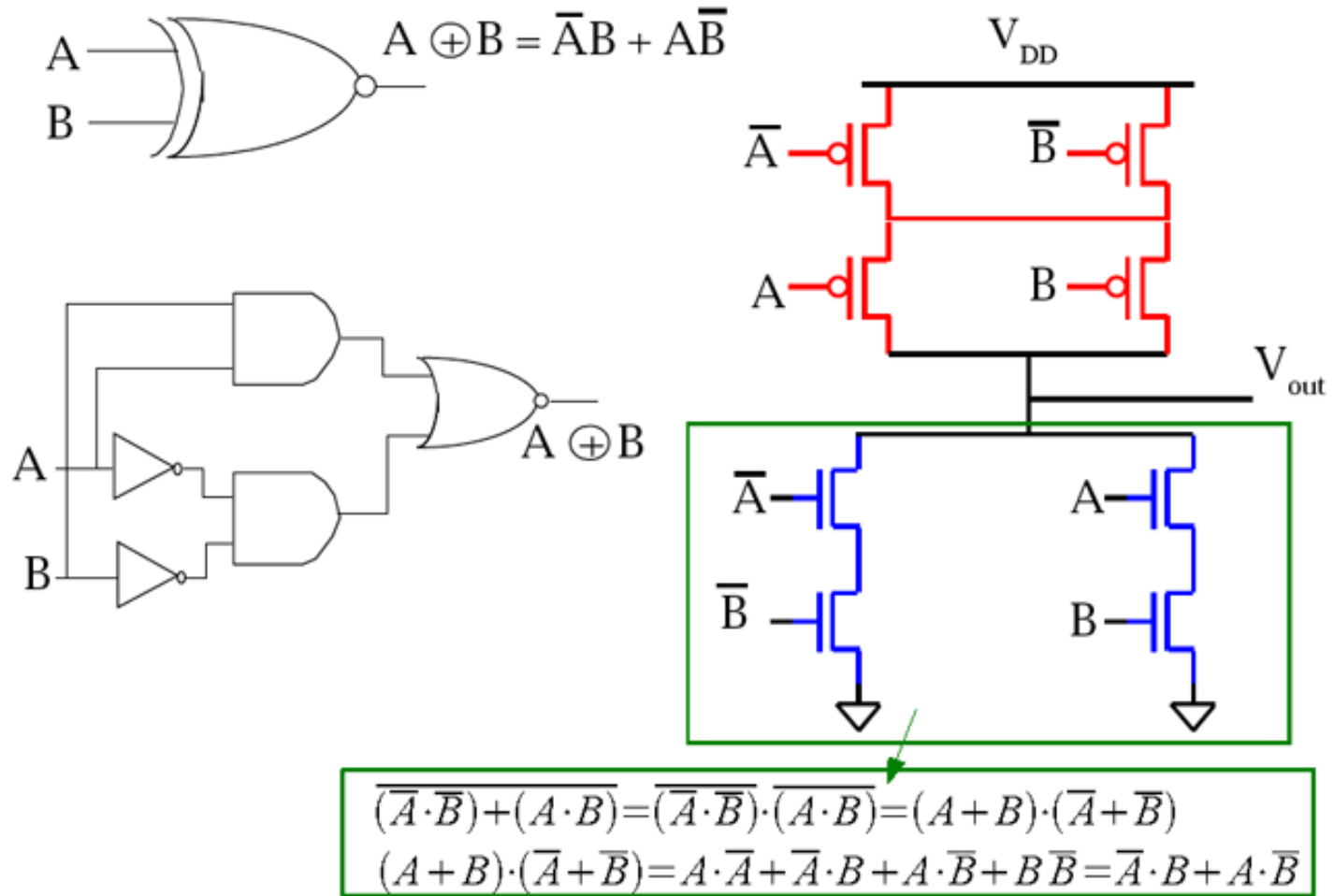
AOI & OAI GATES

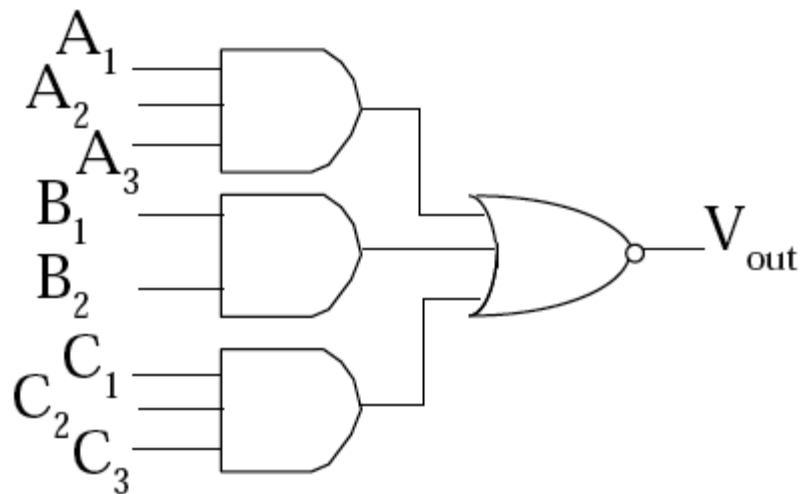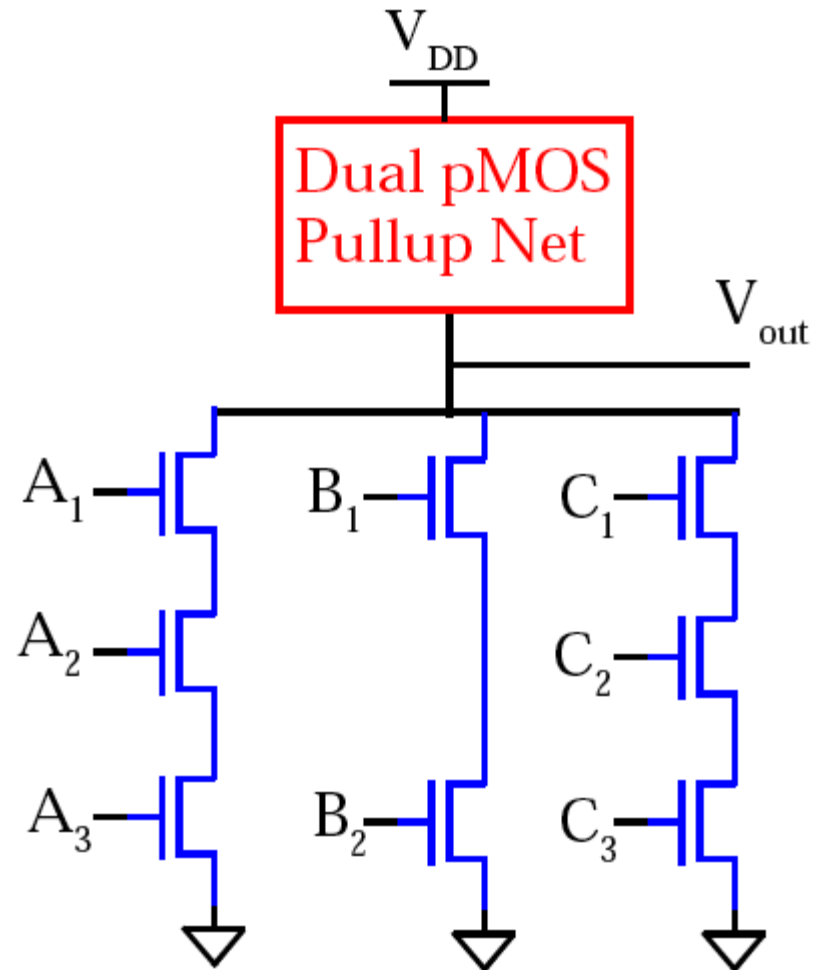AOI -> AND-OR-INVERT (for SUM - of - PRODUCTS Realization)
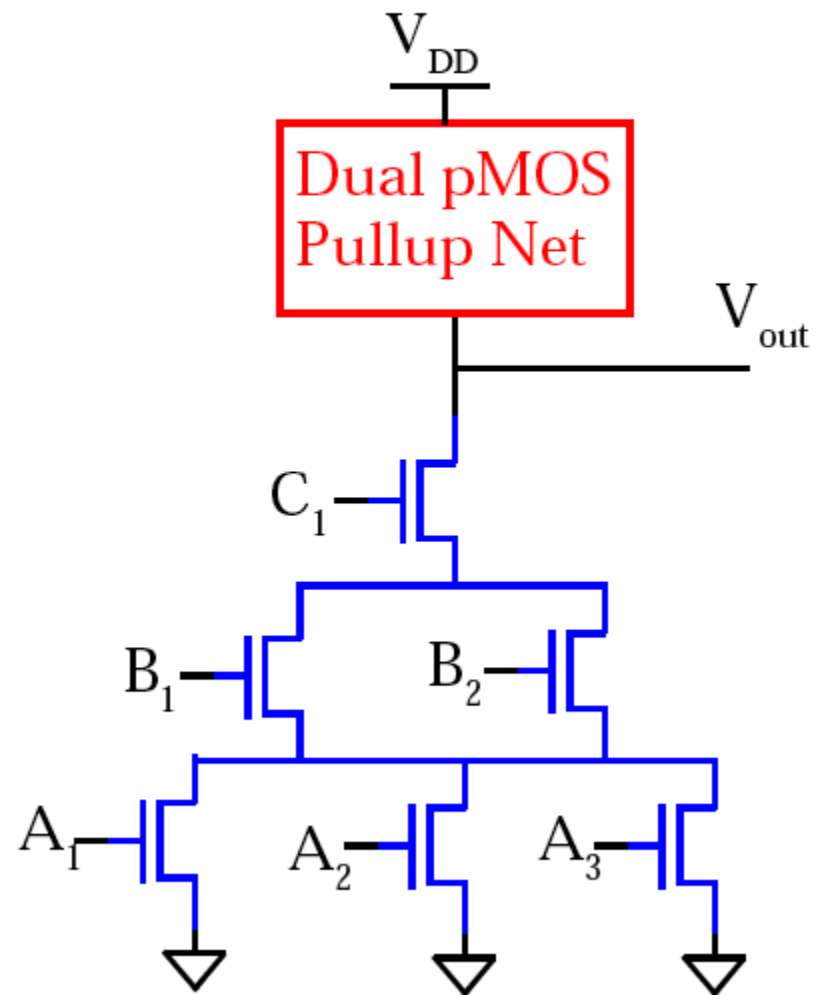OAI -> OR-AND-INVERT (for PRODUCT - of - SUMS Realization)

AOI

OAI -> OR-AND-INVERT (for PRODUCT - of - SUMS Realization)

OAI

V_{DD}

Dual pMOS
Pullup Net

V_{out}

C_1

B_1 B_2

A_1 A_2 A_3
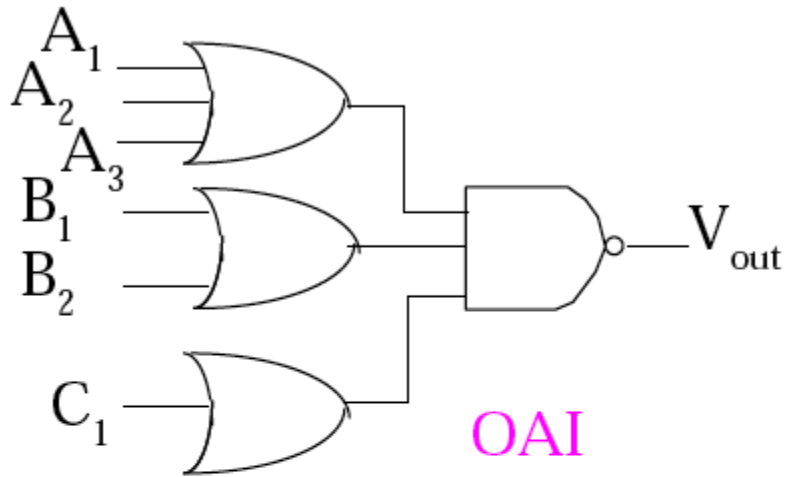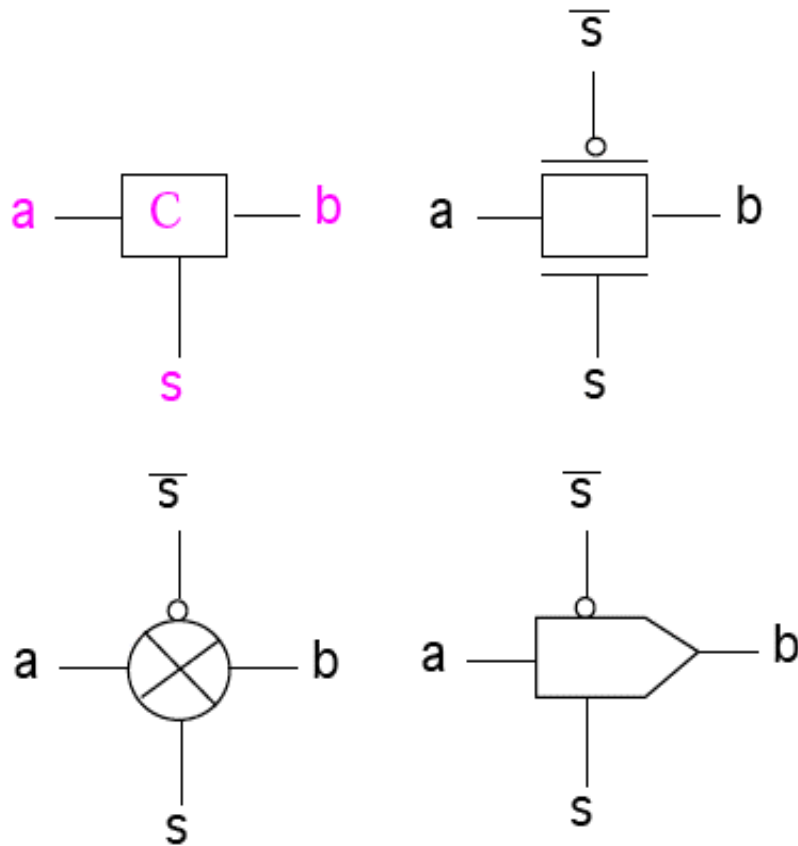
Pseudo-nMOS OAI Realization
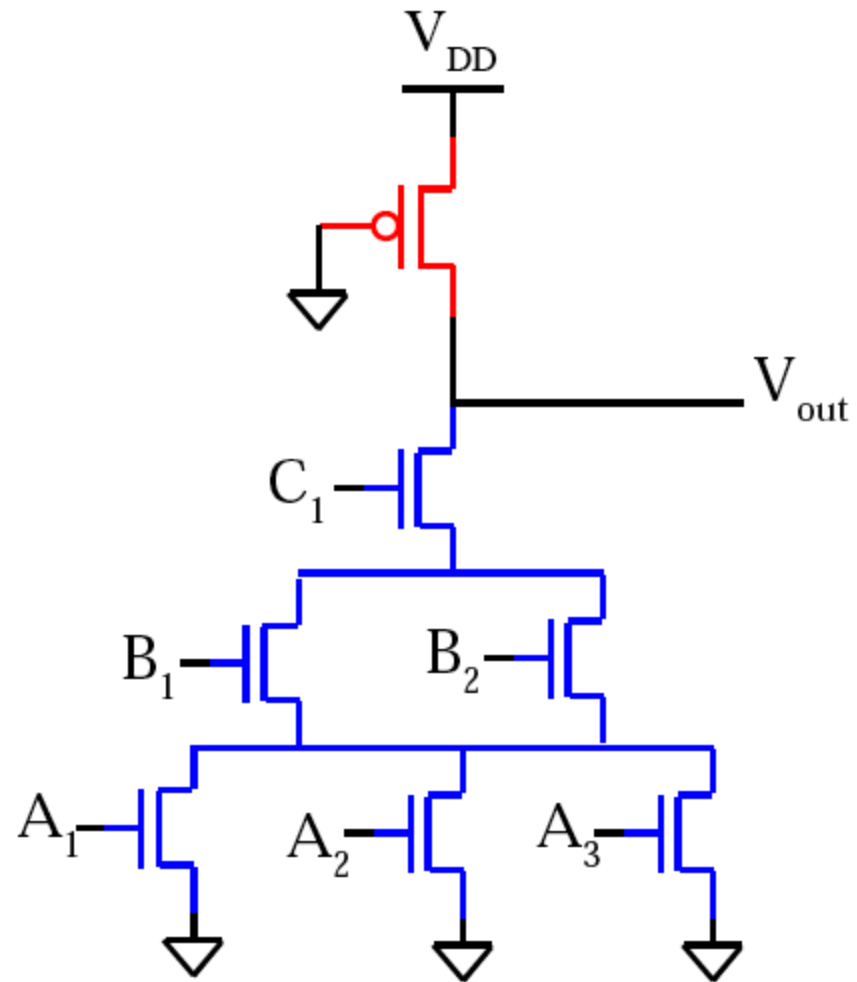
CMOS Transmission Gates (TGs) & TG Logic

SYMBOLS

SWITCH CHARACTERISTICS

Input		Output
0	a ──○▶○── b	Strong 0
1	a ──○▶○── b	Strong 1

$$I_C = I_{DSn} + I_{SDp}$$

$$0V$$

$$I_{SDp}$$

$$V_{SBp} = 0$$

$$V_{in} = V_{DD}$$

S B D

$$I_C \quad V_{out}$$

D B S

$$I_{DSn}$$

$$V_{SBn} = V_{out}$$

$$V_{DD}$$

$$V_{DSn} = V_{DD} - V_{out}$$

$$V_{GSn} = V_{DD} - V_{out}$$

$$V_{DSp} = V_{out} - V_{DD}$$

$$V_{GSp} = -V_{DD}$$

REGION 1
nMOS: SAT
pMOS: SAT
$$V_{DSn} > V_{GSn} - V_{Tn}$$
$$V_{DSp} < V_{GSp} - V_{Tp}$$

REGION 2
nMOS: SAT
pMOS: LIN
$$V_{DSn} > V_{GSn} - V_{Tn}$$
$$V_{DSp} > V_{GSp} - V_{Tp}$$

REGION 3
nMOS: OFF
pMOS: LIN
$$V_{GSn} < V_{Tn}$$
$$V_{DSp} > V_{GSp} - V_{Tp}$$

$$V_{out}$$

$$0V \qquad |V_{Tp}| \qquad (V_{DD} - V_{Tn}) \qquad V_{DD}$$
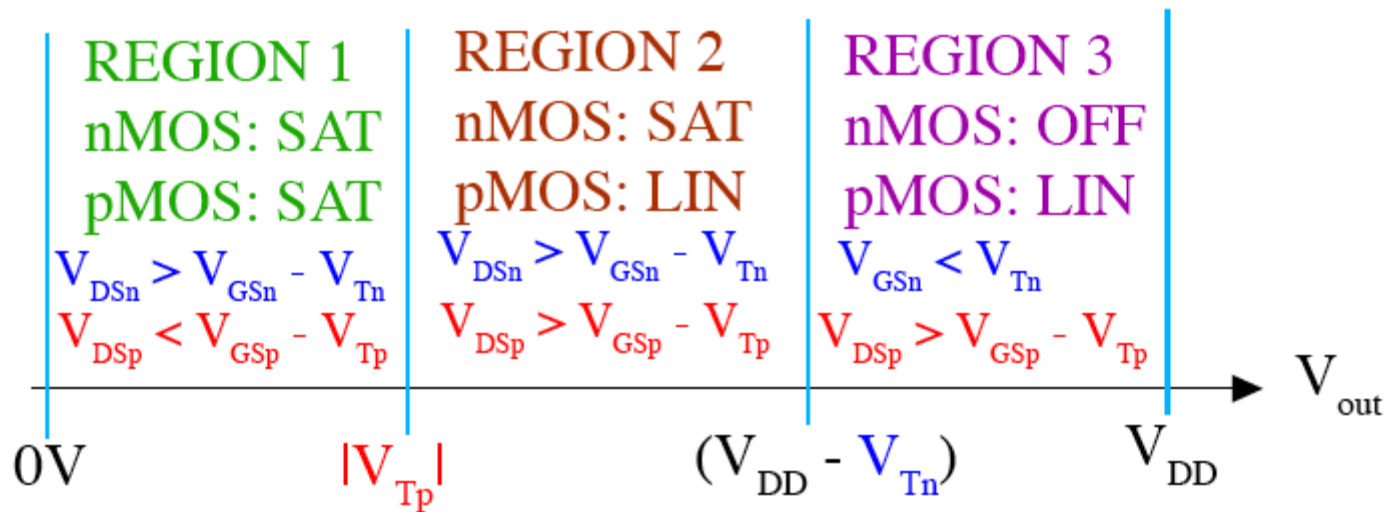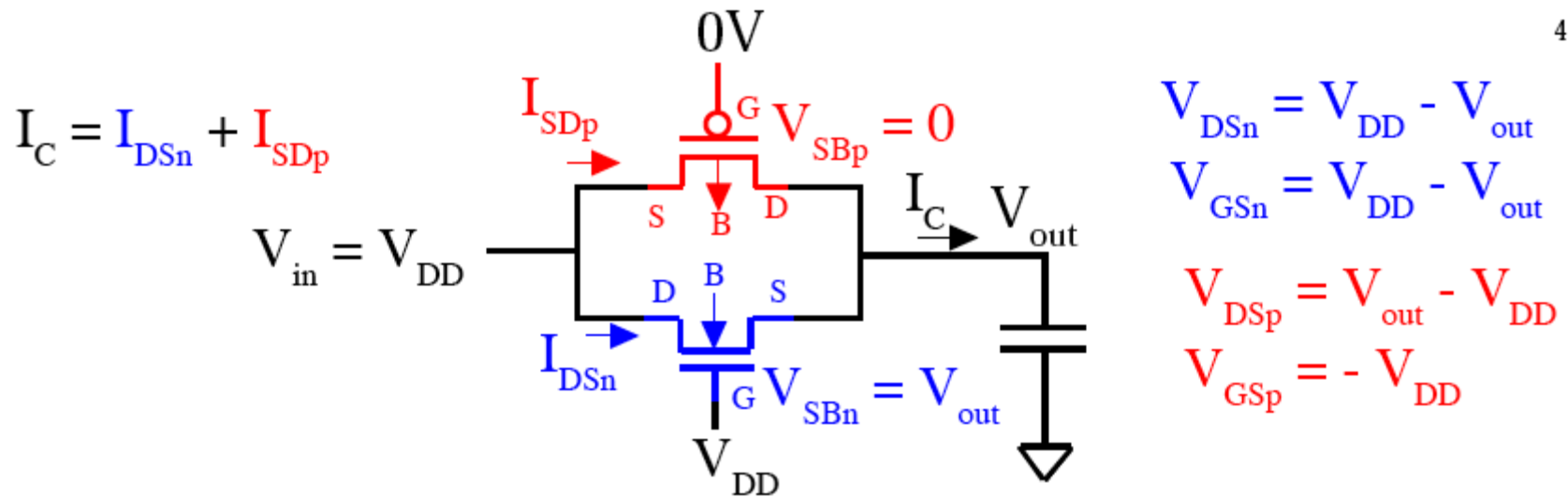
$$R_{eqn} = \frac{V_{DD} - V_{out}}{I_{DSn}} \qquad R_{eqp} = \frac{V_{DD} - V_{out}}{I_{SDp}} \qquad R_{eqTOT} = R_{eqn} \| R_{eqp}$$

REGION 1:
nMOS: SAT
pMOS: SAT

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{k_n(V_{DD} - V_{out} - V_{Tn})^2}$$

$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{k_p(V_{DD} - |V_{Tp}|)^2}$$

REGION 2
nMOS: SAT
pMOS: LIN

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{k_n(V_{DD} - V_{out} - V_{Tn})^2}$$

$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{k_p\left[2(V_{DD} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right]}$$

$$= \frac{2}{k_p\left[2(V_{DD} - |V_{Tp}|) - (V_{DD} - V_{out})\right]}$$

REGION 3
nMOS: OFF
pMOS: LIN

$$R_{eqn} = \infty$$

$$R_{eqp} = \frac{2}{k_p\left[2(V_{DD} - |V_{Tp}|) - (V_{DD} - V_{out})\right]}$$

i_{SDp}

$V_{in} = V_{DD}$

i_{DSn}

$t = 0$

V_{out}

i_C

C_{load}

R_{eqTOT}

$V_{in} = V_{DD}$

$t = 0$

V_{out}

i_C

C_{load}
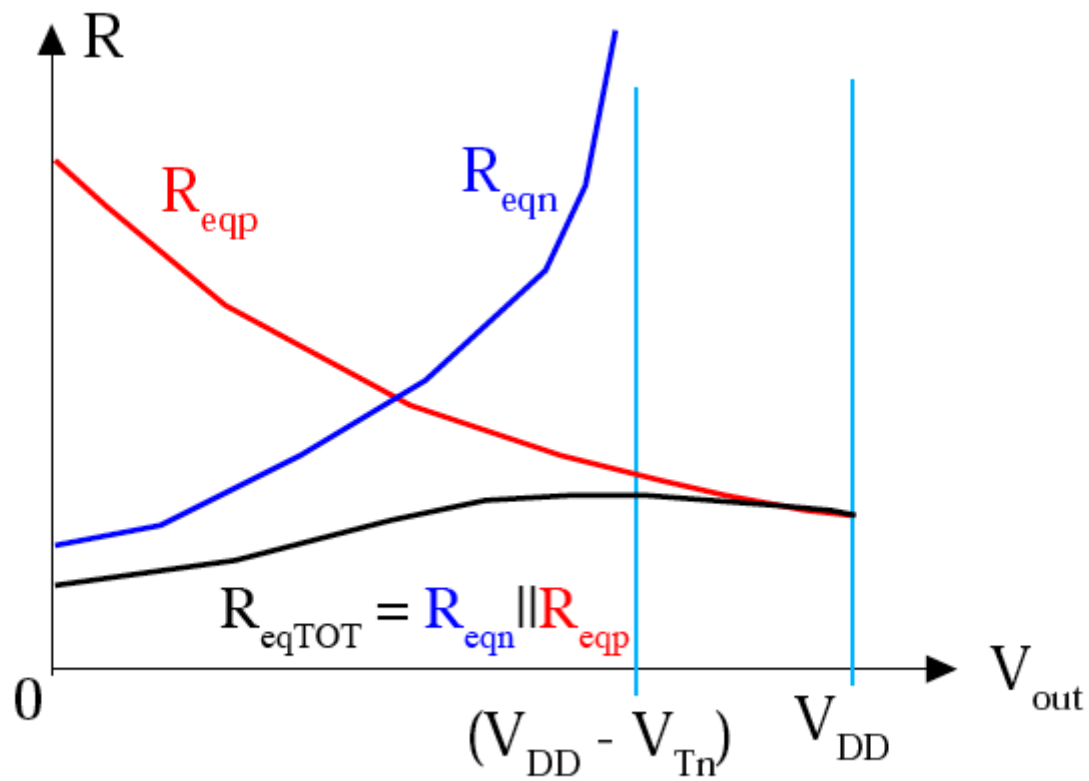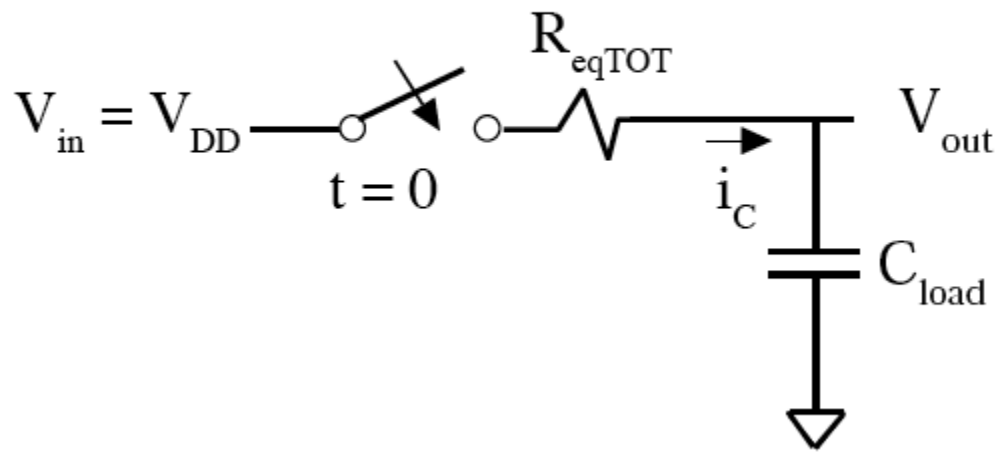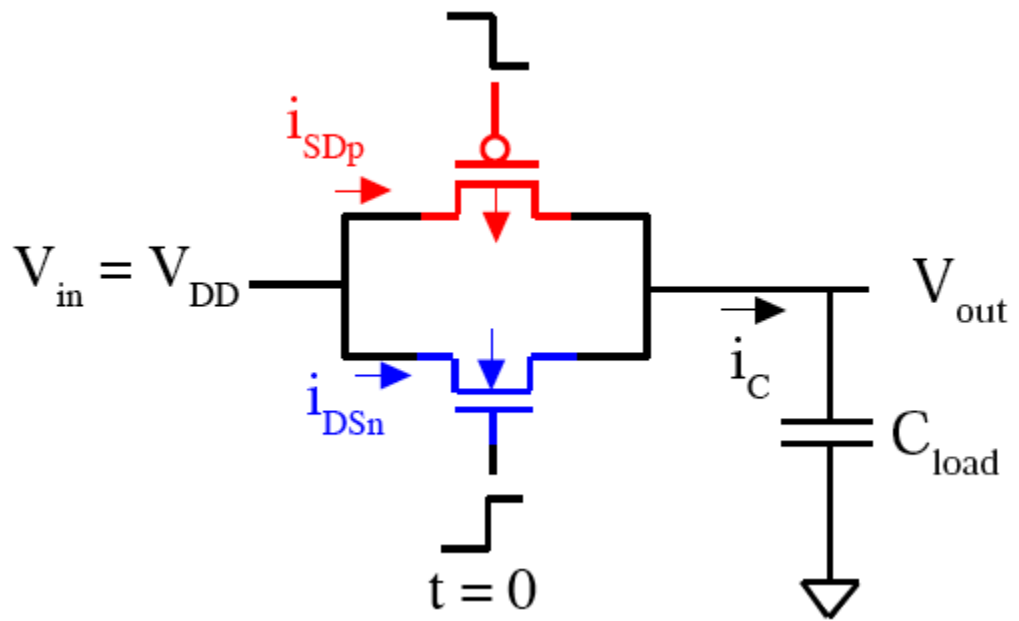
TRANSMISSION GATE LAYOUTS

Simple and small, but no metal lines can pass horizontally

poly used to achieve horizontal metal1 transparency

metal2 used to achieve horizontal metal1 transparency

Routing Gate Signals to Transmission Gate
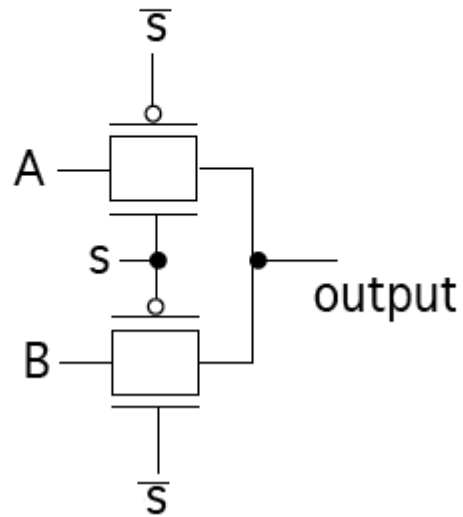
horizontal, via metal1

vertical, via poly

vertical, via metal1 straps
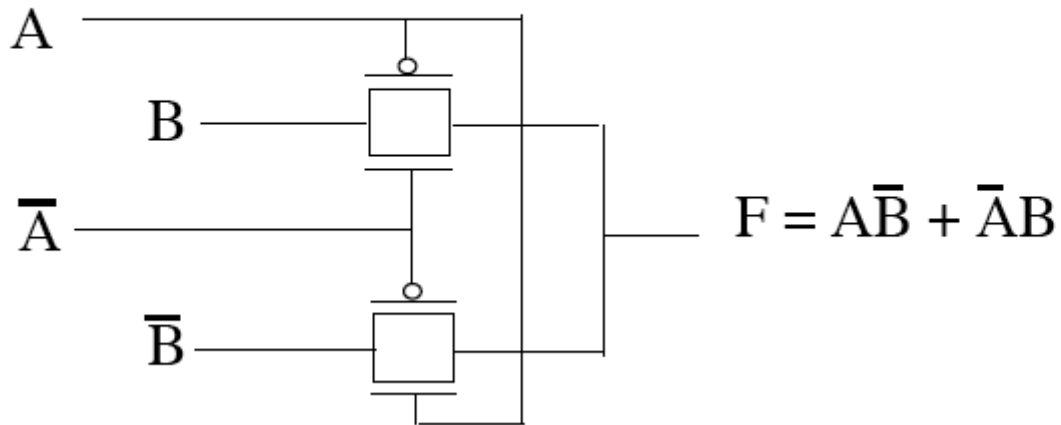
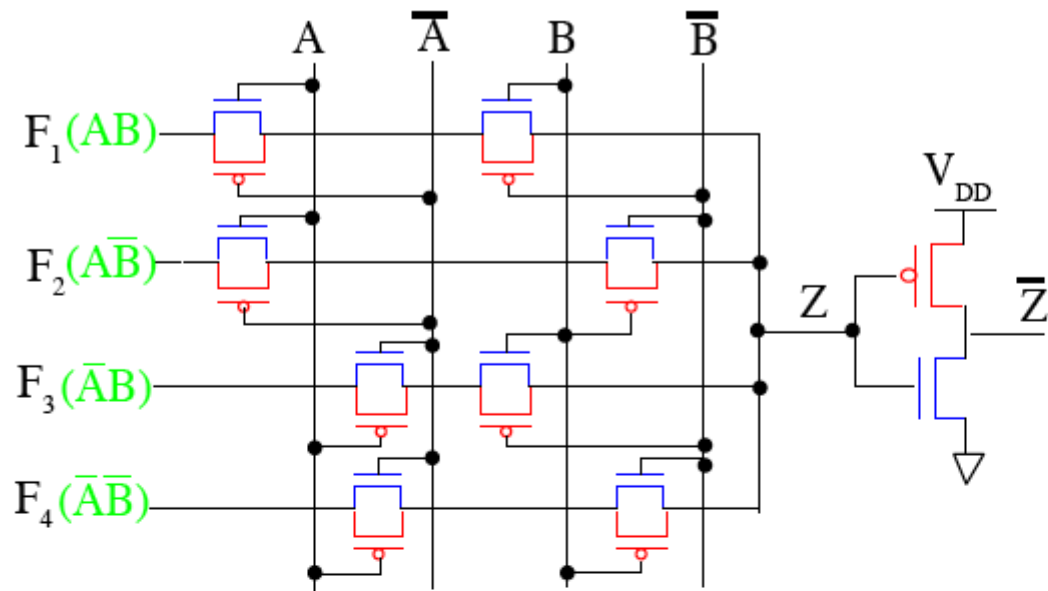metal2 used to achieve vertical metal1 transparency

n⁺
Poly
p⁺
Metal 1
Metal 2
Contact/via

2-INPUT MULTIPLEXER

$$\text{output} = A.s + B.\bar{s}$$

A	B	s	$\bar{s}$	output
x	0	0	1	0 (B)
x	1	0	1	1 (B)
0	x	1	0	0 (A)
1	x	1	0	1 (A)

A

s

B

output

$\bar{s}$

$\bar{s}$

XOR (COMPLEMENTARY PASS-TRANSISTOR LOGIC OR CPL)

A

B

$\bar{A}$

$\bar{B}$

$$F = A\bar{B} + \bar{A}B$$

SOME OF THE FUNCTIONS REALIZED BY THE
BOOLEAN FUNCTION UNIT (CPL)

OPERATION (Z)	F_1	F_2	F_3	F_4
NOR(A,B)	0	0	0	1
XOR(A,B)	0	1	1	0
NAND(A,B)	0	1	1	1
AND(A,B)	1	0	0	0
OR(A,B)	1	1	1	0