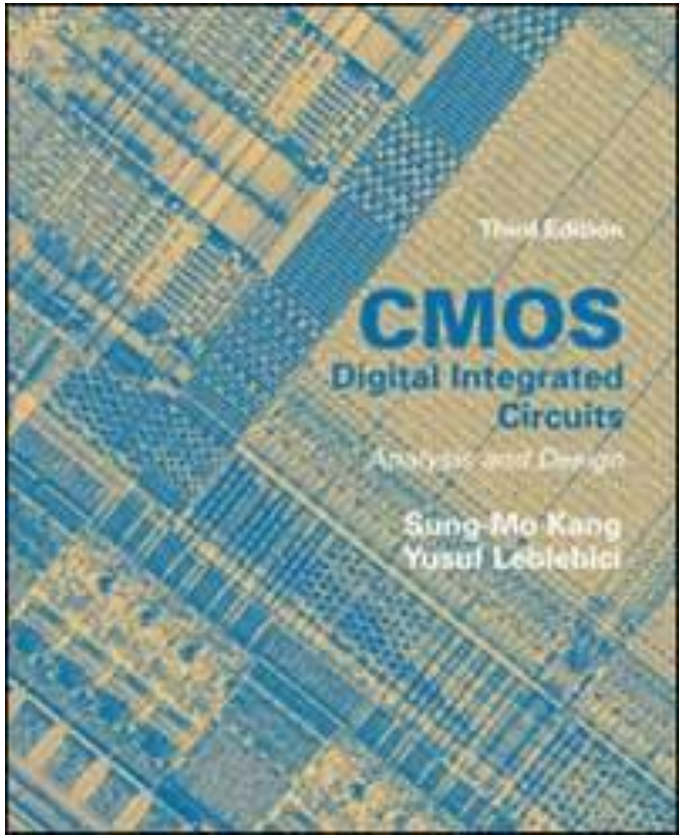
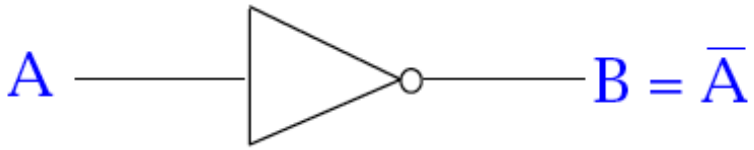
Digital IC Design and Architecture

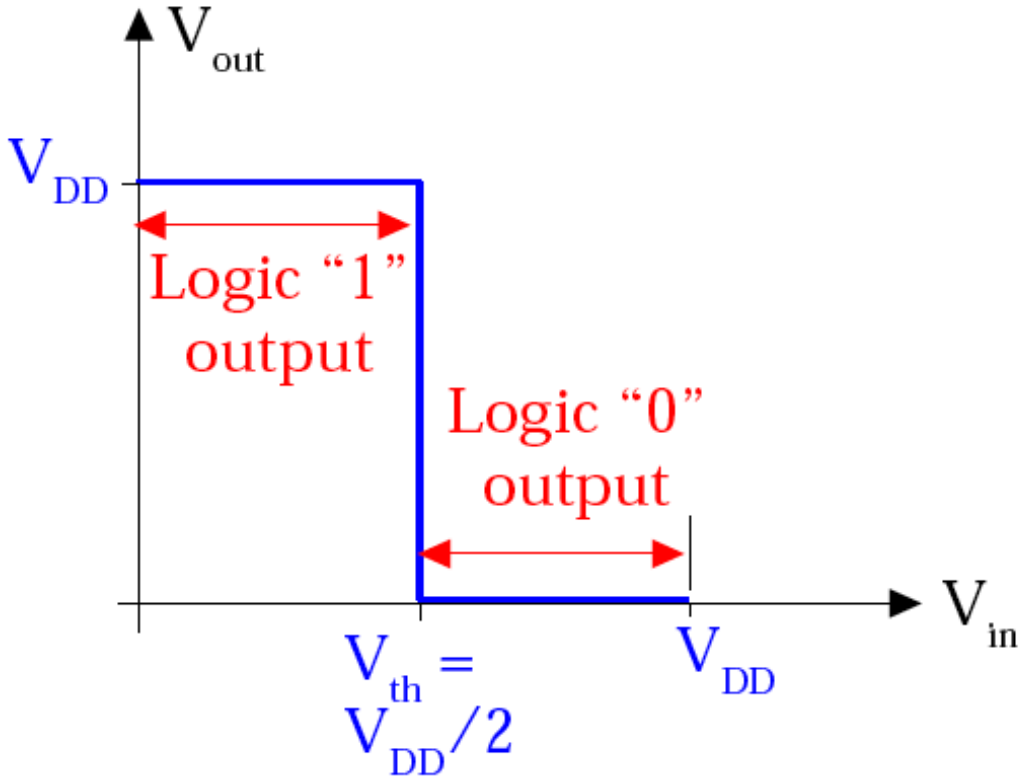


MOS Inverter
Static Characteristics

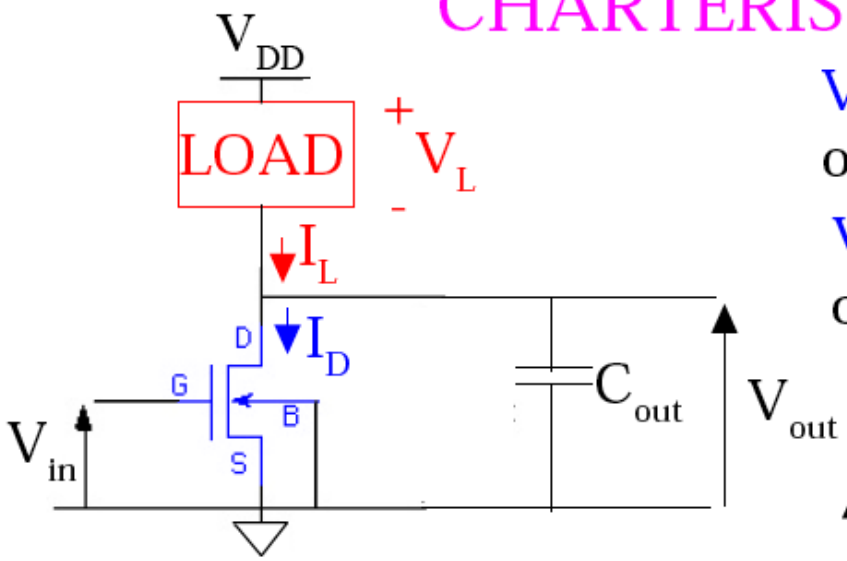
IDEAL INVERTER VOLTAGE TRANSFER CHARTERISTIC (VTC)



A	B
0	1
1	0



ACTUAL INVERTER VOLTAGE TRANSFER CHARTERISTIC (VTC)

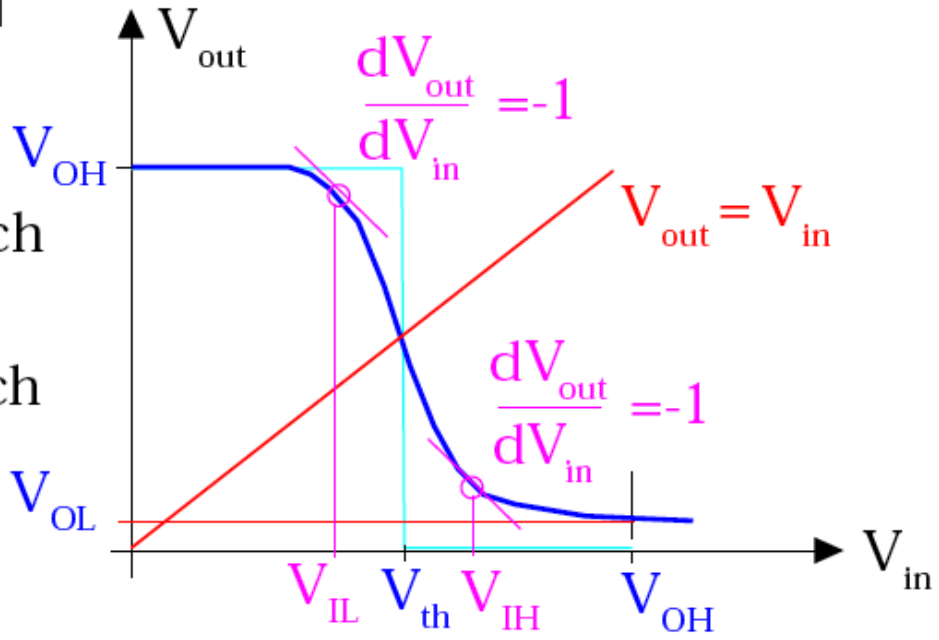


V_{OH} -> max output voltage when output is "1"

V_{OL} -> min output voltage when output is "0"

V_{IL} -> max input voltage which can be interpreted as "0"

V_{IH} -> min input voltage which can be interpreted as "1"



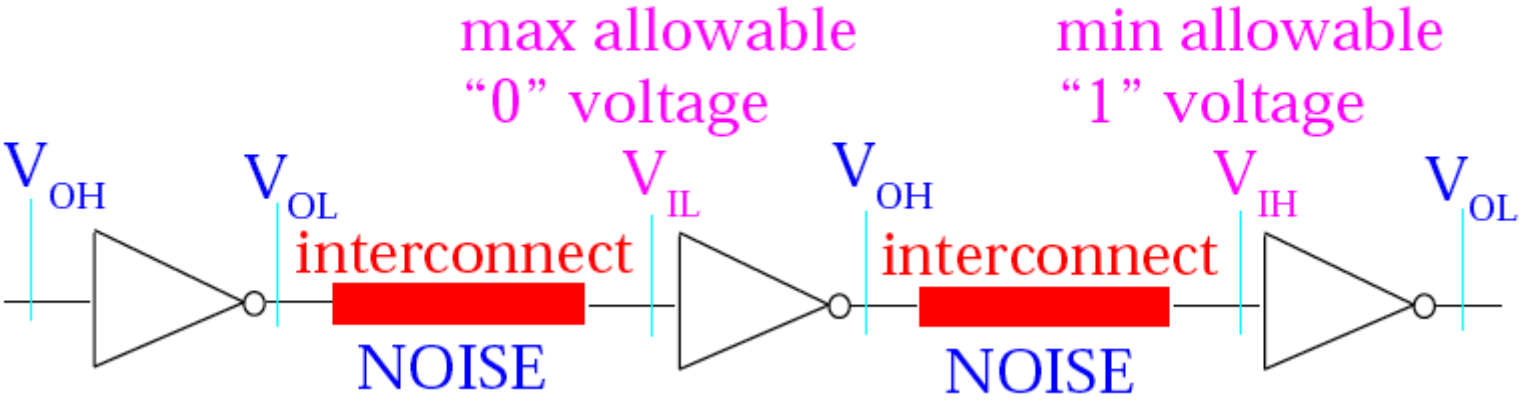
NOISE IMMUNITY AND NOISE MARGINS

V_{OH} -> max output voltage when output is "1"

V_{OL} -> min output voltage when output is "0"

V_{IL} -> max input voltage which can be interpreted as "0"

V_{IH} -> min input voltage which can be interpreted as "1"



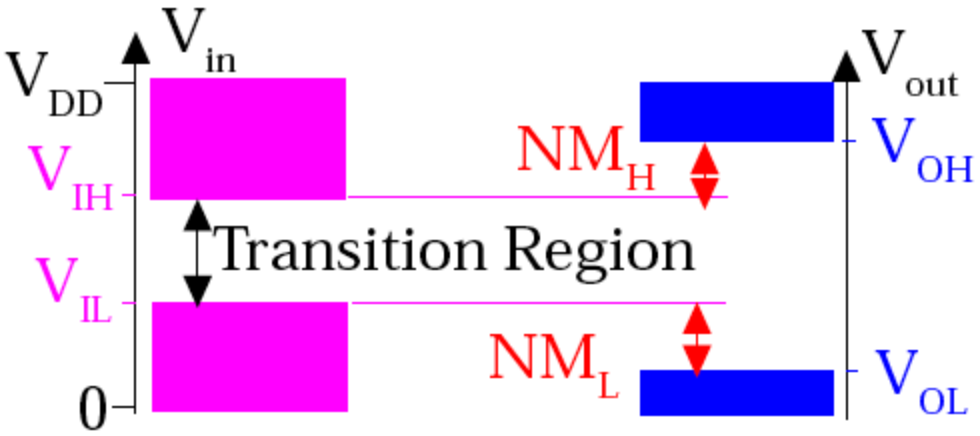
NOISE IMMUNITY AND NOISE MARGINS

V_{OH} -> max output voltage when output is "1"

V_{OL} -> min output voltage when output is "0"

V_{IL} -> max input voltage which can be interpreted as "0"

V_{IH} -> min input voltage which can be interpreted as "1"



$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

JUSTIFICATION FOR V_{IL}, V_{IH}:

LET: $V_{out} = f(V_{in})$, $V'_{out} = f(V_{in} + \Delta V_{noise})$

$$V'_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \Delta V_{noise} + H.O.term \rightarrow 0$$

Using first-order Taylor series expansion

Perturbed Output = Nominal Output + Gain x Ext. Perturbation

FIVE CRITICAL VOLTAGES: V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th} determine:

--> DC Output Voltage Behavior

--> Noise Margins

--> Width and Location of Transition Region

POWER DISSIPATION AND DIE AREA

Power Dissipation -> HEAT

$$T_j = T_a + \Theta P$$

T_j -> junction Temp

T_a -> ambient Temp

Θ -> Thermal Resistance

P -> Power Dissipated

P --> P_{DC}, $P_{dynamic}$

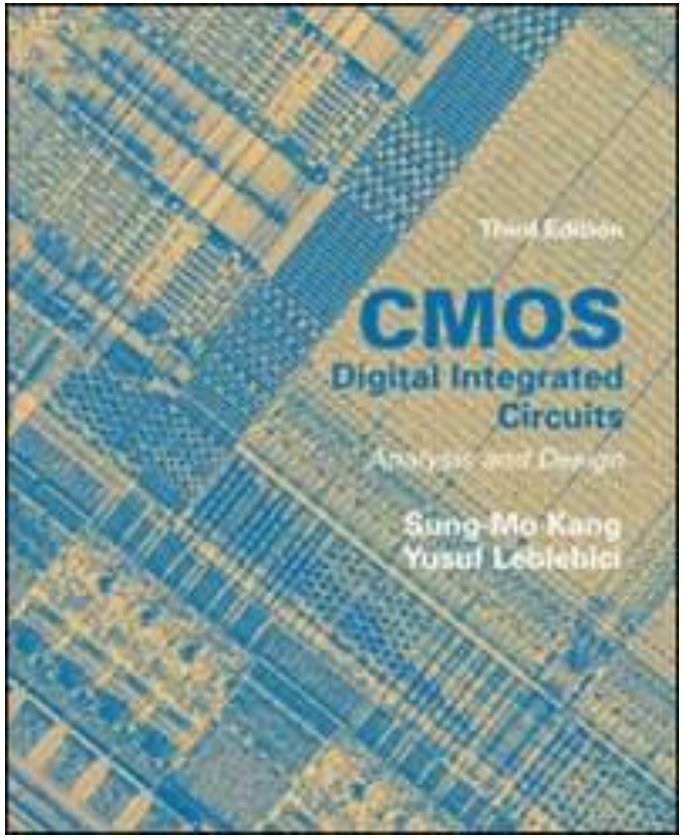
$$P_{DC} = V_{DD} I_{DC}$$

ASSUME: V_{in} = "1" 50% of Op Time, "0" 50% of Op Time

$$P_{DC} = \frac{V_{DD}}{2}\left[I_{DC}(V_{in} = "0") + I_{DC}(V_{in} = "1")\right]$$

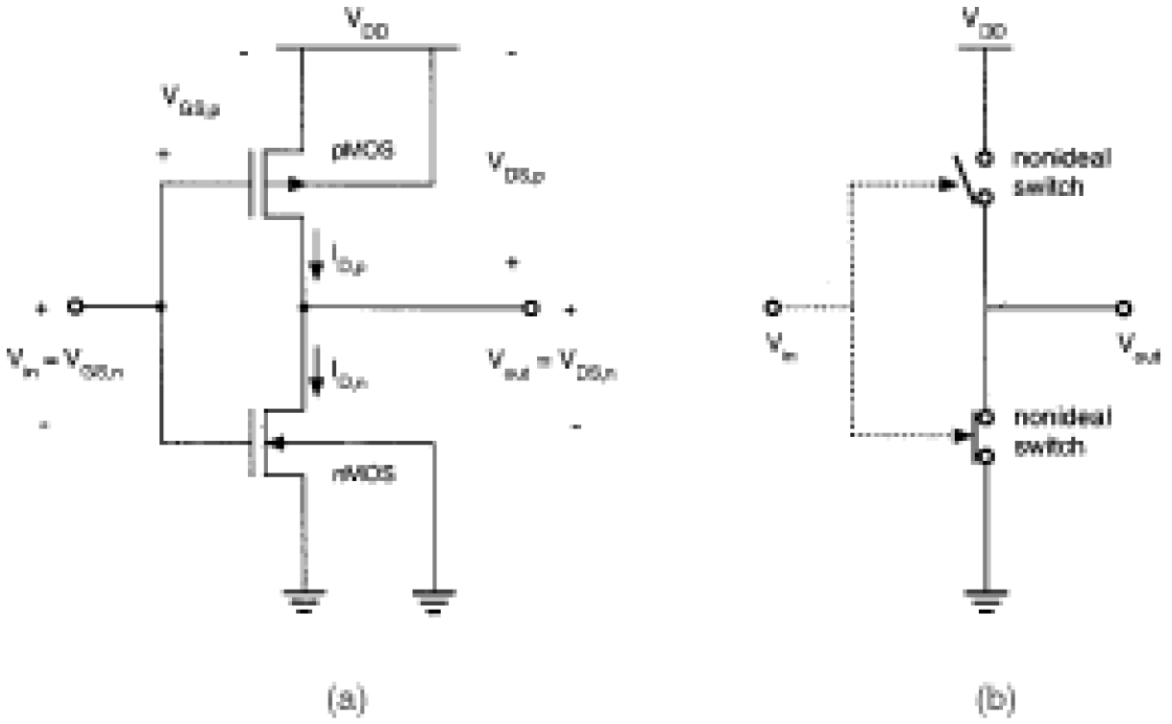
DIE AREA --> MIN W x L and routing --> limited by design rules

Digital IC Design and Architecture

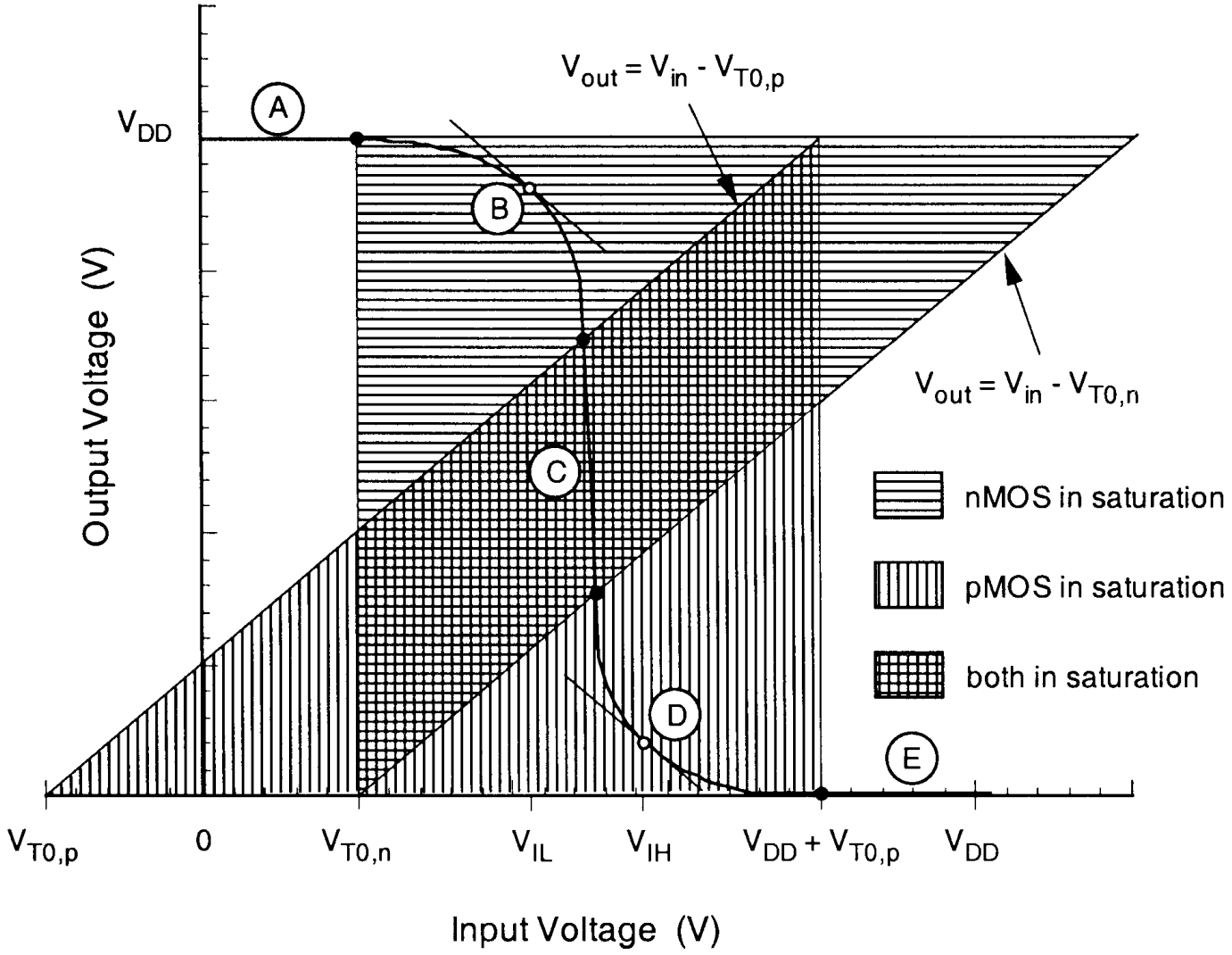


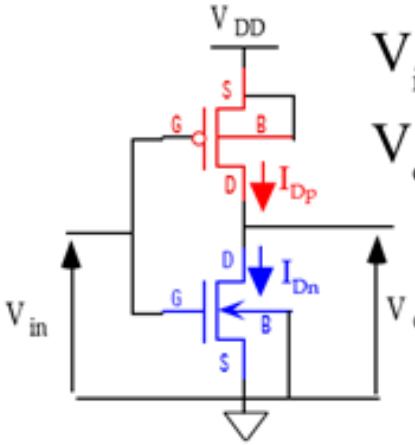
CMOS Inverter

CMOS Inverter Circuit



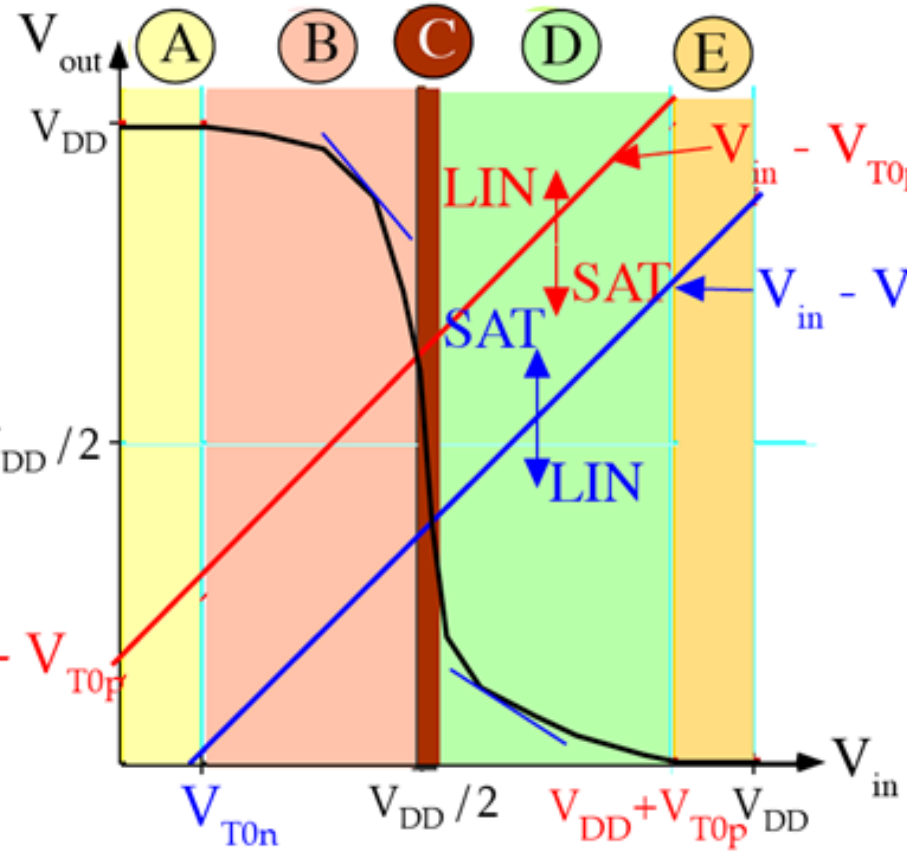
CMOS Inverter Circuit

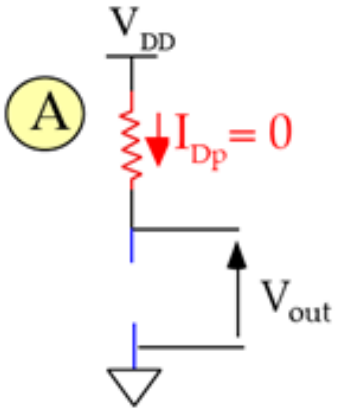


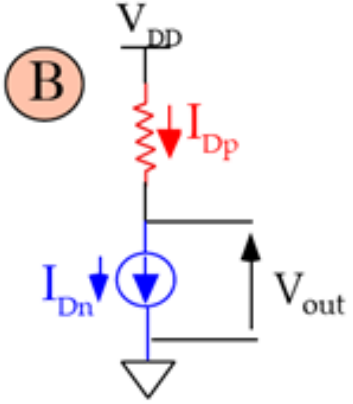


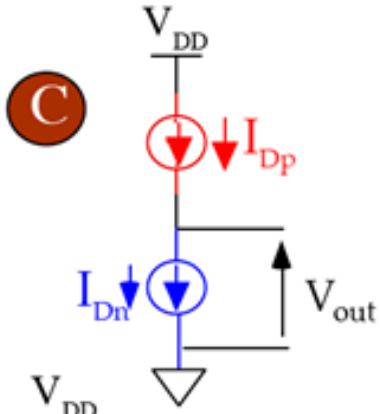
$$V_{in} = V_{gsn} = V_{gsp} + V_{DD}$$

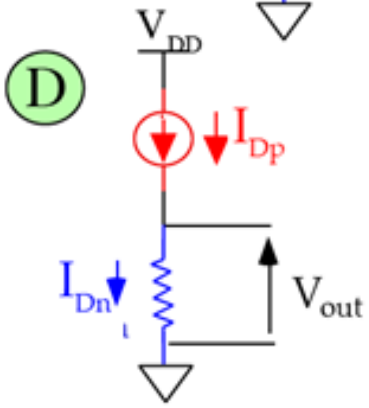
$$V_{out} = V_{dsn} = V_{dsp} + V_{DD}$$

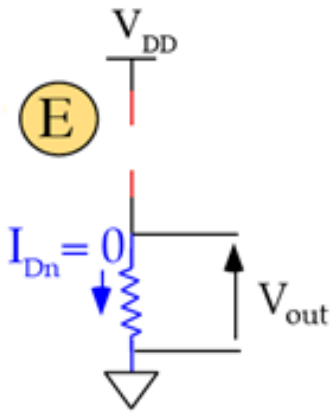




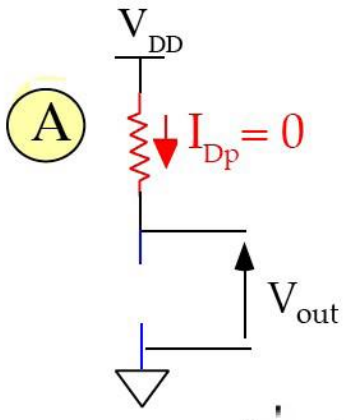








CALCULATE V_{OH}

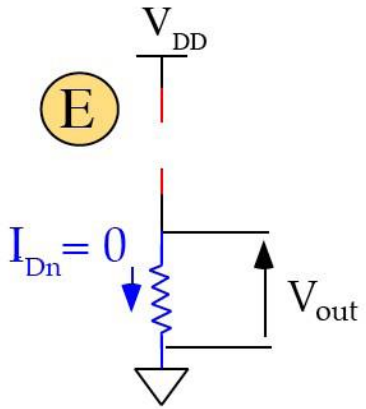


$$I_{Dp} = I_{Dn} = 0$$

$$V_{OH} = V_{DD}$$

$$\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left[2\left(V_{in} - V_{DD} - V_{T0p}\right)\underbrace{\left(V_{out} - V_{DD}\right)}_{0} - \underbrace{\left(V_{out} - V_{DD}\right)^2}_{0}\right] = 0$$

CALCULATE V_{OL}

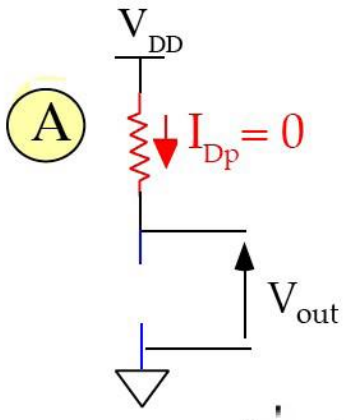


$$I_{Dp} = I_{Dn} = 0$$

$$V_{OL} = 0$$

$$0 = \frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left[2\left(V_{in} - V_{T0n}\right)\underbrace{\left(V_{out}\right)}_{0} - \underbrace{\left(V_{out}\right)^2}_{0}\right]$$

CALCULATE V_{OH}



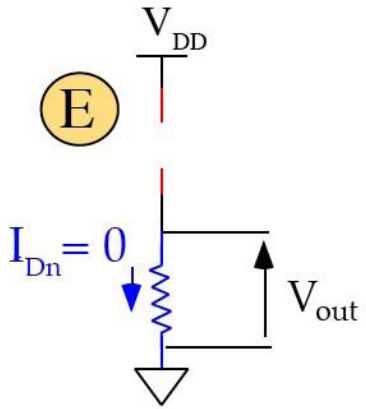
$$I_{Dp} = I_{Dn} = 0$$

- nMOS is off
- pMOS is on and in linear region

$$V_{OH} = V_{DD}$$

$$\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left[2\left(V_{in} - V_{DD} - V_{T0p}\right)\overset{0}{\cancel{\left(V_{out} - V_{DD}\right)}} - \overset{0}{\cancel{\left(V_{out} - V_{DD}\right)^2}}\right] = 0$$

CALCULATE V_{OL}

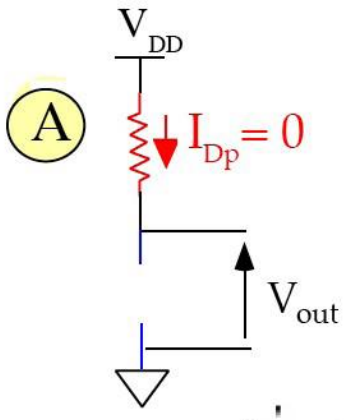


$$I_{Dp} = I_{Dn} = 0$$

$$V_{OL} = 0$$

$$0 = \frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left[2\left(V_{in} - V_{T0n}\right)\overset{0}{\cancel{\left(V_{out}\right)}} - \overset{0}{\cancel{\left(V_{out}\right)^2}}\right]$$

CALCULATE V_{OH}



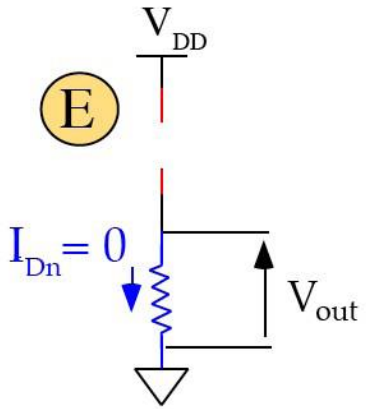
$$I_{Dp} = I_{Dn} = 0$$

- nMOS is off
- pMOS is on and in linear region

$$V_{OH} = V_{DD}$$

$$\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left[2\left(V_{in} - V_{DD} - V_{T0p}\right)\overset{0}{\cancel{\left(V_{out} - V_{DD}\right)}} - \overset{0}{\cancel{\left(V_{out} - V_{DD}\right)^2}}\right] = 0$$

CALCULATE V_{OL}



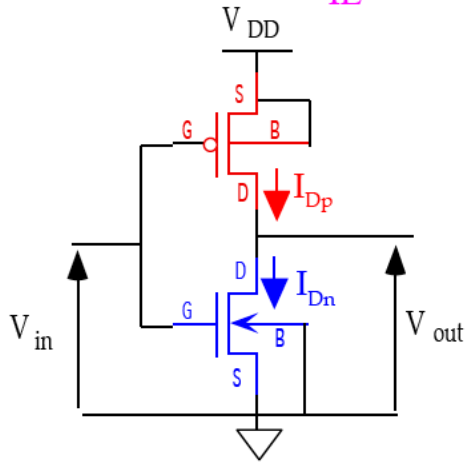
$$I_{Dp} = I_{Dn} = 0$$

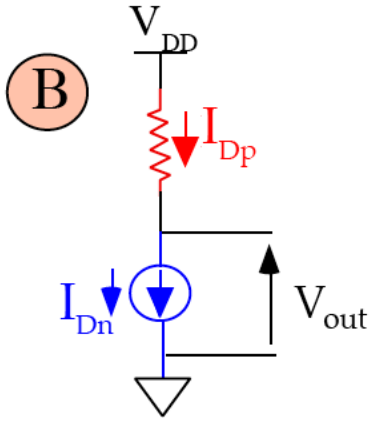
- nMOS is on and in linear region
- pMOS is off

$$V_{OL} = 0$$

$$0 = \frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left[2\left(V_{in} - V_{T0n}\right)\overset{0}{\cancel{\left(V_{out}\right)}} - \overset{0}{\cancel{\left(V_{out}\right)^2}}\right]$$

CALCULATE V_{IL}





$$I_{Dp} = I_{Dn}$$

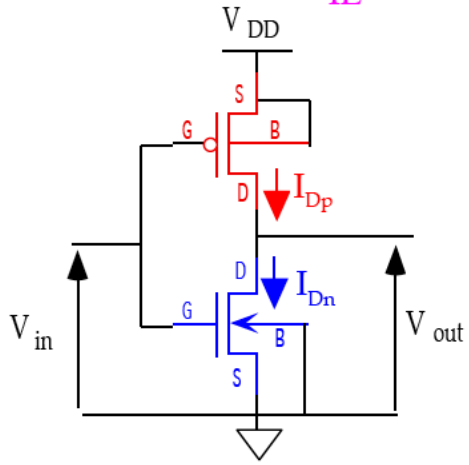
$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{T0\,n})^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2(V_{GSp} - V_{T0\,p})V_{DSp} - V_{DSp}^2\right]$$

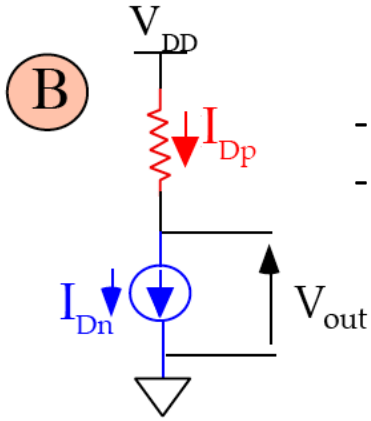
$$V_{GSn} = V_{in},\ V_{GSp} = V_{in} - V_{DD},\ V_{DSp} = V_{out} - V_{DD}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0\,n})^2$$

$$= \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2(V_{in} - V_{DD} - V_{T0\,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

CALCULATE V_{IL}





- nMOS is in saturation region
- pMOS is in linear region

$$I_{Dp} = I_{Dn}$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{T0\,n})^2 = \frac{k'_p}{2}\left(\frac{W}{L}\right)_p \left[2(V_{GSp} - V_{T0\,p})V_{DSp} - V_{DSp}^2\right]$$

$$V_{GSn} = V_{in},\ V_{GSp} = V_{in} - V_{DD},\ V_{DSp} = V_{out} - V_{DD}$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0\,n})^2$$

$$= \frac{k'_p}{2}\left(\frac{W}{L}\right)_p \left[2(V_{in} - V_{DD} - V_{T0\,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0\,n})^2$$

$$= \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2(V_{in} - V_{DD} - V_{T0\,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right] \qquad (5.59)$$

DIFFERENTIATING wrt V_{in}

$$k_n'\left(\frac{W}{L}\right)_n (V_{in} - V_{T0\,n}) = k_p'\left(\frac{W}{L}\right)_p \left[(V_{out} - V_{DD}) + (V_{in} - V_{DD} - V_{T0\,p})\frac{dV_{out}}{dV_{in}}\right.$$

$$\left. -(V_{out} - V_{DD})\frac{dV_{out}}{dV_{in}}\right]$$

($V_{in} \to V_{IL}$; $\frac{dV_{out}}{dV_{in}} \to (-1)$)

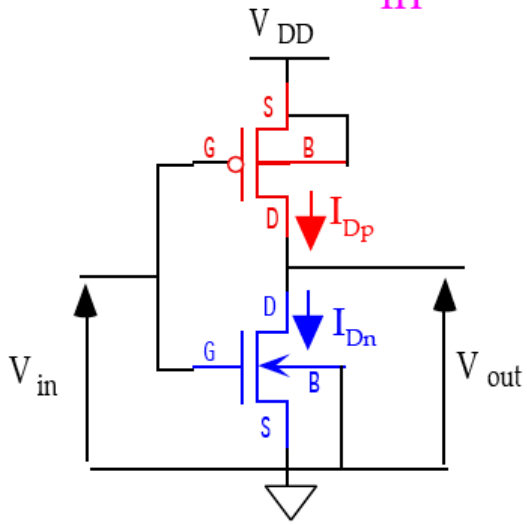
$$k_n'\left(\frac{W}{L}\right)_n (V_{IL} - V_{T0\,n}) = k_p'\left(\frac{W}{L}\right)_p \left[2V_{out} - V_{IL} + V_{T0\,p} - V_{DD}\right]$$

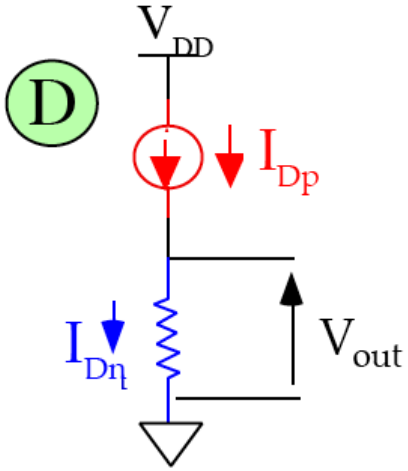
SOLVING FOR V_{IL}

$$V_{IL} = \frac{2V_{out} + V_{T0\,p} - V_{DD} + k_R V_{T0\,n}}{1 + k_R} \qquad \text{where} \quad k_R = \frac{k_n'(W/L)_n}{k_p'(W/L)_p} \qquad (5.62)$$

SOLVE Eqs (5.59) and (5.62) for V_{out} and V_{IL}

CALCULATE V_{IH}





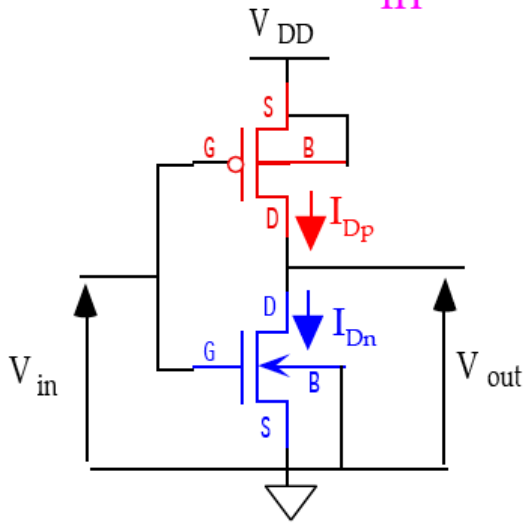
$$I_{Dp} = I_{Dn}$$

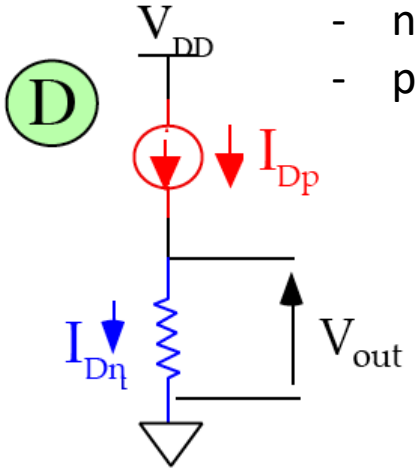
$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{GSn}-V_{T0n})V_{DSn}-V_{DSn}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{GSp}-V_{T0p}\right)^2$$

$$V_{GSn} = V_{in},\ V_{DSn} = V_{out},\ V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0p}\right)^2$$

CALCULATE V_{IH}





- nMOS is in linear region
- pMOS is in saturation region

$$I_{Dp} = I_{Dn}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{GSn}-V_{T0n})V_{DSn}-V_{DSn}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{GSp}-V_{T0p}\right)^2$$

$$V_{GSn} = V_{in},\ V_{DSn} = V_{out},\ V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0p}\right)^2$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0p}\right)^2 \quad (5.64)$$

DIFFERENTIATING wrt V_{in}

$$k_n'\left(\frac{W}{L}\right)_n\left[(V_{in}-V_{T0n})\frac{dV_{out}}{dV_{in}}+V_{out}-V_{out}\frac{dV_{out}}{dV_{in}}\right]=k_p'\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0p}\right)$$

V_{IH} (-1) (-1) V_{IH}

$$k_n'\left(\frac{W}{L}\right)_n\left[-V_{IH}+V_{T0n}+2V_{out}\right]=k_p'\left(\frac{W}{L}\right)_p\left(V_{IH}-V_{DD}-V_{T0p}\right)$$

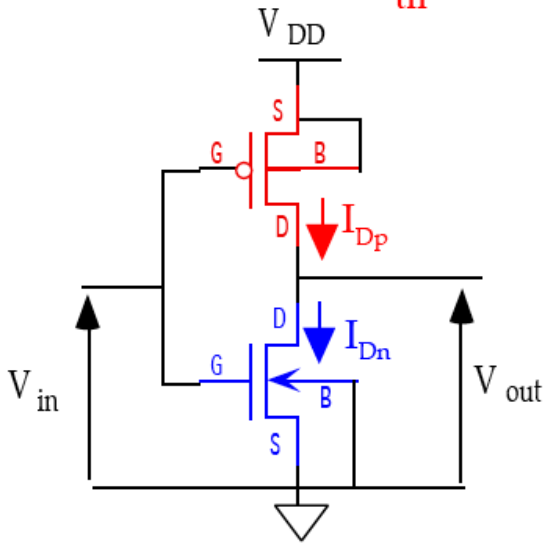
SOLVING FOR V_{IH}

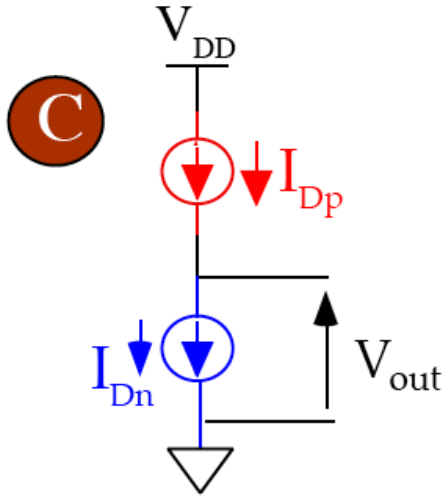
$$V_{IH}=\frac{V_{DD}+V_{T0p}+k_R(2V_{out}+V_{T0n})}{1+k_R} \quad (5.67)$$

where $$k_R=\frac{k_n'(W/L)_n}{k_p'(W/L)_p}$$

SOLVE Eqs. (5.64) and (5.67) for V_{out} and V_{IH}

CALCULATE V_{th}





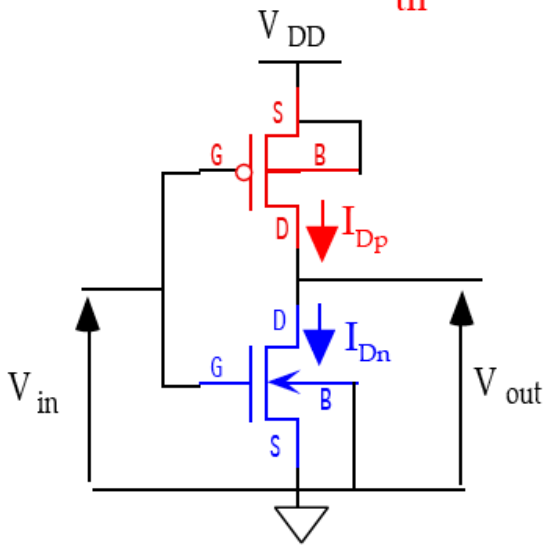
$$I_{Dp} = I_{Dn}$$

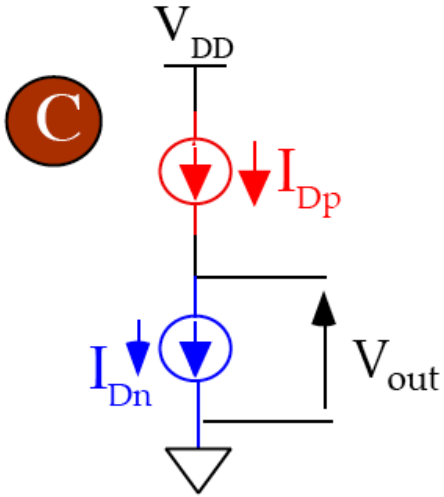
$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{T0\,n})^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p (V_{GSp} - V_{T0\,p})^2$$

$$V_{GSn} = V_{in},\ V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0\,n})^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p (V_{in} - V_{DD} - V_{T0\,p})^2$$

CALCULATE V_{th}





- nMOS is in saturation region
- pMOS is in saturation region

$$I_{Dp} = I_{Dn}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{T0n})^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p (V_{GSp} - V_{T0p})^2$$

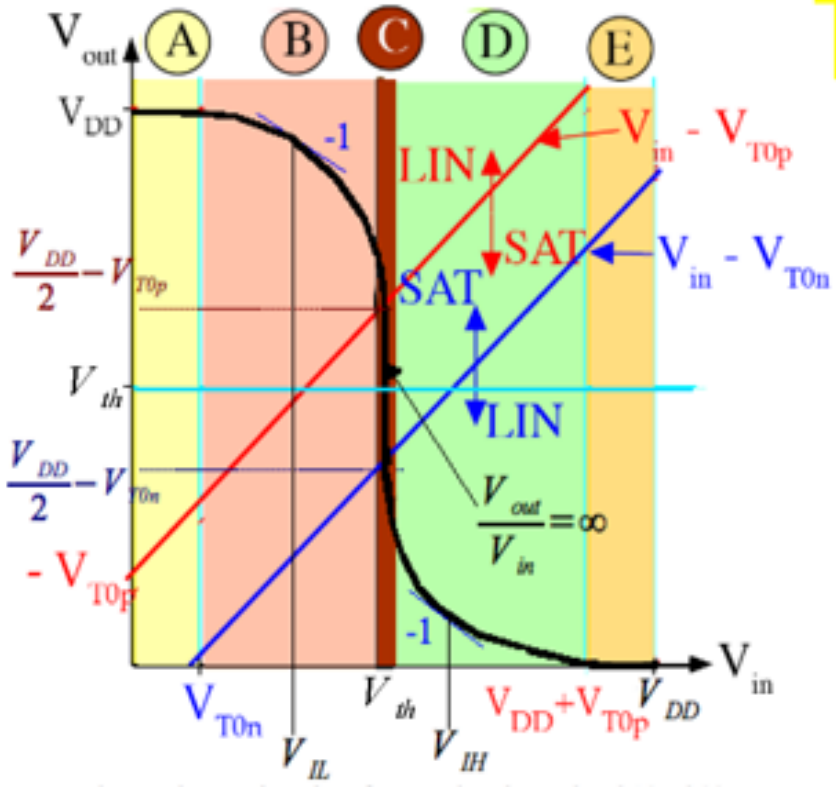
$$V_{GSn} = V_{in},\ V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0n})^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p (V_{in} - V_{DD} - V_{T0p})^2$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left(V_{in}-V_{T0\,n}\right)^2=\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0\,p}\right)^2$$

SOLVING for $V_{th}=V_{in}$

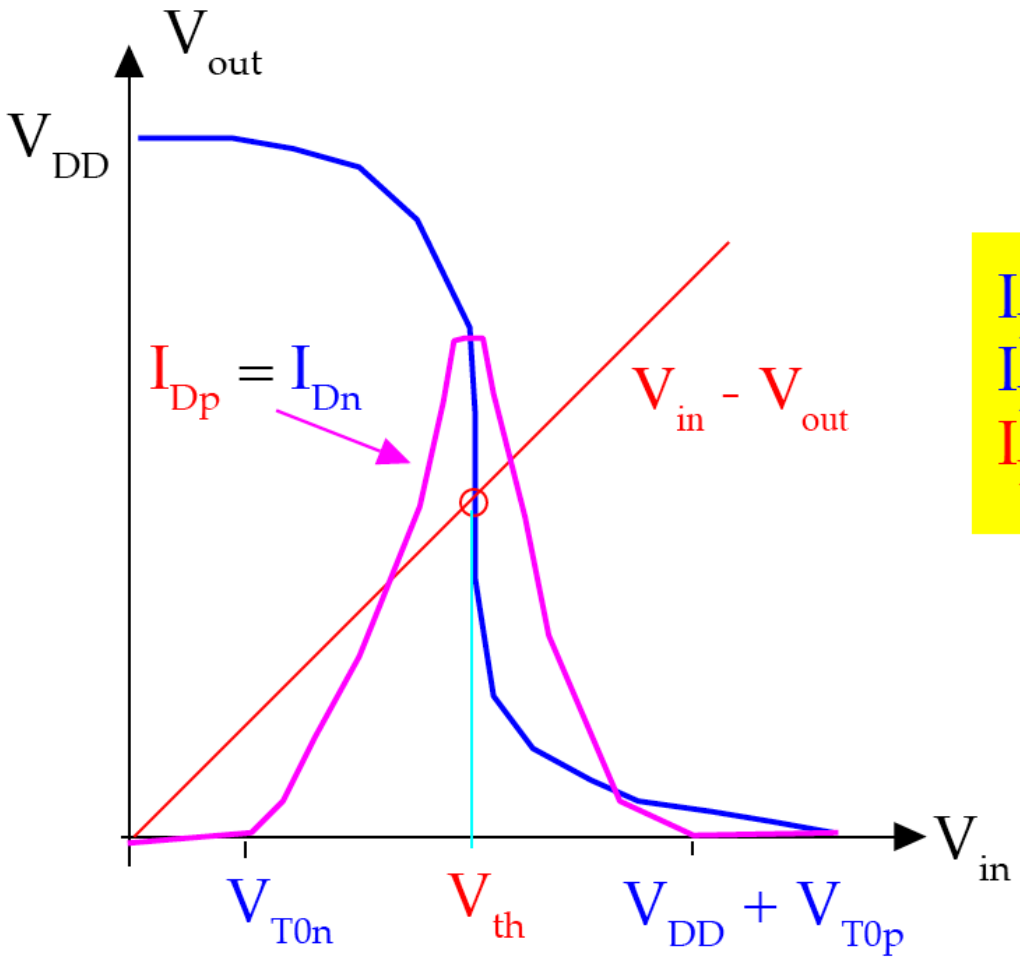
$$V_{in}=V_{th}=\frac{V_{T0\,n}+\sqrt{\frac{1}{k_R}}\left(V_{DD}+V_{T0\,p}\right)}{\left(1+\sqrt{\frac{1}{k_R}}\right)}$$



RECALL THAT

$$V_{th}=V_{in}=V_{out}$$

POWER SUPPLY CURRENT VS V_{IN}

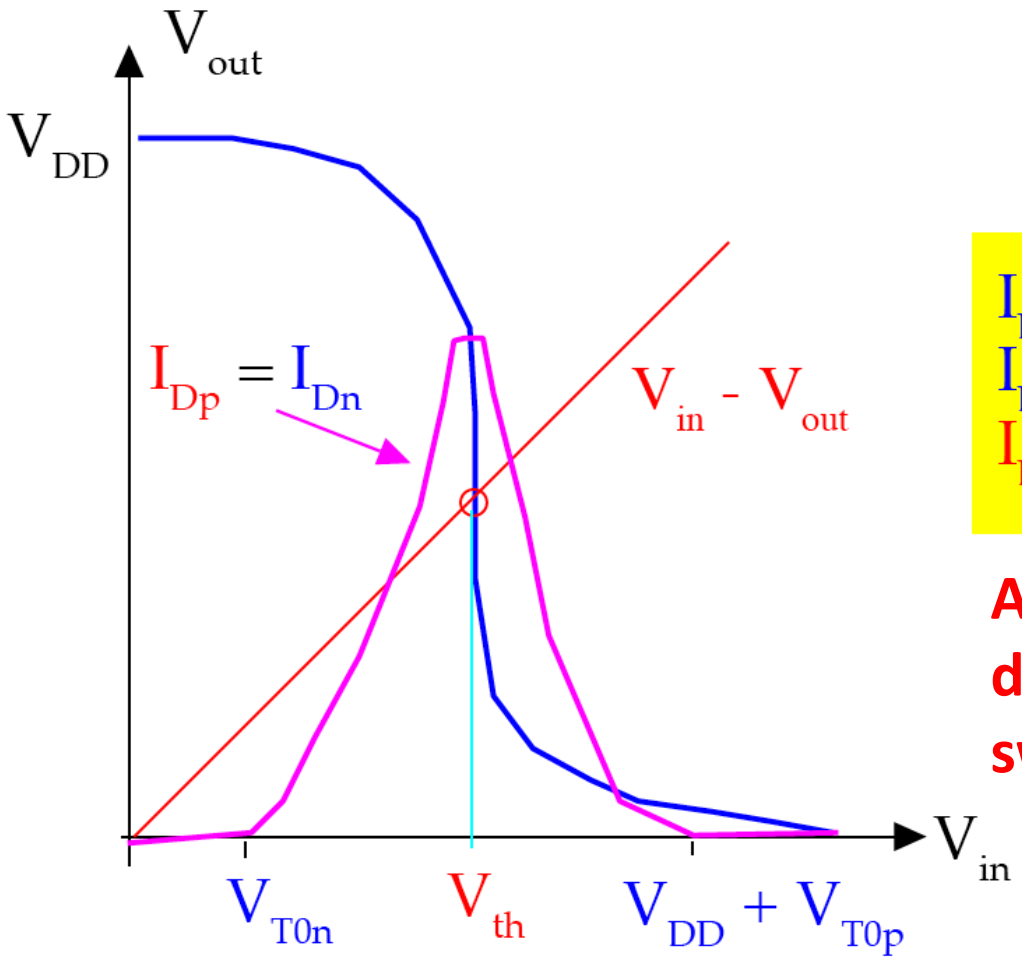


$I_D = 0,\ V_{in} < V_{T0n}$

$I_D = 0,\ V_{in} > V_{DD} + V_{T0p}$

$I_D = MAX,\ V_{in} = V_{th}$

POWER SUPPLY CURRENT VS V_{IN}



$I_D = 0,\ V_{in} < V_{T0n}$

$I_D = 0,\ V_{in} > V_{DD} + V_{T0p}$

$I_D = MAX,\ V_{in} = V_{th}$

Almost all power is dissipated during the switching!

DESIGN OF CMOS INVERTERS

$$V_{in} = V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

SOLVING FOR k_R

$$k_R = \left(\frac{V_{DD} + V_{T0p} - V_{th}}{V_{th} - V_{T0n}}\right)^2$$

FOR IDEAL INVERTER $V_{th} = \frac{1}{2} V_{DD}$

$$(k_R)_{ideal} = \left(\frac{0.5V_{DD} + V_{T0p}}{0.5V_{DD} - V_{T0n}}\right)^2$$

IF $V_{T0} = V_{T0n} = -V_{T0p}$ $\Rightarrow$ $(k_R)_{\text{symmetric inverter}} = 1$

$$k_R = \frac{k_n'(W/L)_n}{k_p'(W/L)_p} = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}$$

FOR SYMMETRIC INVERTER $V_{T0} = V_{T0n} = -V_{T0p}$ $\quad (k_R)_{\text{symmetric inverter}} = 1$

$$\frac{(W/L)_n}{(W/L)_p} = k_R \frac{\mu_p}{\mu_n} \xrightarrow{k_R = 1} \frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n}$$

$$\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n} = \frac{230\,\text{cm}^2/\text{Vs}}{580\,\text{cm}^2/\text{Vs}} \longrightarrow (W/L)_p = 2.5(W/L)_n$$

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{T0})$$ solve eqs. (5.59) and (5.62)

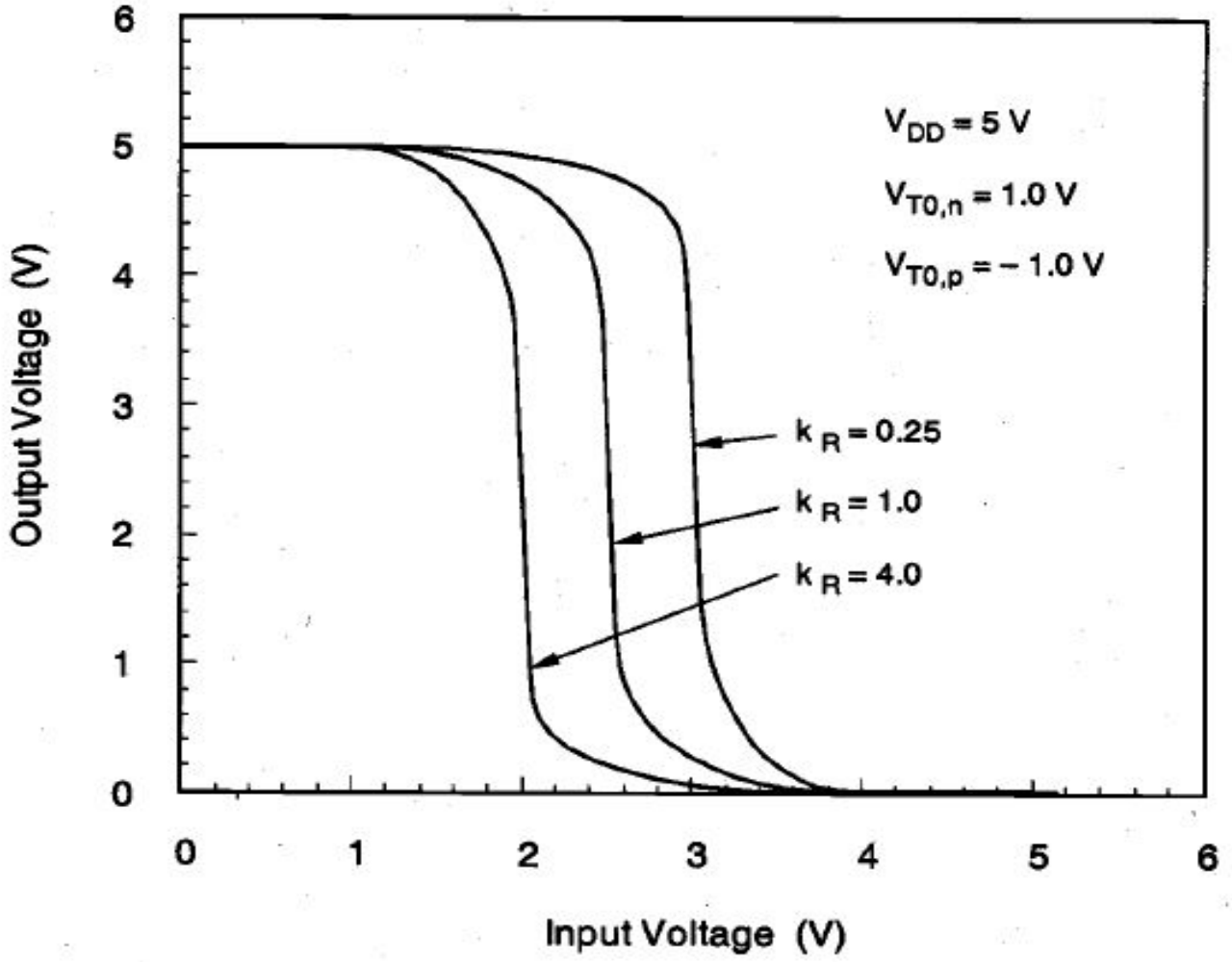
$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_{T0})$$ solve eqs. (5.64) and (5.67)

NOTE: $V_{IL} + V_{IH} = V_{DD}$

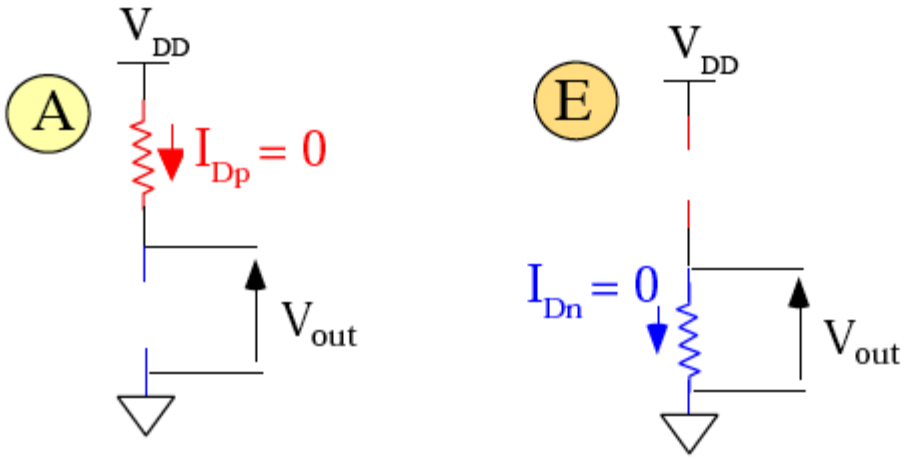
$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = (3/8)V_{DD} + (2/8)V_{T0}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = (3/8)V_{DD} + (2/8)V_{T0}$$

VTC for three CMOS inverters with different nMOS-pMOS ratios



POWER DISSIPATION CONSIDERATIONS



$$P_{DC} = \frac{V_{DD}}{2}\left[I_{DC}(V_{in} = \text{"0"}) + I_{DC}(V_{in} = \text{"1"})\right] = \frac{P(V_{in} = 0) + P(V_{in} = 1)}{2}$$

WHEN $V_{in} = V_{OL}$: $I_L = I_D = 0 \Rightarrow P(V_{in} = 0) = 0$

WHEN $V_{in} = V_{OH}$: $I_L = I_D = 0 \Rightarrow P(V_{in} = 1) = 0$

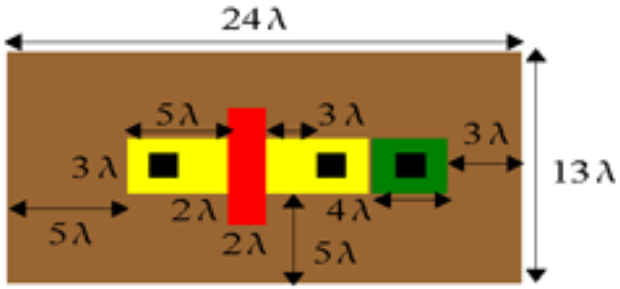
$$P_{DC} = 0$$

Minimum Area MOS Transistor Layouts

COLOR LEGEND

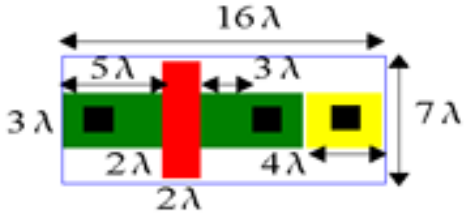
- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

Minimum pMOS Layout

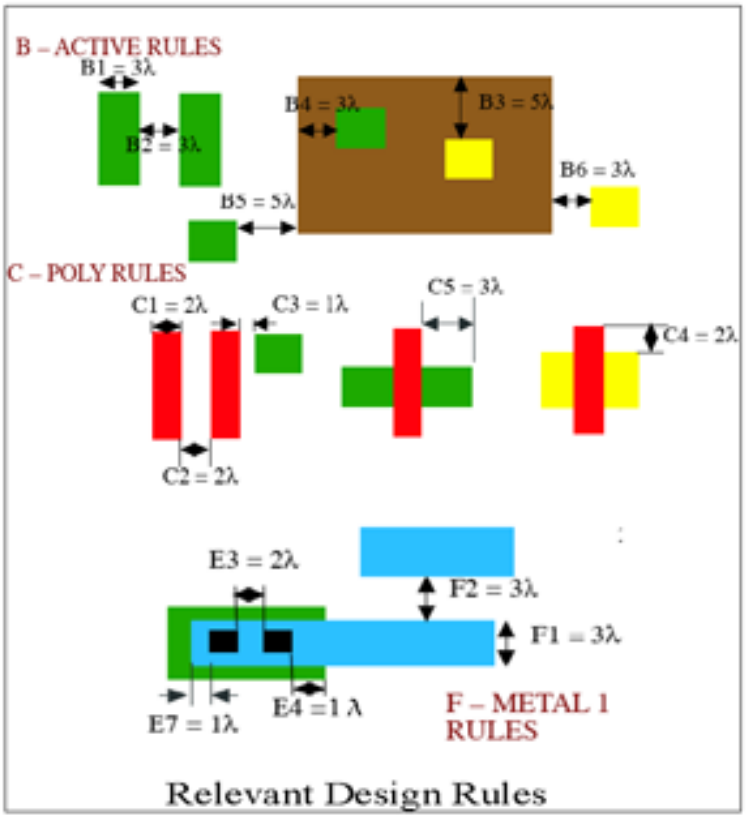


$Area = 24 \cdot 13\lambda^2 = 312\lambda^2$

Minimum nMOS Layout



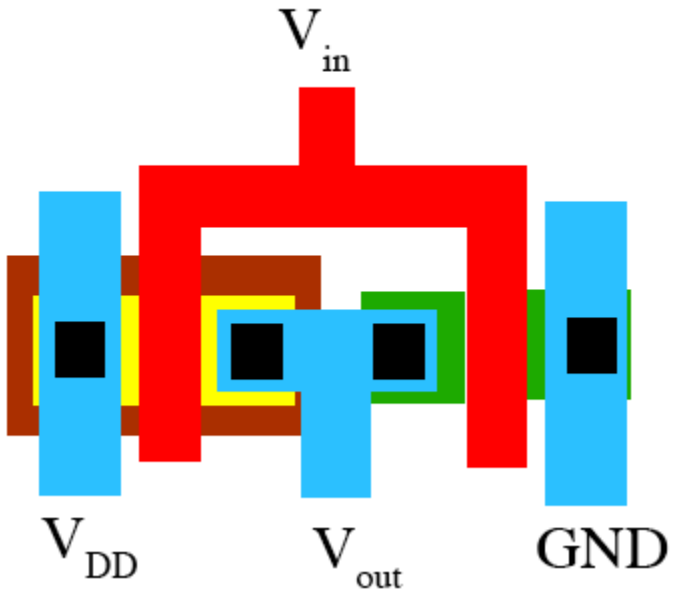
$Area = 16 \cdot 7\lambda^2 = 112\lambda^2$

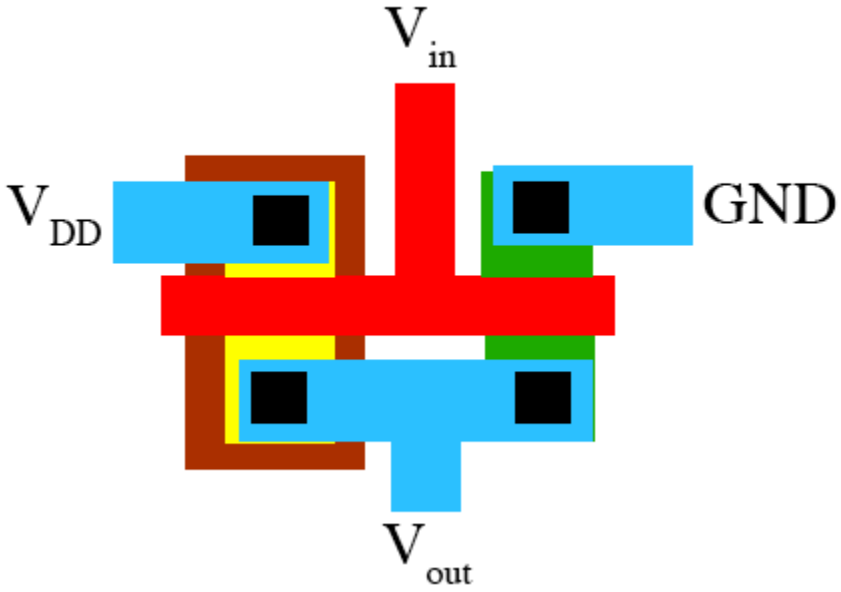


DIE AREA CONSIDERATIONS

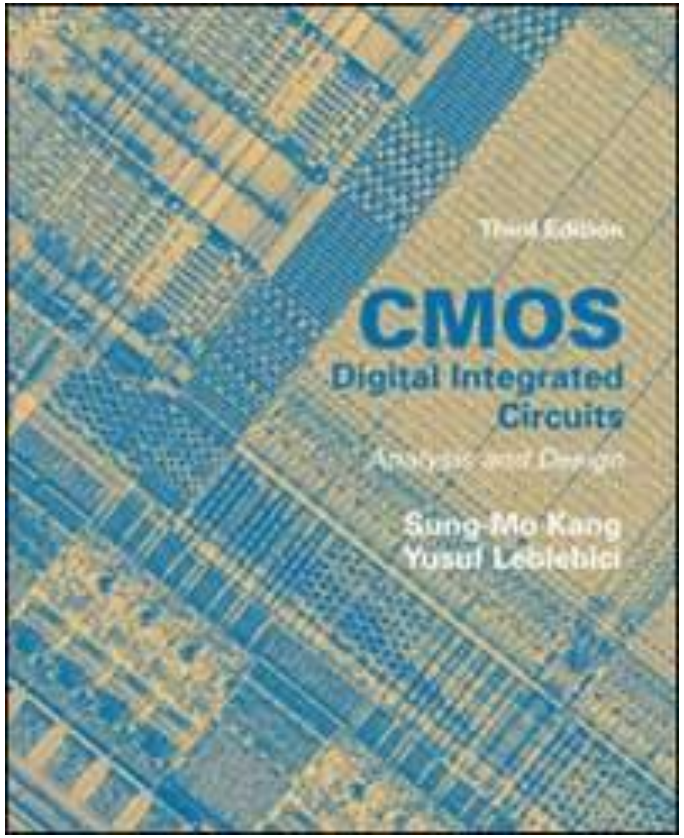
COLOR LEGEND

- n-Well
- n^+
- Polysilicon
- p^+
- Metal 1
- Contact/via



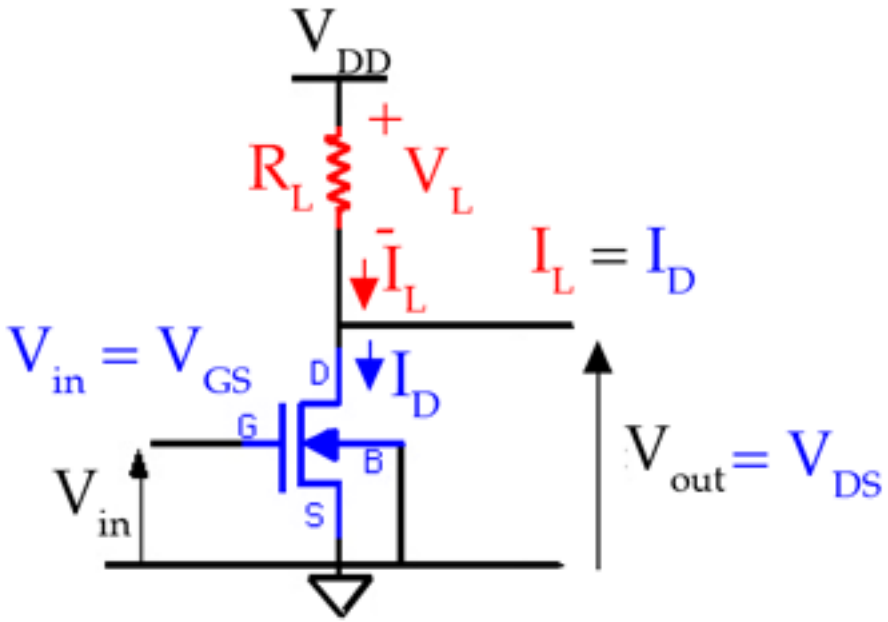


Digital IC Design and Architecture



Resistive Load Inverter

RESISTIVE-LOAD INVERTER



$V_{BS} = 0 \Rightarrow V_{T,n} = V_{T0,n}$

Let (for hand calculations) $\lambda = 0$

CUTOFF: $V_{in} = V_{GS} < V_{T0,n}, \; I_D = 0$

LINEAR: $V_{in} = V_{GS} \geq V_{T0,n}$

$V_{out} = V_{DS} \leq V_{in} - V_{t0,n}$

$$I_D = \frac{k_n}{2}\left[2(V_{in} - V_{T0,n})V_{out} - V_{out}^2\right]$$

SATURATION:

$V_{in} = V_{GS} \geq V_{T0,n}$

$V_{out} = V_{DS} > V_{in} - V_{T0,n}$

$$I_D = \frac{k_n}{2}(V_{in} - V_{T0,n})^2$$

Where: $k_n = \mu_n C_{ox} \frac{W}{L}$

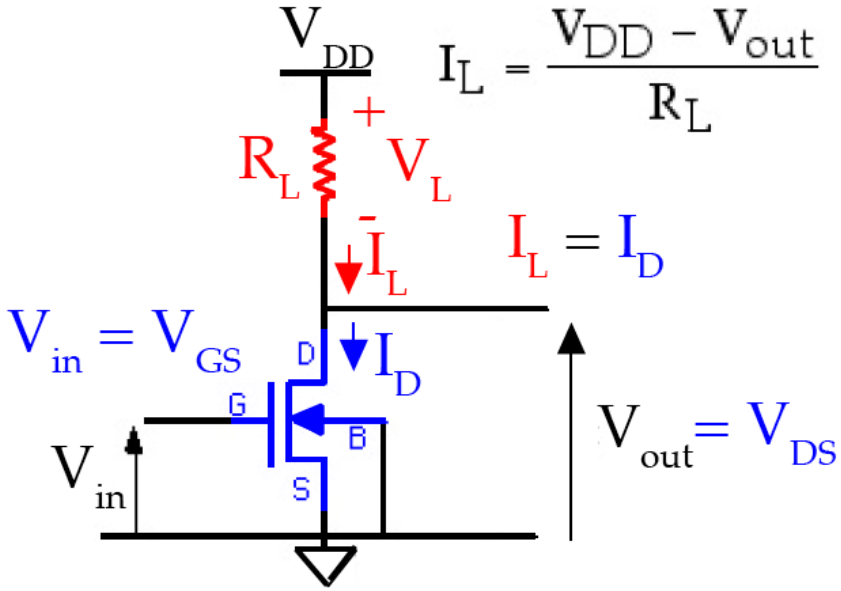
Units

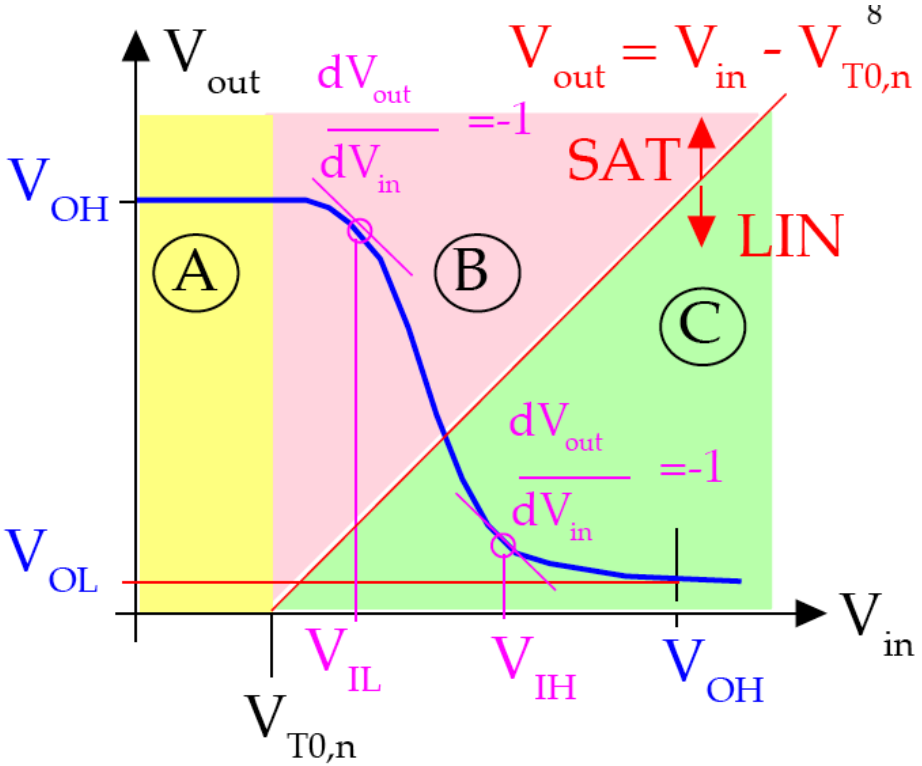
$$k_n = \left(\frac{cm^2}{V\,sec}\right)\left(\frac{F}{cm^2}\right) = \left(\frac{\cancel{cm^2}}{V\,sec}\right)\left(\frac{C}{V\cancel{cm^2}}\right)$$

$$= \left(\frac{C/sec}{V^2}\right) = \frac{A}{V^2}$$

RESISTOR R_L:

$$I_L = \frac{V_{DD} - V_{out}}{R_L}$$



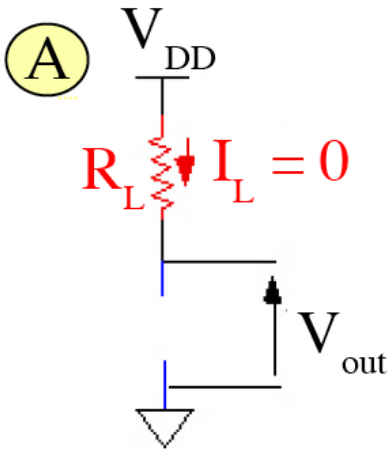


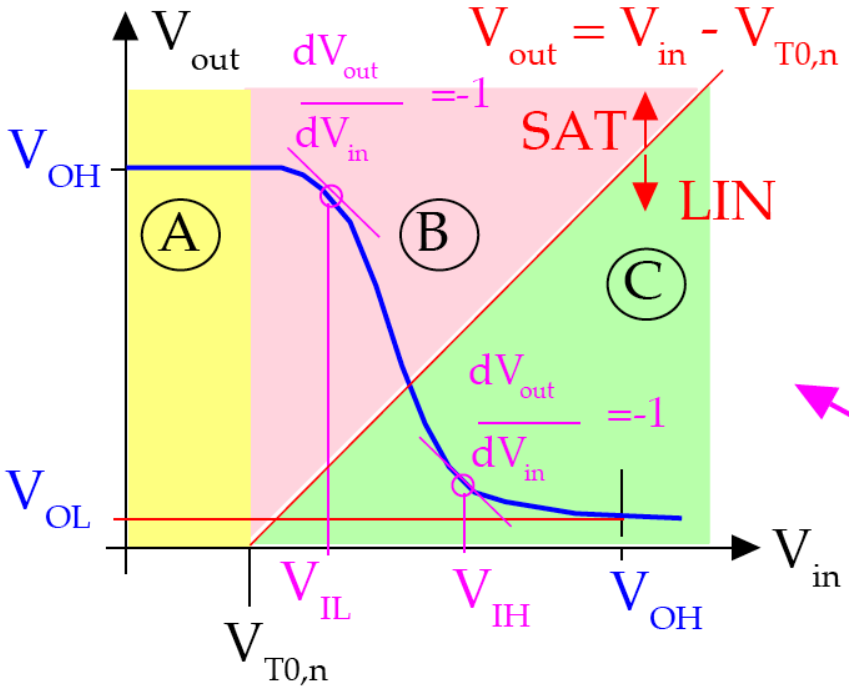
CALCULATION OF V_{OH}: (A)

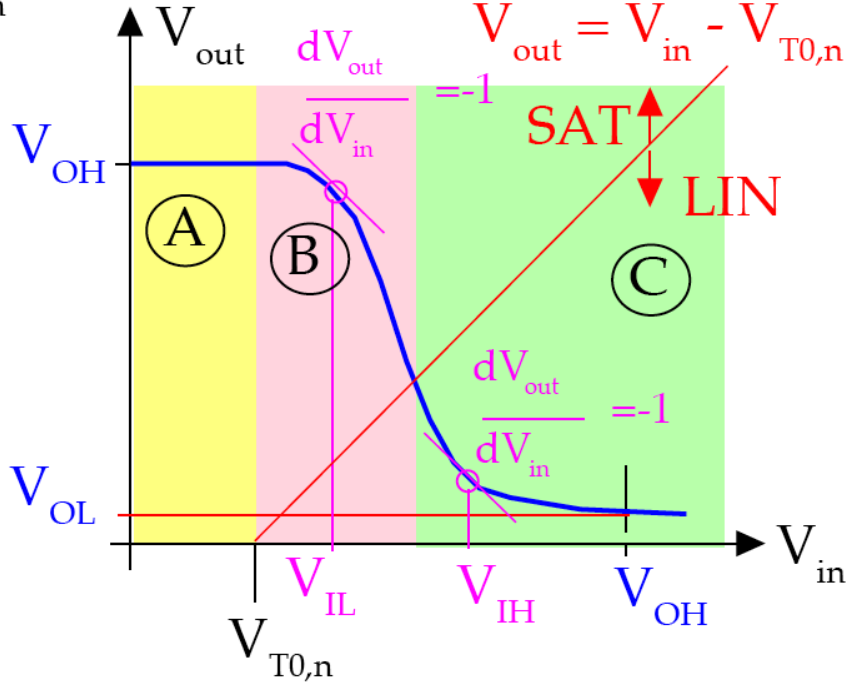
$$V_{out} = V_{DD} - R_L I_L$$

$V_{in} < V_{T0,n}$ => nMOS Cut-off

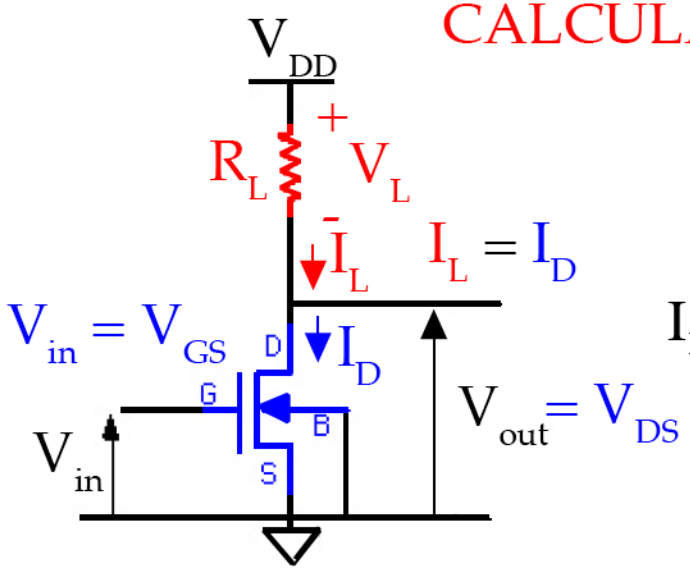
$$I_D = I_L = 0 \Rightarrow V_{OH} = V_{DD}$$




V out
dV out
dV in
=-1
V out = V in - V T0,n
SAT
LIN
V OH
A
B
C
dV out
dV in
=-1
V OL
V in
V IL
V IH
V OH
V T0,n


V out
dV out
dV in
=-1
V out = V in - V T0,n
SAT
LIN
V OH
A
B
C
dV out
dV in
=-1
V OL
V in
V IL
V IH
V OH
V T0,n

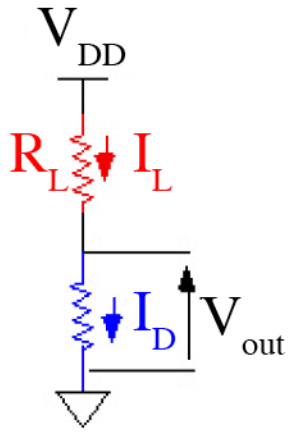
CALCULATION OF V_{OL}: C



$$I_L = \frac{V_{DD} - V_{out}}{R_L}$$

$$I_D = \frac{k_n}{2}\left[2(V_{in} - V_{T0,n})\,V_{out} - V_{out}^2\right]$$

C



$I_L = I_D$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2}\left[2(V_{DD} - V_{T0,n})\,V_{OL} - V_{OL}^2\right]$$

where $V_{in} = V_{OH} = V_{DD}$

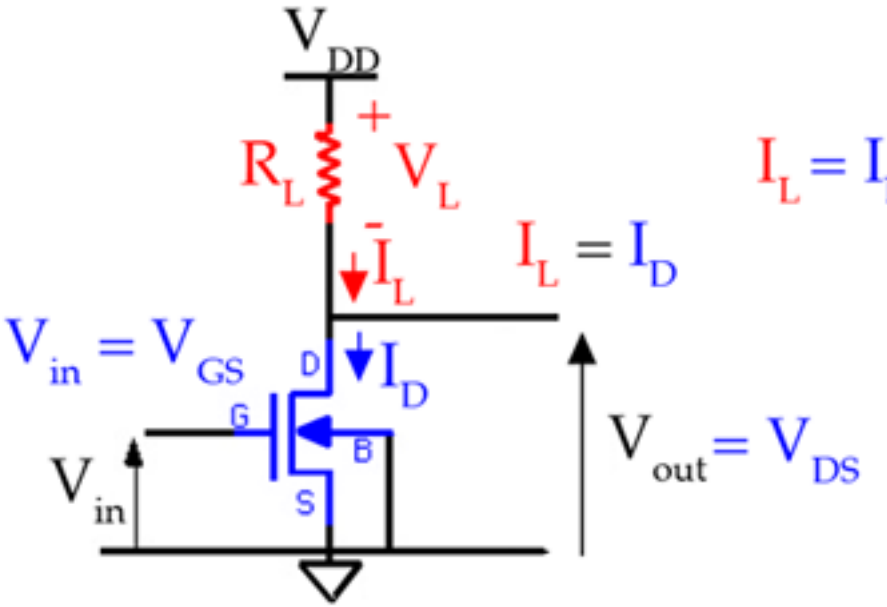
where $V_{out} = V_{OL}$

$$V_{OL}^2 - 2\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)V_{OL} + \frac{2}{k_n R_L}V_{DD} = 0$$

$0 < V_{OL} < V_{T0,n}$

$$V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} \pm \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L}V_{DD}}$$

CALCULATION OF V_{IL}: (B)



$I_L = I_D$ →

$$\frac{V_{DD} - V_{out}(V_{in})}{R_L} = \frac{k_n}{2}(V_{in} - V_{T0,n})^2$$

Differentiate wrt to V_{in}, i.e.

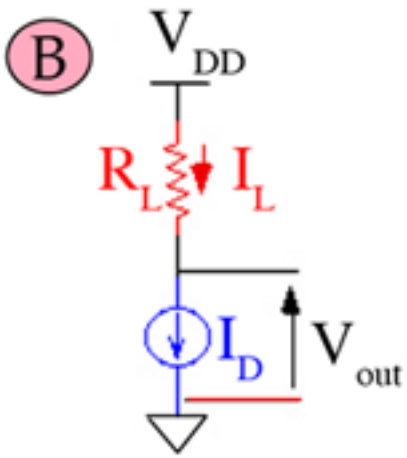
$$-\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = k_n(V_{in} - V_{T0,n})$$

$$\frac{dV_{out}}{dV_{in}} = -1 \quad @\ V_{in} = V_{IL}$$

$$=> V_{out} \approx V_{OH}$$

$$-\frac{1}{R_L}(-1) = k_n(V_{IL} - V_{T0,n})$$

$$V_{IL} = V_{T0,n} + \frac{1}{k_n R_L}$$

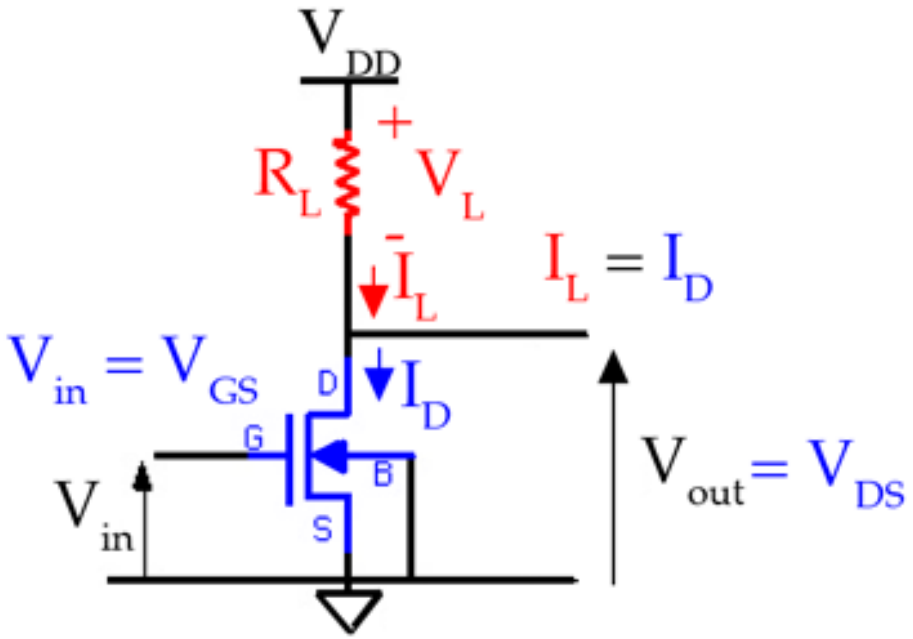


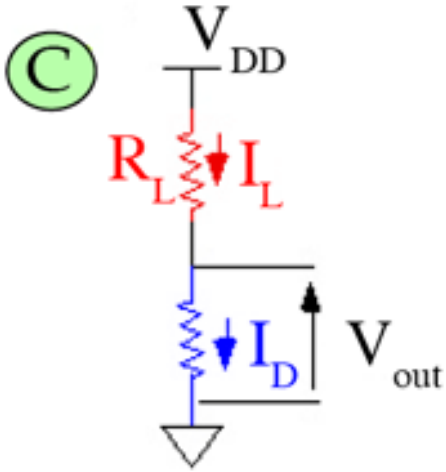
Find V_{out} (when $V_{in} = V_{IL}$):

$$\frac{V_{DD} - V_{out}(V_{in} = V_{IL})}{R_L} = \frac{k_n}{2}(V_{IL} - V_{T0,n})^2$$

$$V_{out}(V_{in} = V_{IL}) = V_{DD} - \frac{1}{2 k_n R_L}$$

CALCULATION OF V_{IH}: C





$$\frac{dV_{out}}{dV_{in}} = -1 \quad @\ V_{in} = V_{IH}$$

$$\Rightarrow V_{out} \approx V_{OL}$$

$$I_L = I_D \rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[2(V_{in} - V_{T0,n})\,V_{out} - V_{out}^2\right]$$

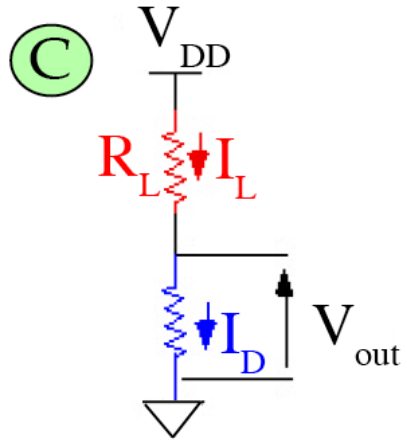
Differentiate wrt to V_{in}, i.e.

$$-\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{k_n}{2}\left[2(V_{in} - V_{T0,n})\frac{dV_{out}}{dV_{in}} + 2\,V_{out} - 2\,V_{out}\frac{dV_{out}}{dV_{in}}\right]$$

$\frac{dV_{out}}{dV_{in}}$: -1 at $V_{in} = V_{IH}$; V_{in}: V_{IH}; $\frac{dV_{out}}{dV_{in}}$: -1; $\frac{dV_{out}}{dV_{in}}$: -1

$$V_{IH} = V_{T0,n} + 2\,V_{out} - \frac{1}{k_n R_L}$$

CALCULATION OF V_{IH}: C



Find $V_{out}(V_{in} = V_{IH})$:

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[2(V_{IH} - V_{T0,n})V_{out} - V_{out}^2\right]$$

where

$$V_{IH} = V_{T0,n} + 2V_{out} - \frac{1}{k_n R_L}$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[2(V_{T0,n} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0,n})V_{out} - V_{out}^2\right]$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[3V_{out}^2 - \frac{2V_{out}}{k_n R_L}\right]$$

$$\frac{V_{DD}}{R_L} = \frac{3}{2}k_n V_{out}^2 \longrightarrow V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

CALCULATION OF V_{th}:

$$V_{in} = V_{out} = V_{th} \Rightarrow V_{DS} = V_{GS} > V_{GS} - V_{T0,n} \longrightarrow \text{B}$$

$$I_L = I_D \rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}(V_{in} - V_{T0,n})^2$$

($V_{out} \rightarrow V_{th}$, $V_{in} \rightarrow V_{th}$)

$$\frac{V_{DD} - V_{th}}{R_L} = \frac{k_n}{2}(V_{th} - V_{T0,n})^2$$

$$V_{th}^2 - 2\left(V_{T0,n} - \frac{1}{k_n R_L}\right)V_{th} + V_{T0,n}^2 - \frac{2V_{DD}}{k_n R_L} = 0$$

$$V_{th} = V_{T0,n} - \frac{1}{k_n R_L} \pm \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

SUMMARY - RESISTIVE LOAD INVERTER

$$V_{th} = V_{T0,n} - \frac{1}{k_n R_L} + \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

$$V_{IL} = V_{T0,n} + \frac{1}{k_n R_L} \qquad V_{out}(V_{in} = V_{IL}) = V_{DD} - \frac{1}{2k_n R_L}$$

$$V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} \qquad V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}}$$

$$V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} \pm \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L}V_{DD}}$$

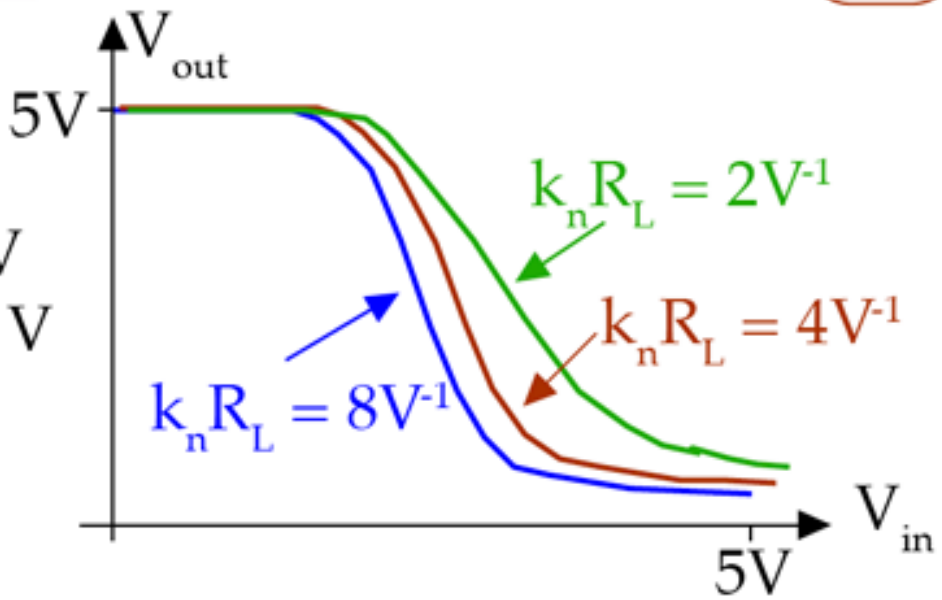
$$V_{OH} = V_{DD}$$

$V_{DD} = 5V$

$V_{T0,n} = 1\ V$

Units

$$k_n R_L = \left(\frac{A}{V^2}\right)\left(\frac{V}{A}\right) = V^{-1}$$

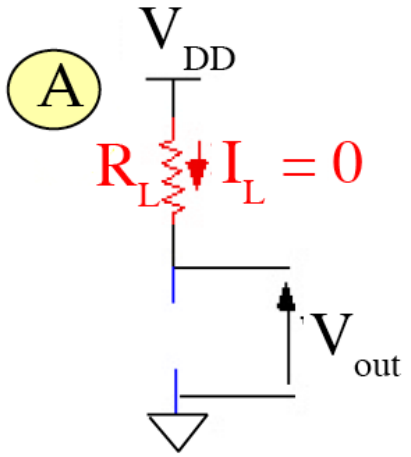


POWER DISSIPATION - RESISTIVE LOAD INVERTER

$$P_{DC} = \frac{V_{DD}}{2}\left[I_{DC}(V_{in} = "0") + I_{DC}(V_{in} = "1")\right]$$

WHEN $V_{in} = V_{OL}$: DRIVER nMOS in CUT-OFF

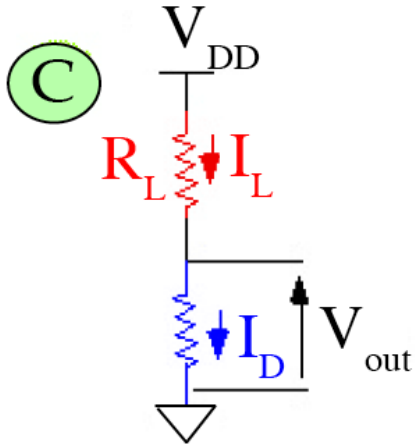
$$I_L = I_D = 0 \Rightarrow P(V_{in} = 0) = 0$$



WHEN $V_{in} = V_{OH}$:

$$I_{DC}(V_{in} = "1") = I_L = I_D = \frac{V_{DD} - V_{OL}}{R_L}$$

$$P(V_{in} = "1") = \frac{V_{DD}}{2}\,\frac{V_{DD} - V_{OL}}{R_L}$$



$$P_{DC}(\text{average}) = \frac{V_{DD}}{2}\,\frac{V_{DD} - V_{OL}}{R_L}$$

Two examples of resistive load inverter layout are shown below:

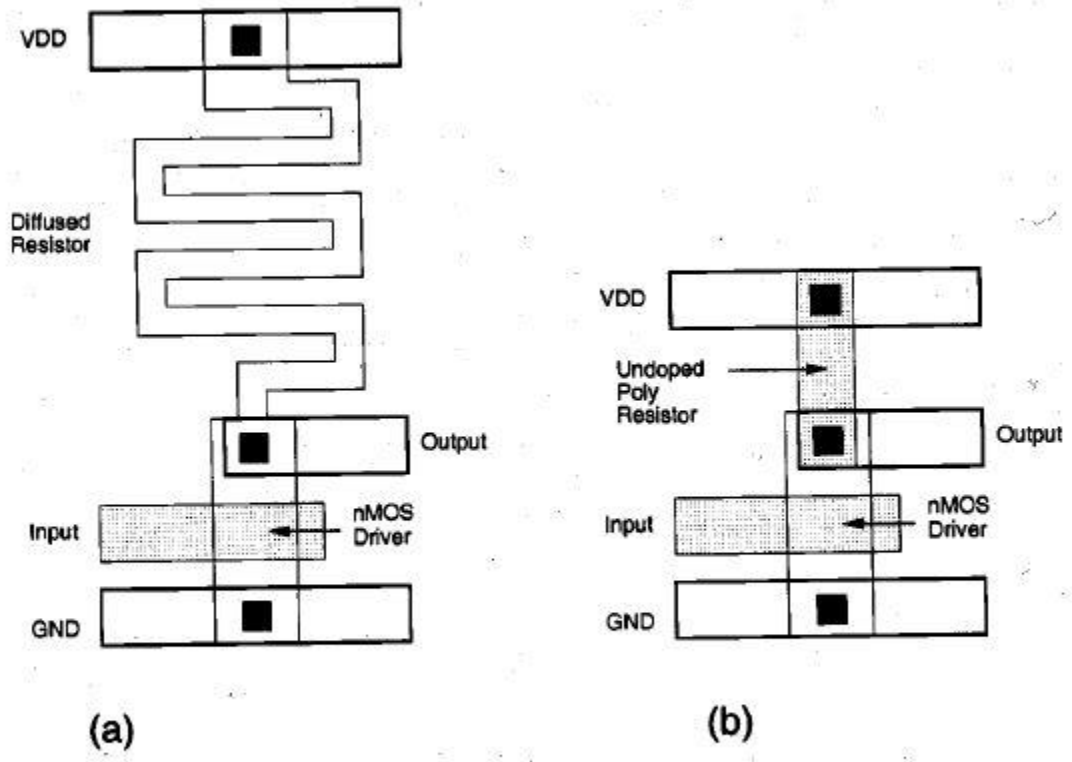
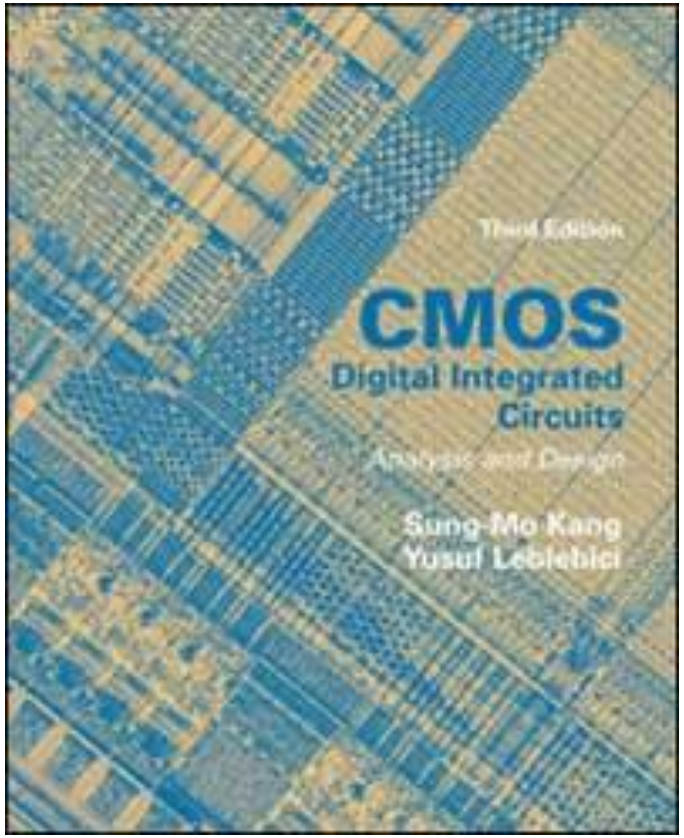


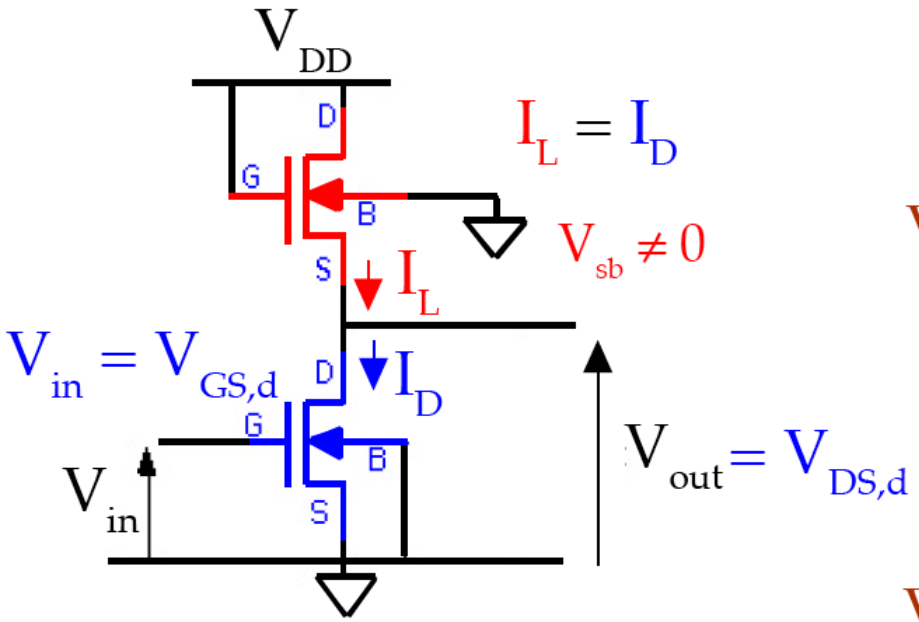
Figure 5.10. Sample layout of resistive-load inverter circuits with (a) diffused resistor and (b) undoped polysilicon resistor.

Digital IC Design and Architecture



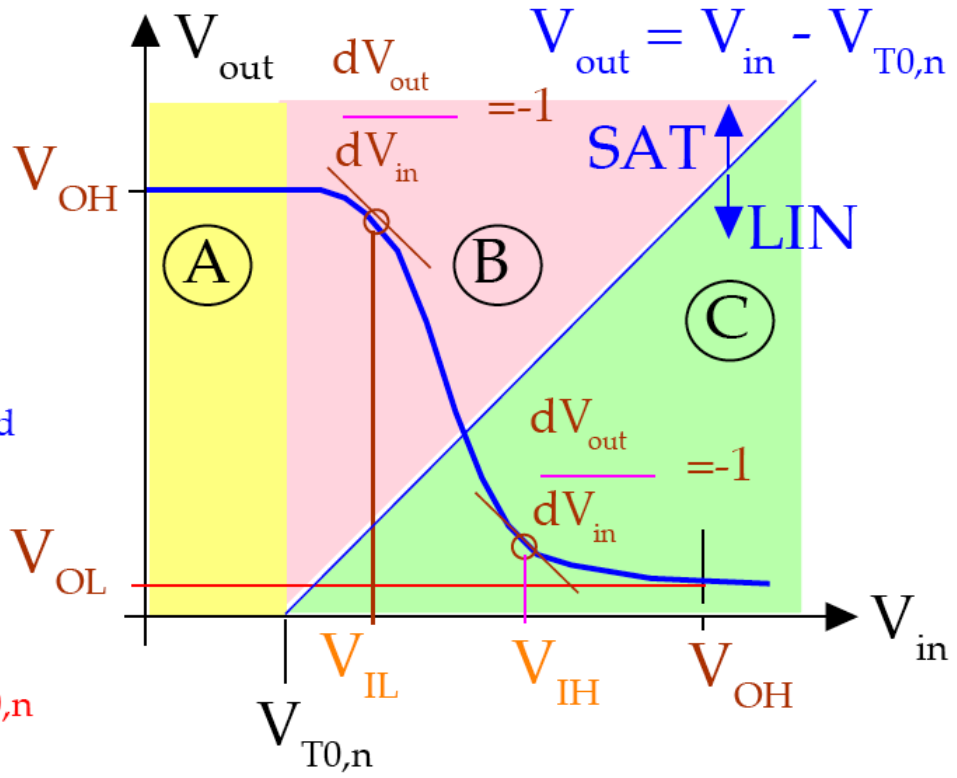
Saturated Enhancement Load Inverter

SATURATED ENHANCEMENT-LOAD INVERTER



$V_{BS,d} = 0 \Rightarrow V_{T,d} = V_{T0,n}$

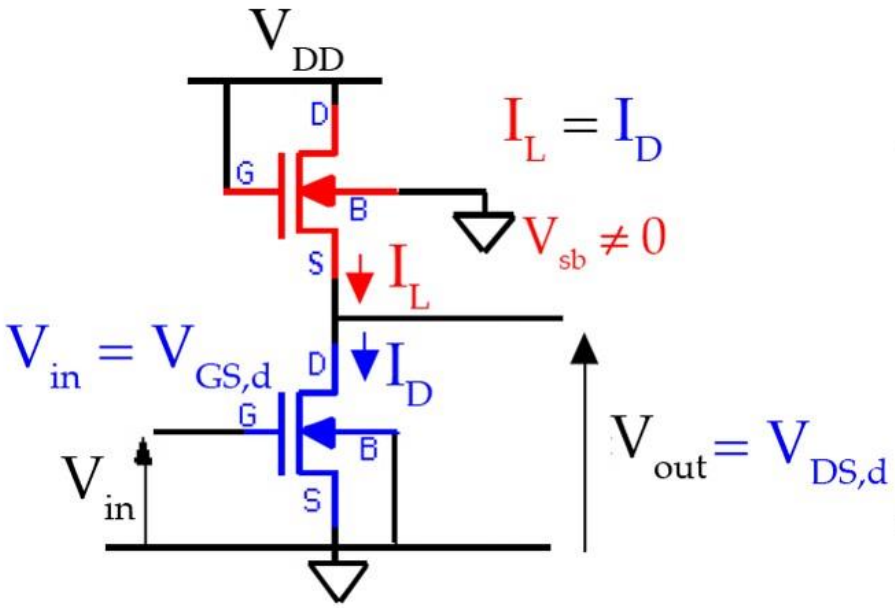
$V_{BS,L} = -V_{out} < 0 \Rightarrow V_{T,L} \neq V_{T0,n}$

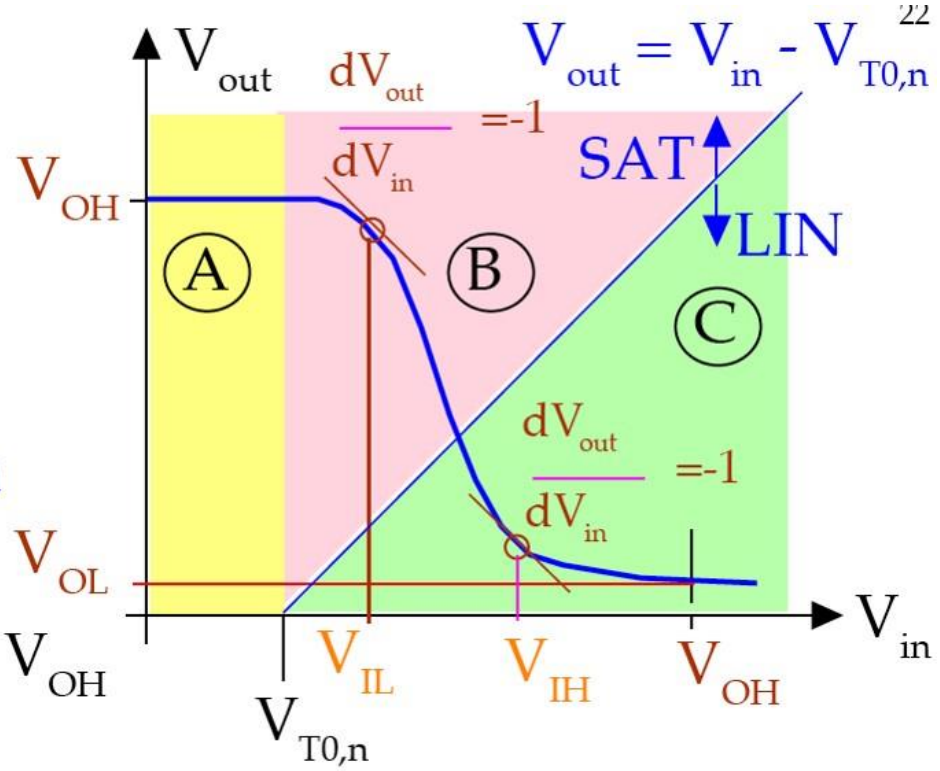


LOAD:

$V_{GS,L} = V_{DS,L} \Rightarrow V_{DS,L} > V_{GS,L} - V_{T,L}$ SAT cond. is ALWAYS SATISFIED

$$I_L = \frac{k'_n}{2}\left(\frac{W}{L}\right)_L \left(V_{GS,L} - V_{T.L}\right)^2 = \frac{k'_n}{2}\left(\frac{W}{L}\right)_L \left(V_{DD} - V_{out} - V_{T.L}\right)^2$$





Load -> Sat, Driver -> Cutoff (A) V_{OH}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=0$$

Load -> Sat, Driver -> Sat (B) V_{IL}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=\frac{k_n'}{2}\left(\frac{W}{L}\right)_d\left(V_{in}-V_{T0,n}\right)^2$$

Load -> Sat, Driver -> Lin (C) V_{IH}, V_{OL}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=\frac{k_n'}{2}\left(\frac{W}{L}\right)_d\left(2[V_{in}-V_{T0,n}]V_{out}-V_{out}^2\right)$$

$V_{OH} < V_{DD}$

$V_{OL} > 0$

- Saturated Enhancement Load Inverters require relatively high stand-by DC power dissipation

- Because of this high stand-by DC power dissipation the Enhancement-load nMOS inverters are not used in any large-scale digital applications

Textbook examples to be reviewed:

Examples 5.1 and 5.2 – Resistive Load Inverter

Example 5.4 – nMOS with pMOS Load Inverter