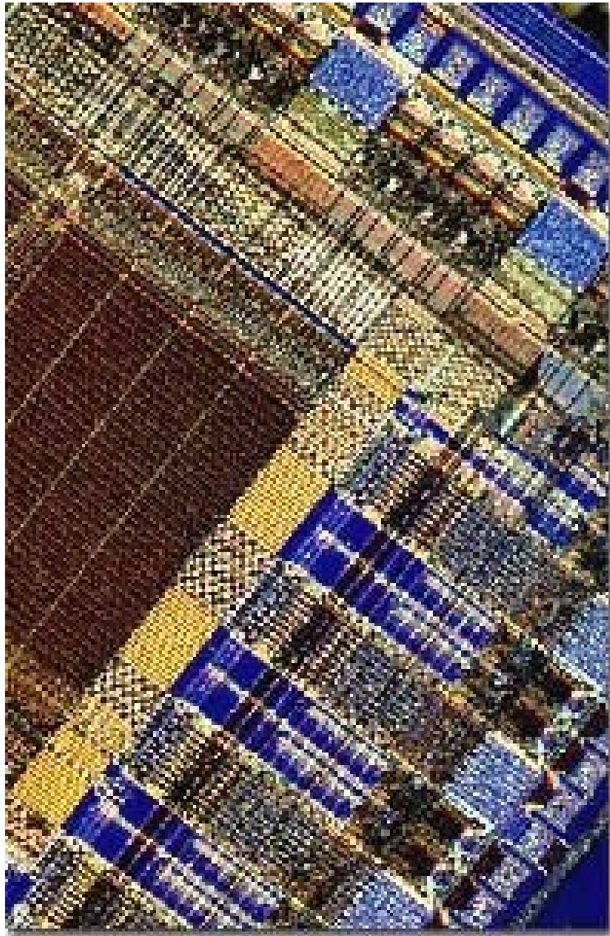
Digital Integrated Circuit Design and Architecture



Chapter 2: Fabrication of MOSFETs

CMOS ICs Fabrication

- CMOS transistors and CMOS ICs are fabricated on silicon wafers
- Photo-Lithography process is used for the fabrication and it is similar to printing press
- On each step of different materials are deposited or etched

Silicon Ingot

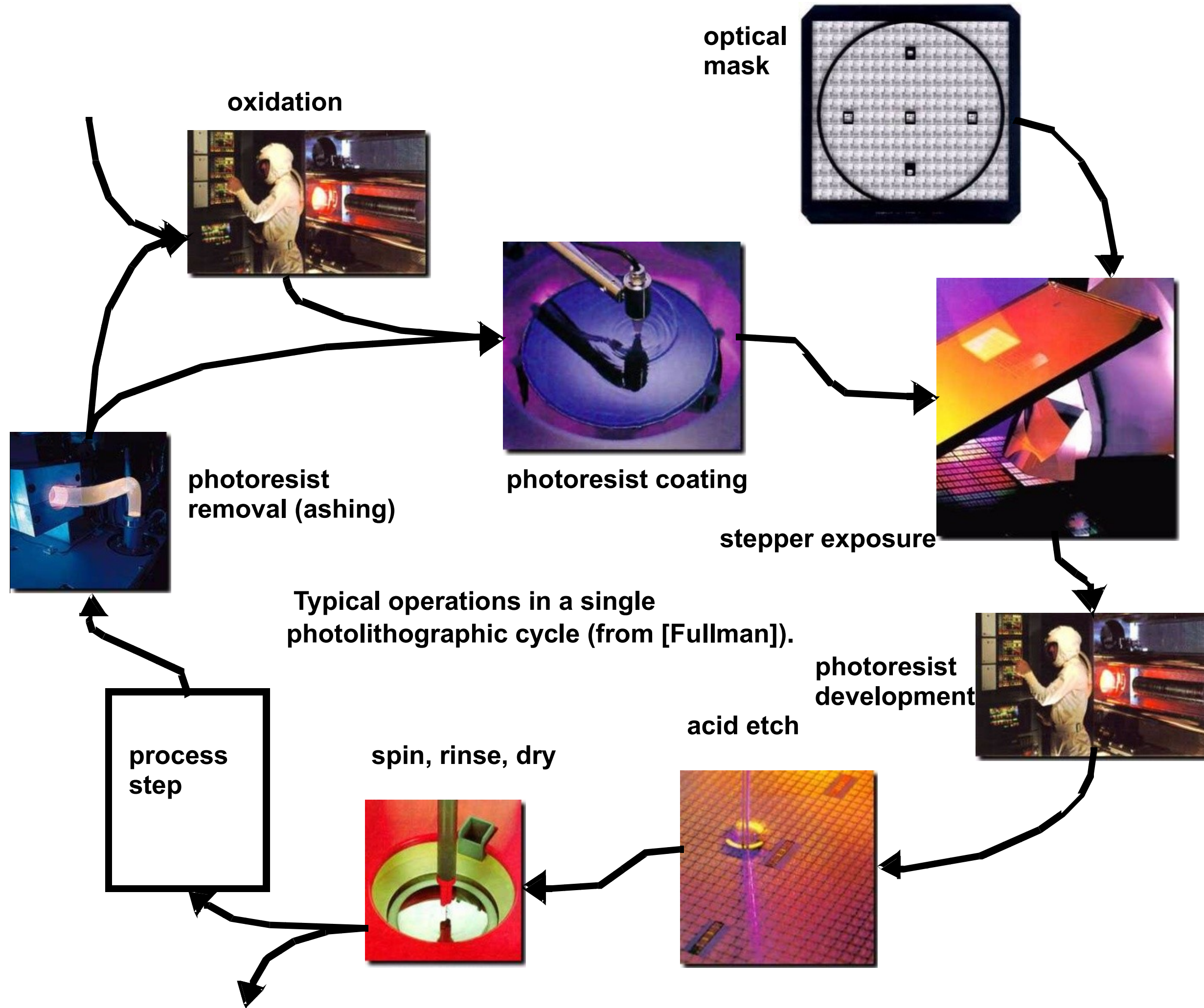
Silicon Ingot and Wafer Manufacturing

Ingot

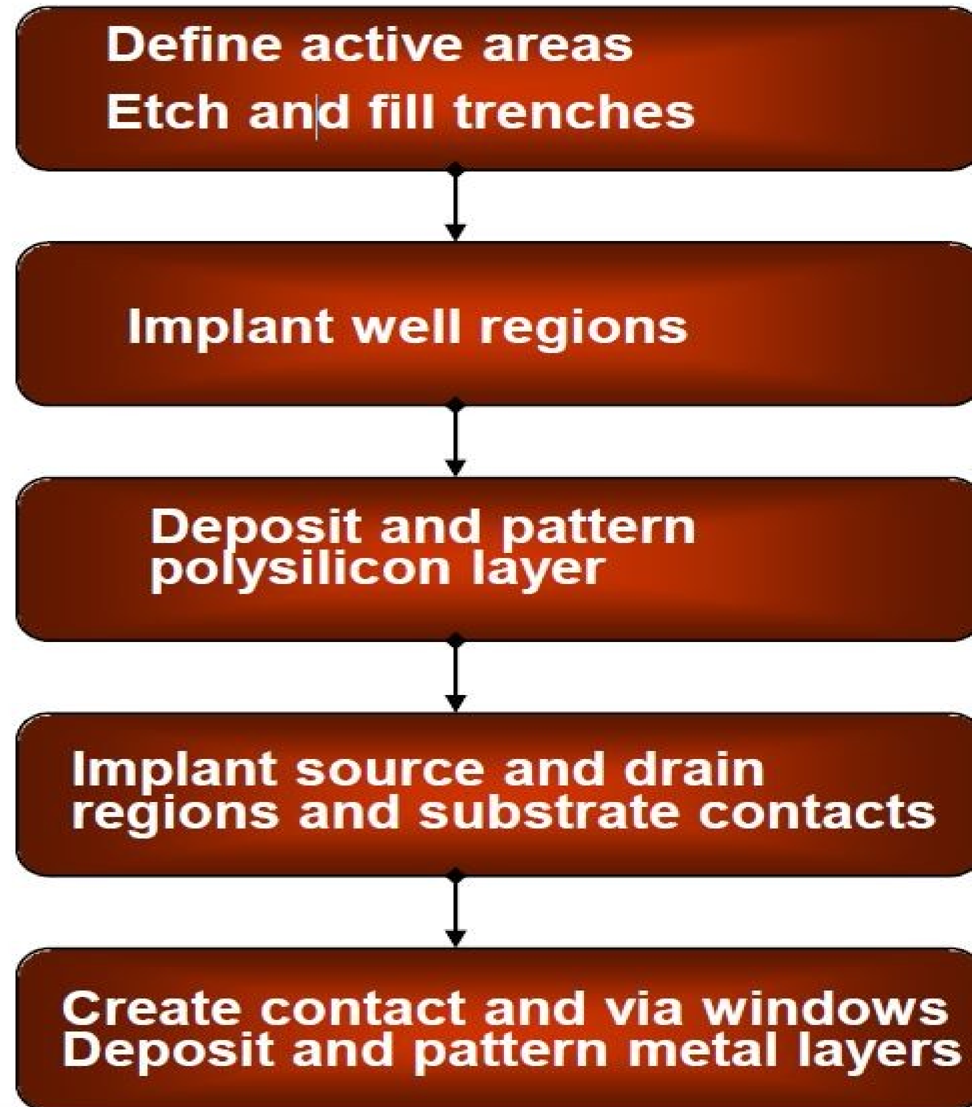
Wafer

From *Smithsonian*, 2000

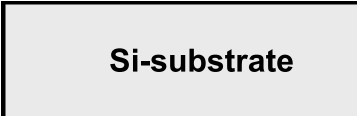
Photo-Lithographic Process



CMOS Process insight

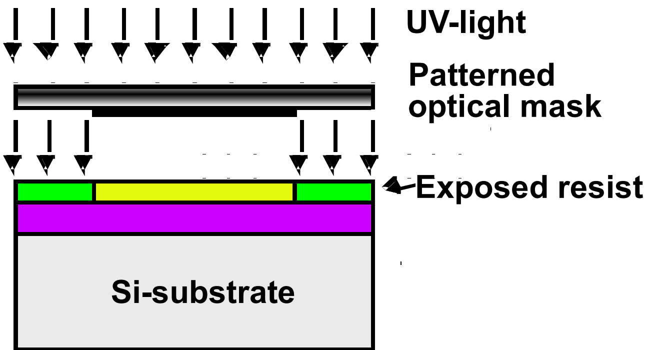


Patterning of SiO2 – Basic Steps

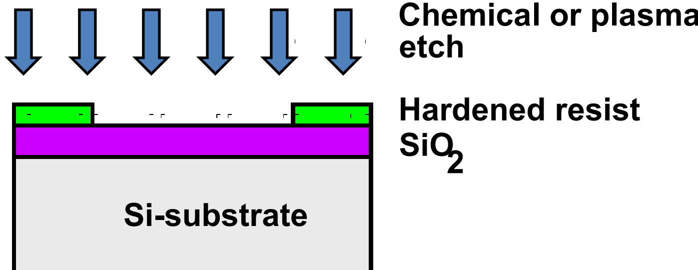


(a) Silicon base material

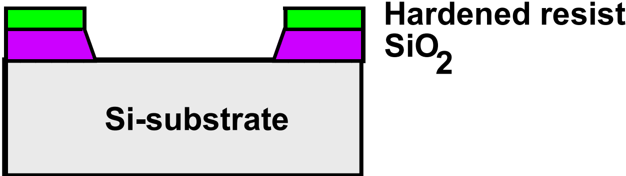
(b) After oxidation and deposition of negative photoresist



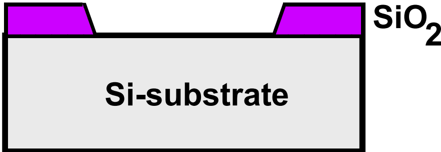
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

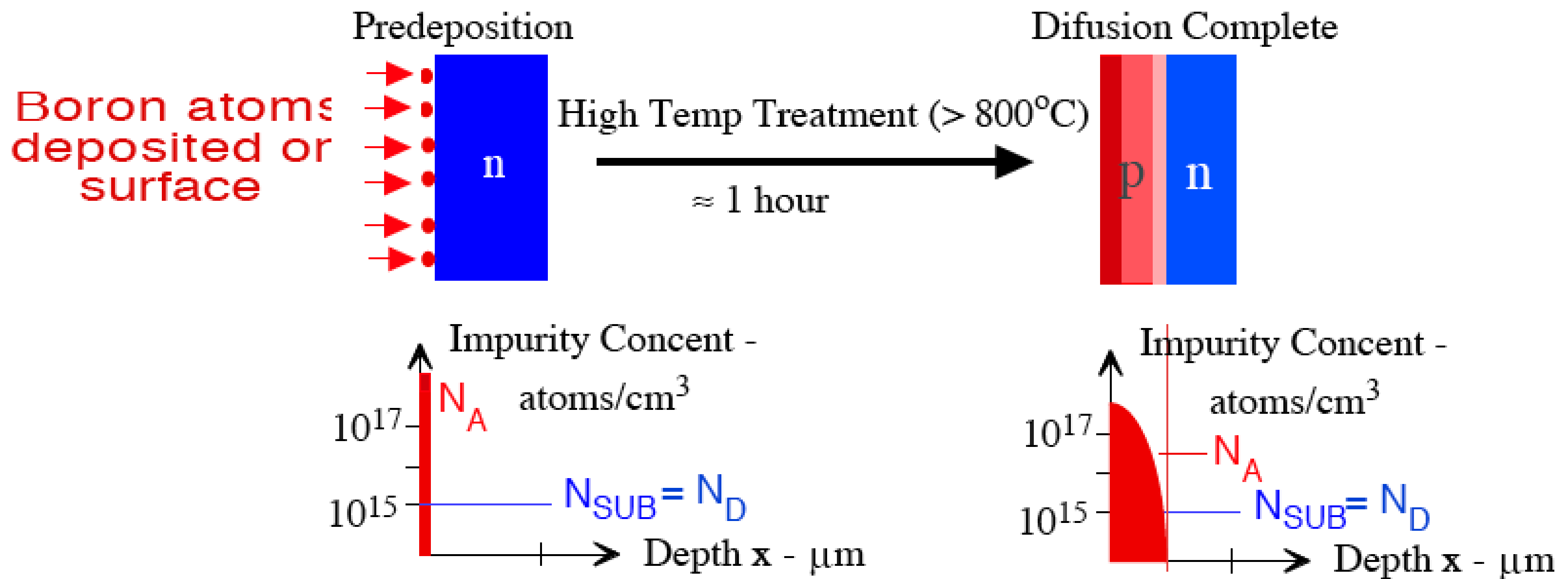


(e) After etching



(f) Final result after removal of resist

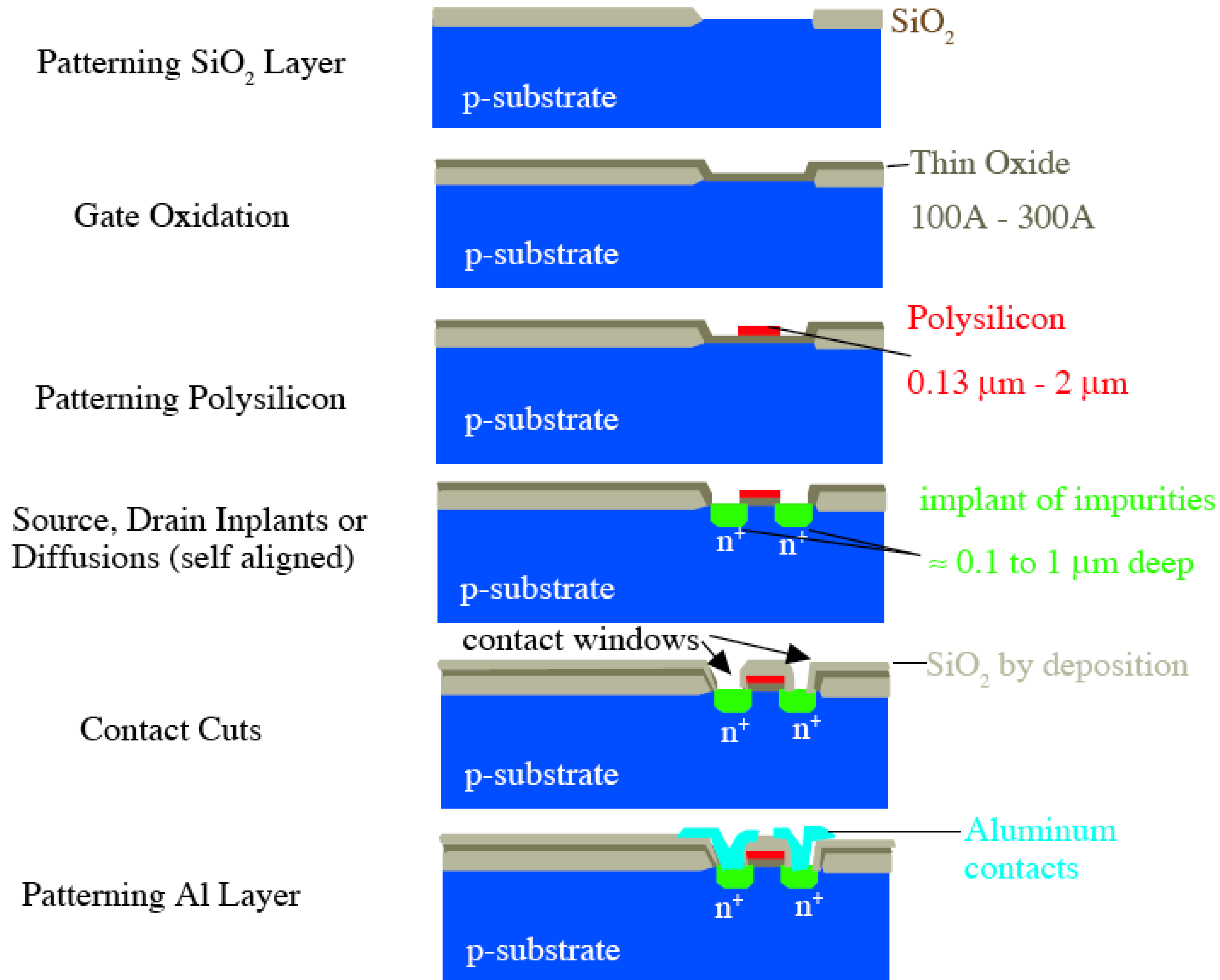
Creating Diffusion Regions



-> Boron typically used for p-type doping

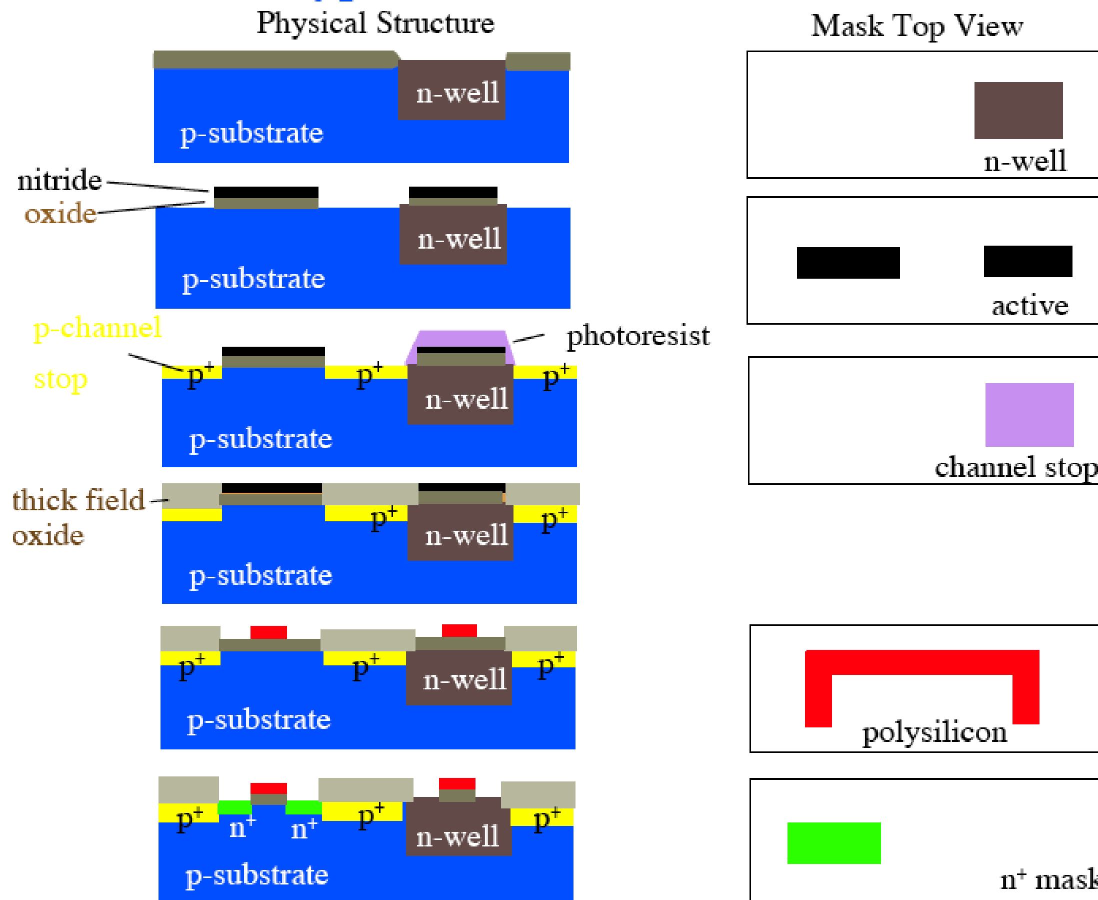
-> Arsenic and Phosphorus are typically used for n-type doping.

Fabrication Steps in Si-Gate (self-aligned) NMOS Process

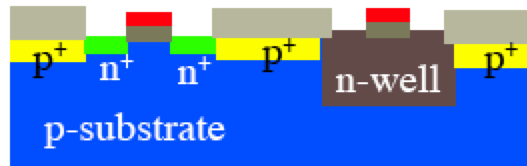


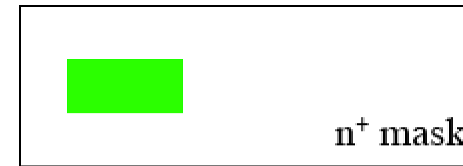
CMOS Process Walk-Through

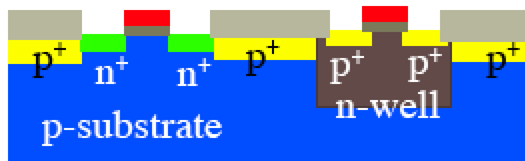
Fabrication of nMOS and pMOS transistors process example

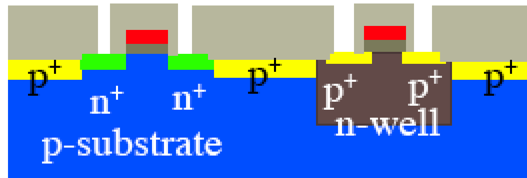


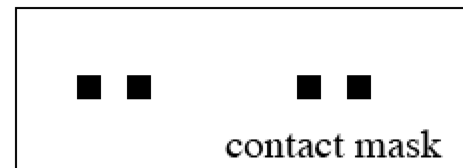
CMOS Process Walk-Through

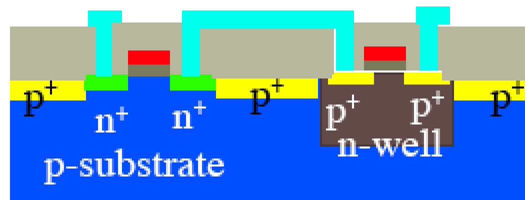


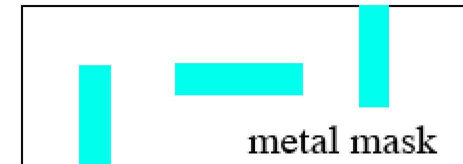




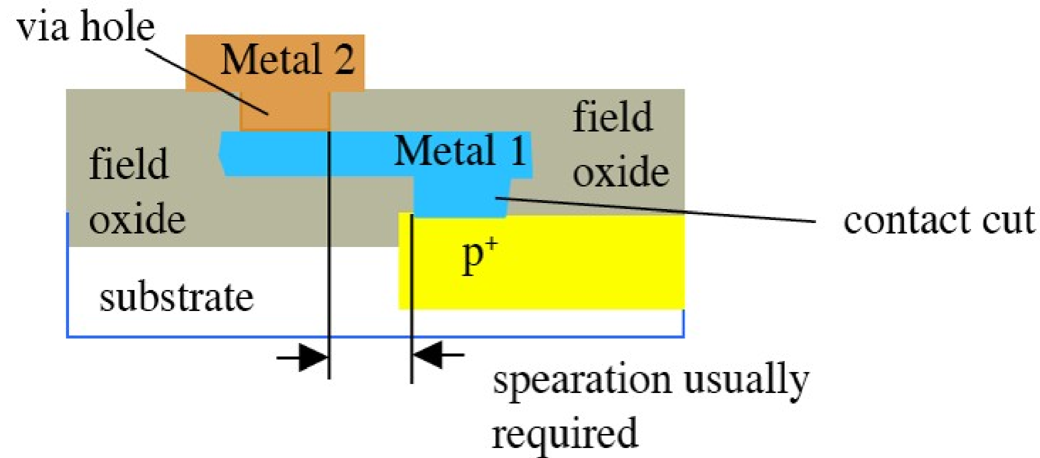


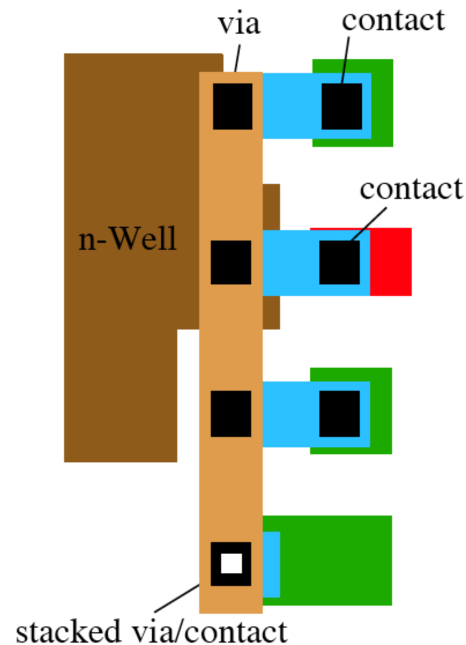






Contacts and Vias in CMOS Fabrication





MOSIS (MOS Implementation) layout design rules

Rule number	Description	λ-Rule
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ

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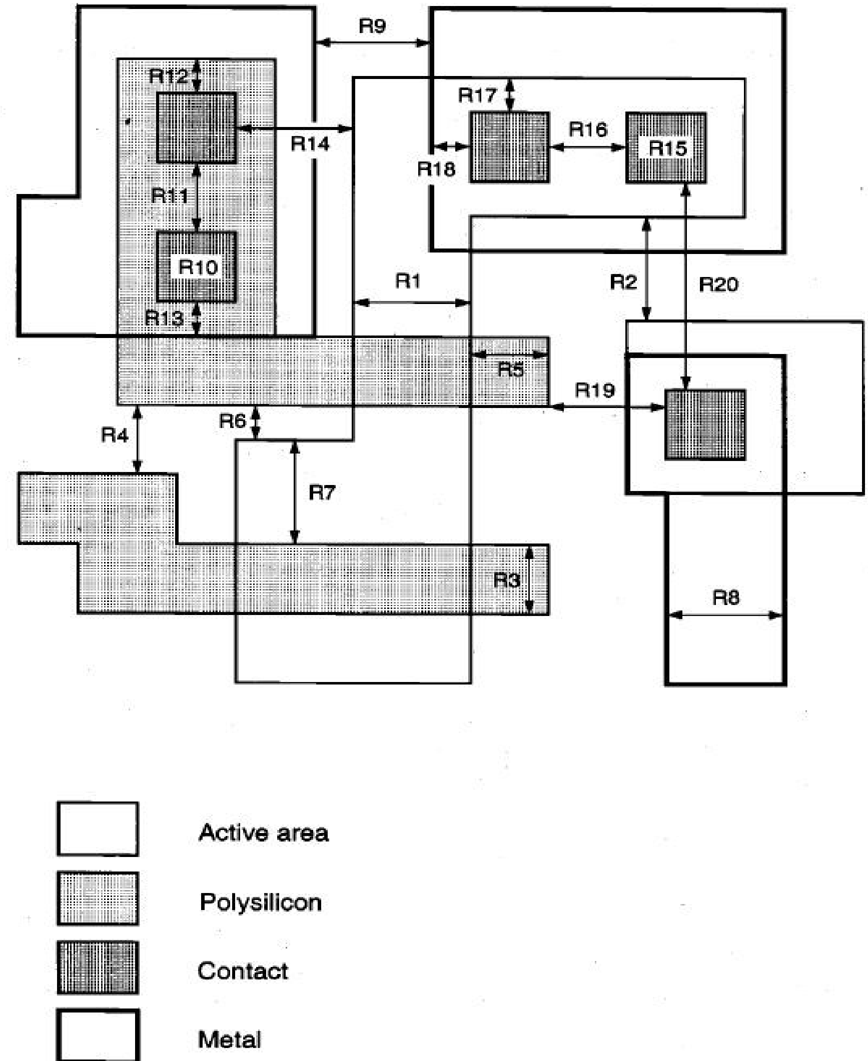
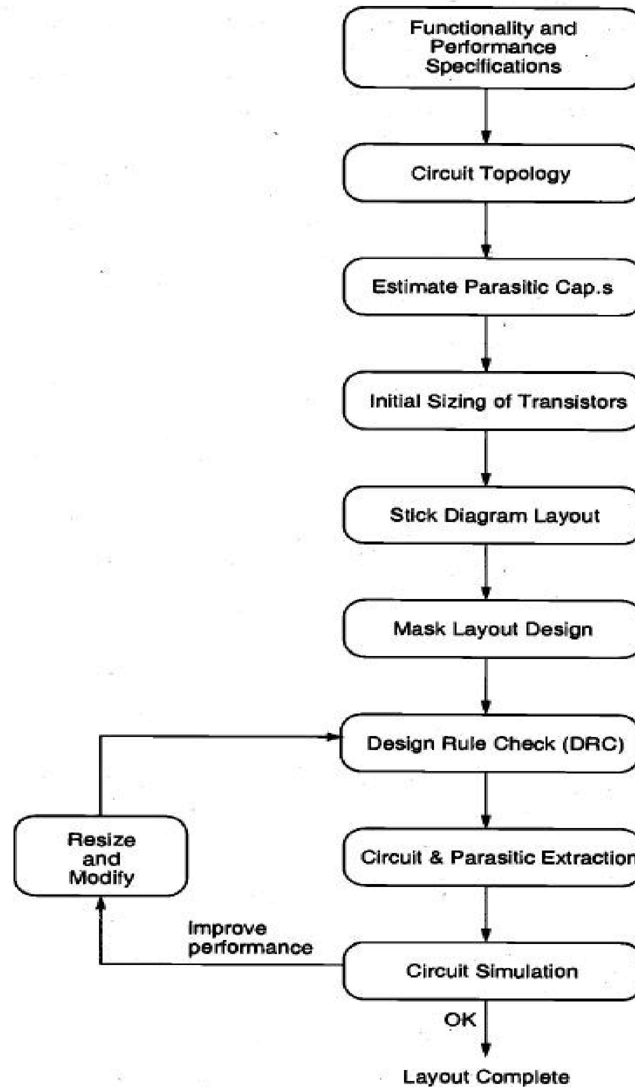
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ

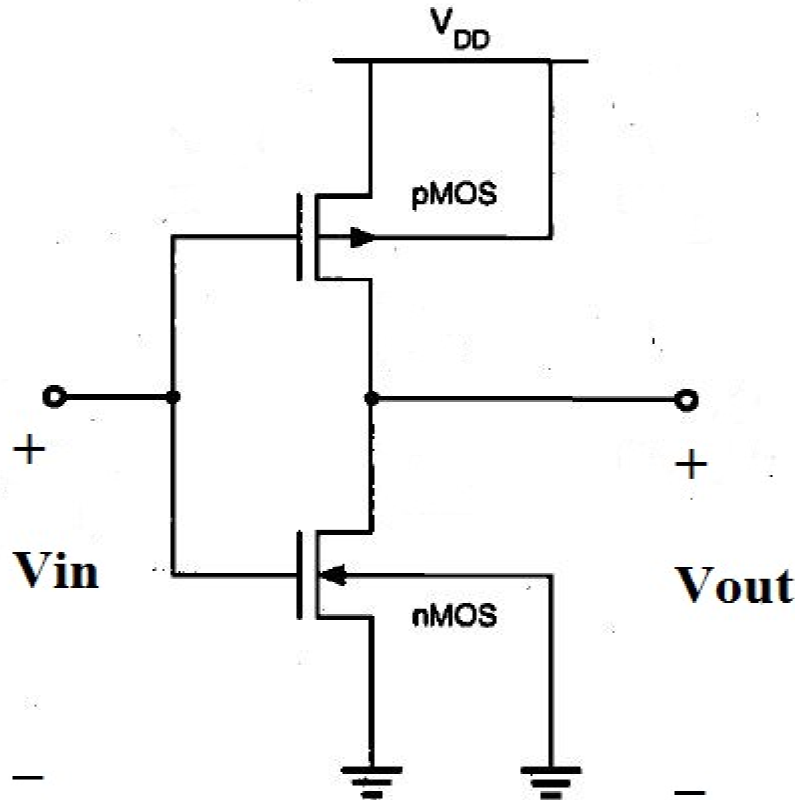


CMOS Inverter Layout Design Example



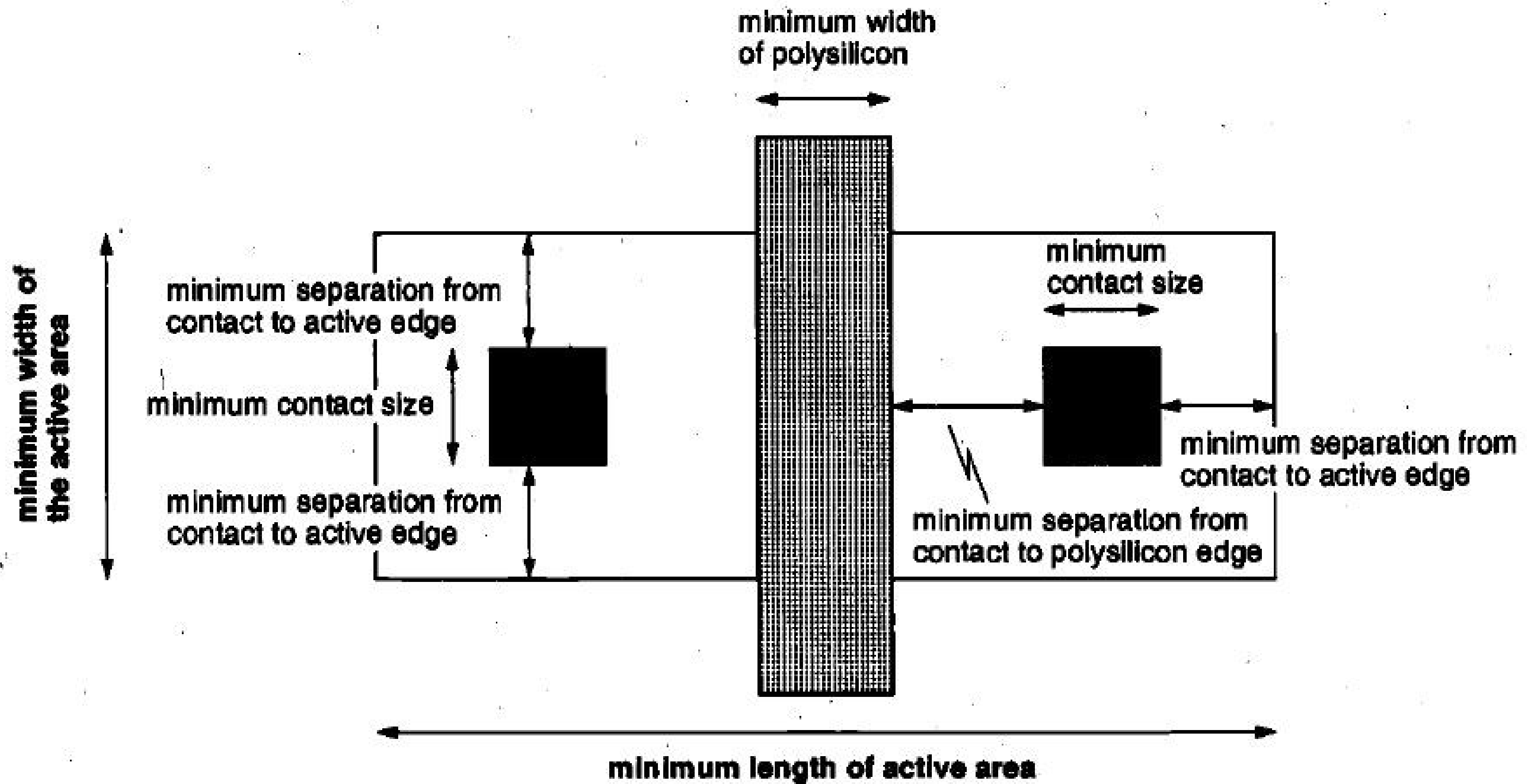
Typical design flow for the production of a mask layout

CMOS Inverter Layout Design Example



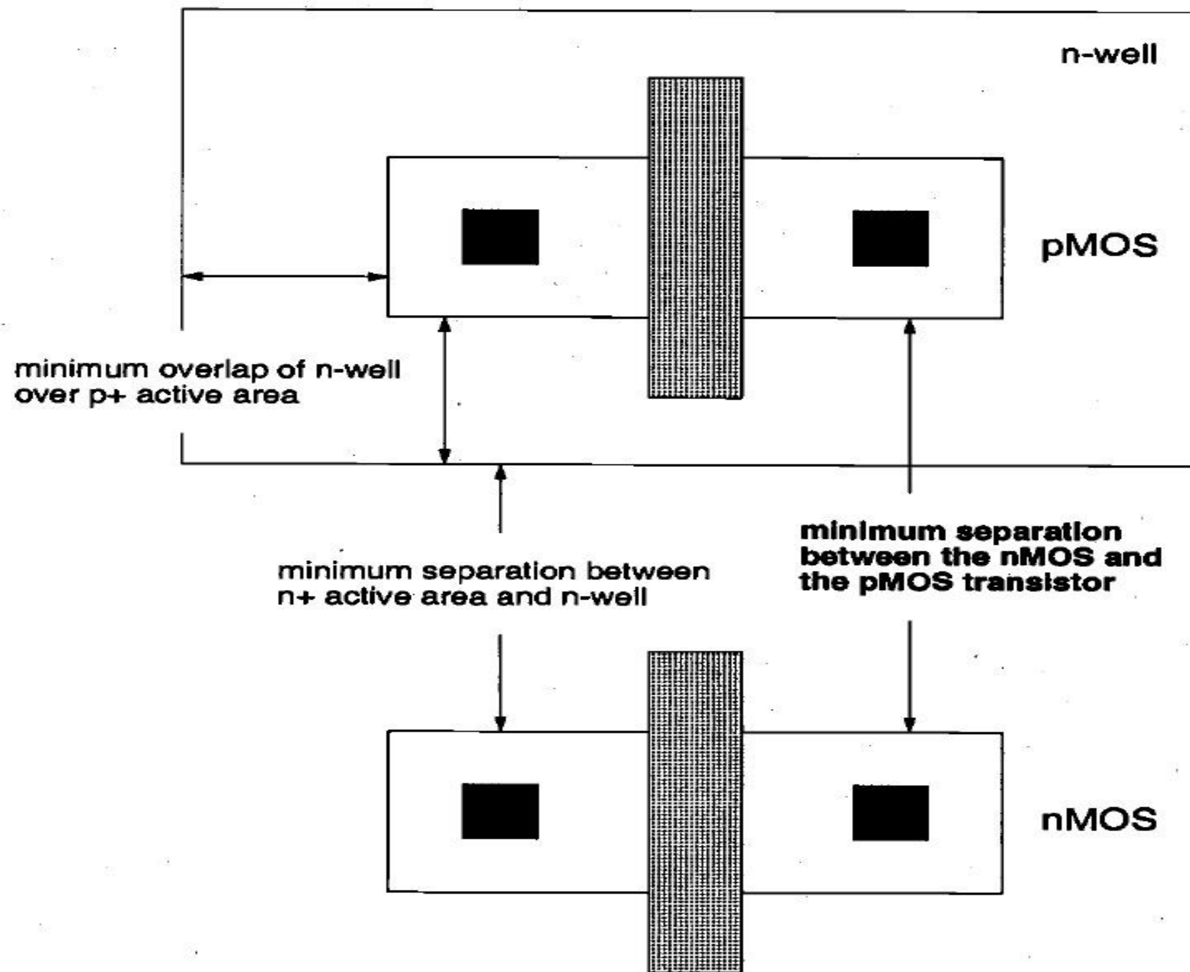
CMOS inverter

CMOS Inverter Layout Design Example



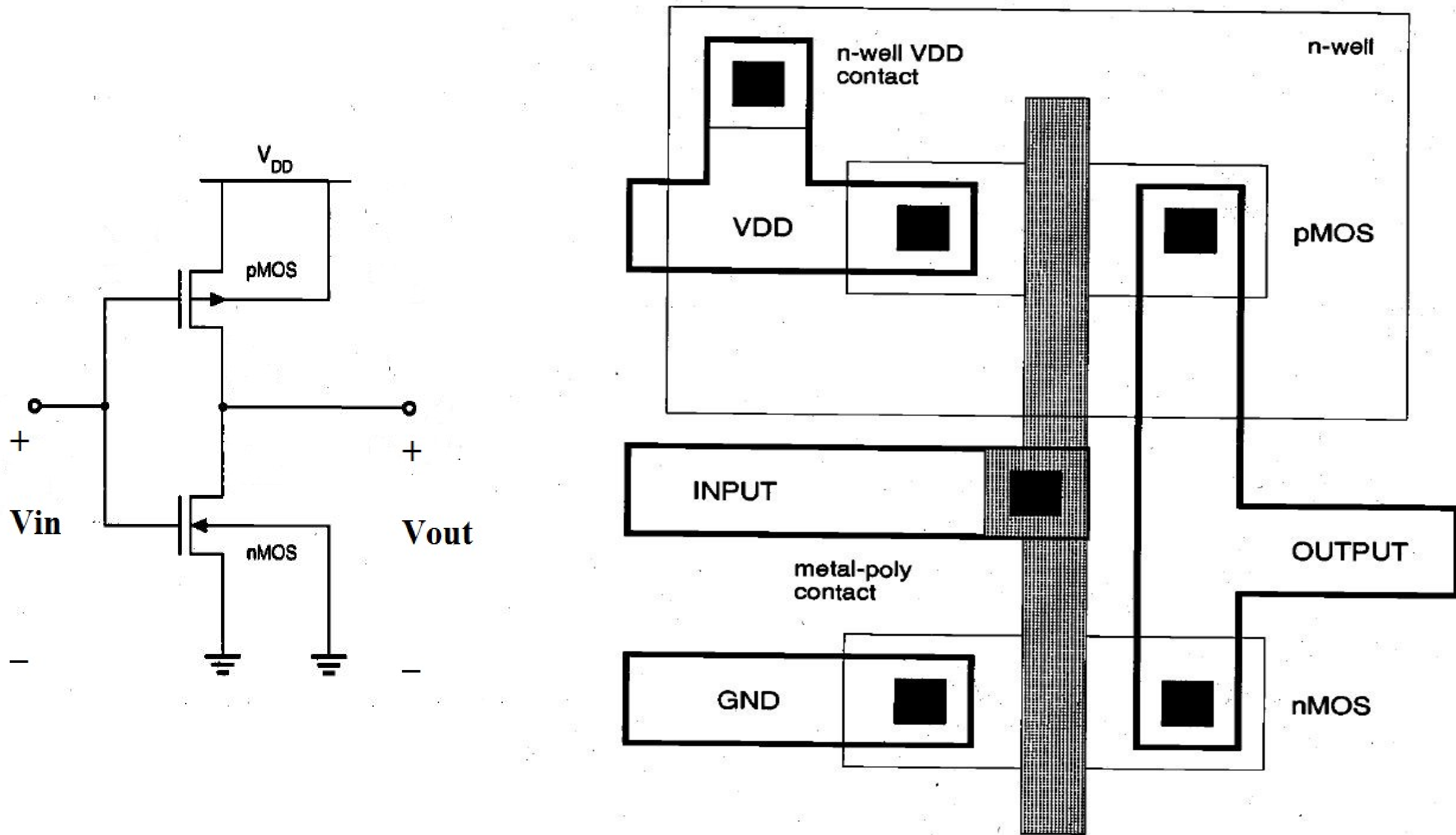
Design rules which determine the dimensions of a min size transistor

CMOS Inverter Layout Design Example



Design rules which determine the separation between nMOS and pMOS transistor

CMOS Inverter Layout Design Example



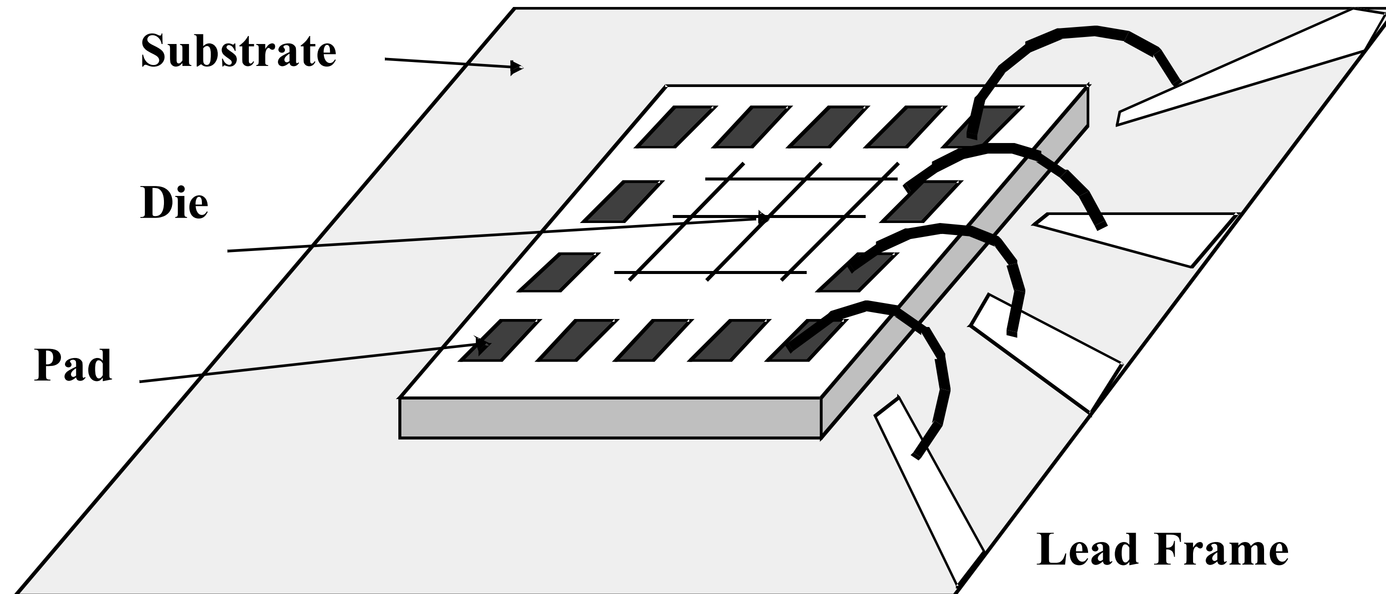
Complete mask layout of the CMOS inverter

Packaging Requirements

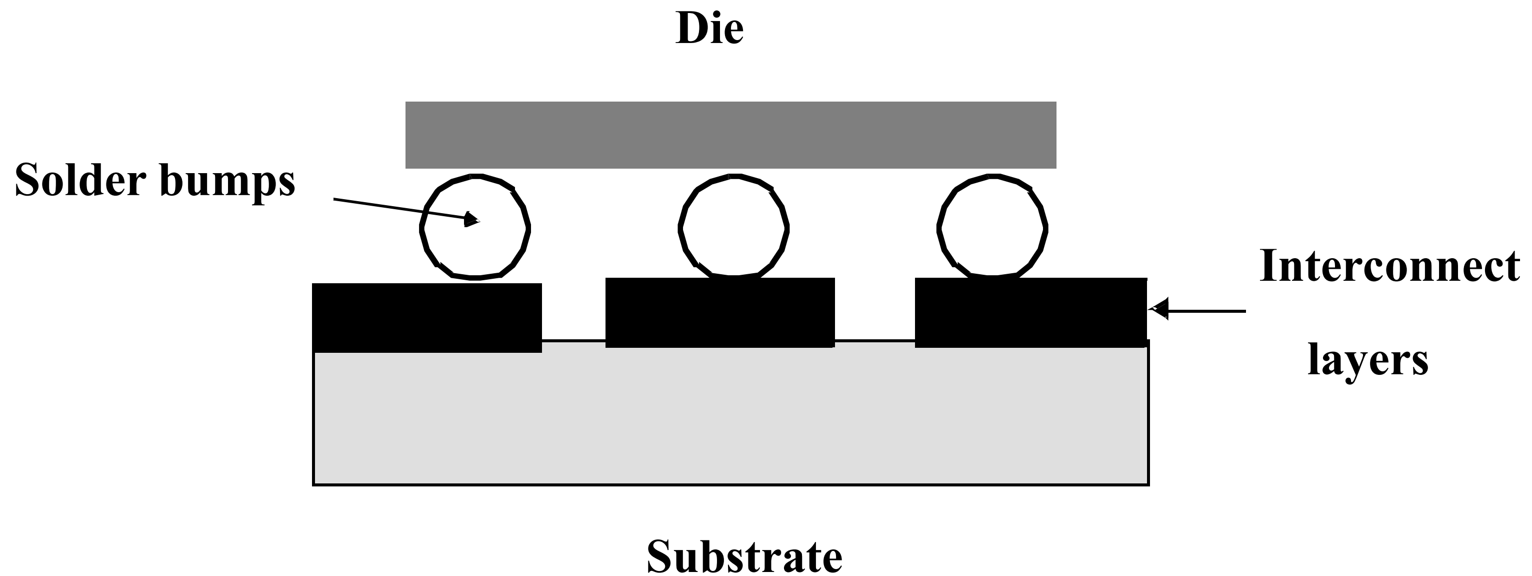
- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

Bonding Techniques

Wire Bonding



Flip-Chip Bonding



Package Types

Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])