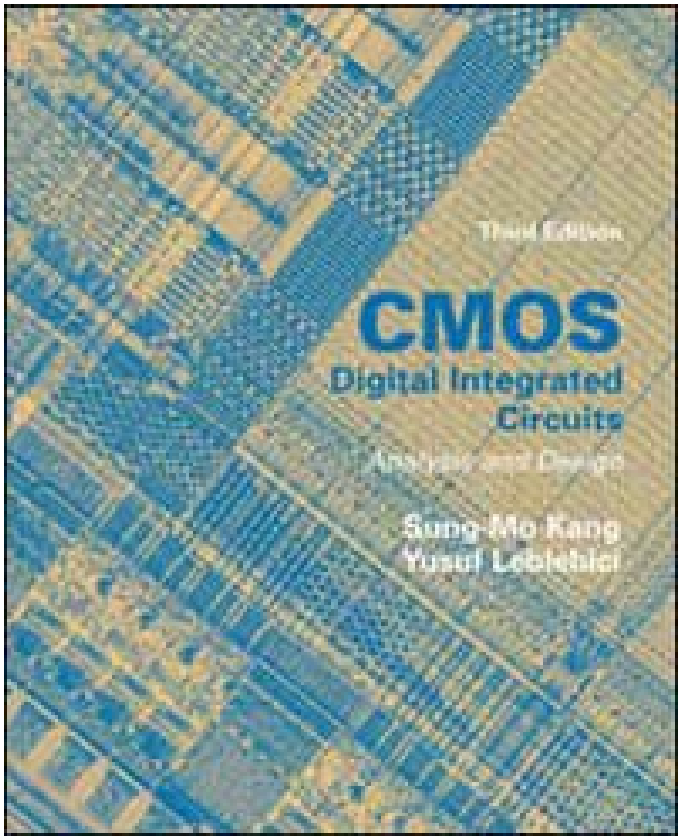
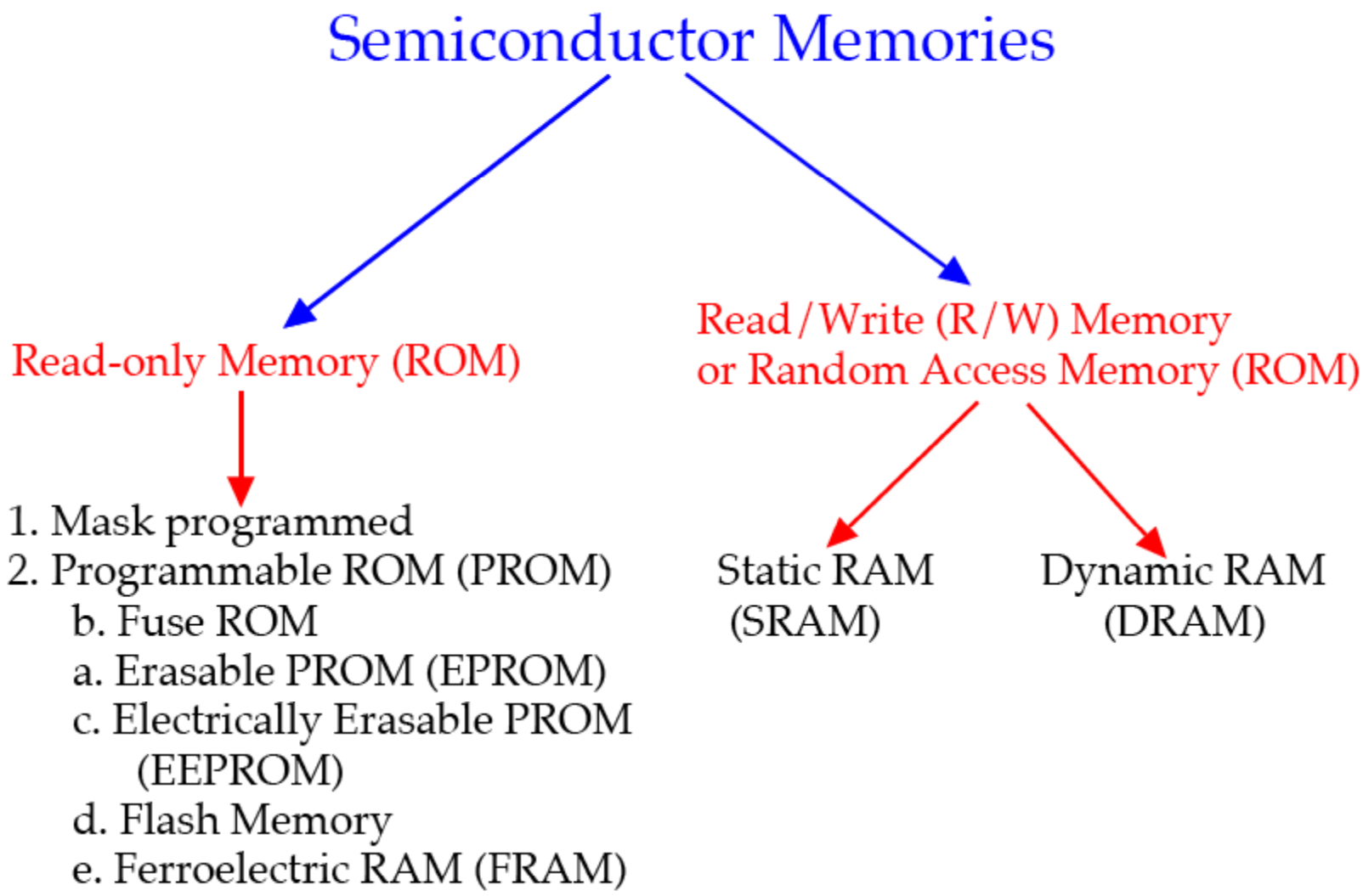
Digital IC Design and Architecture



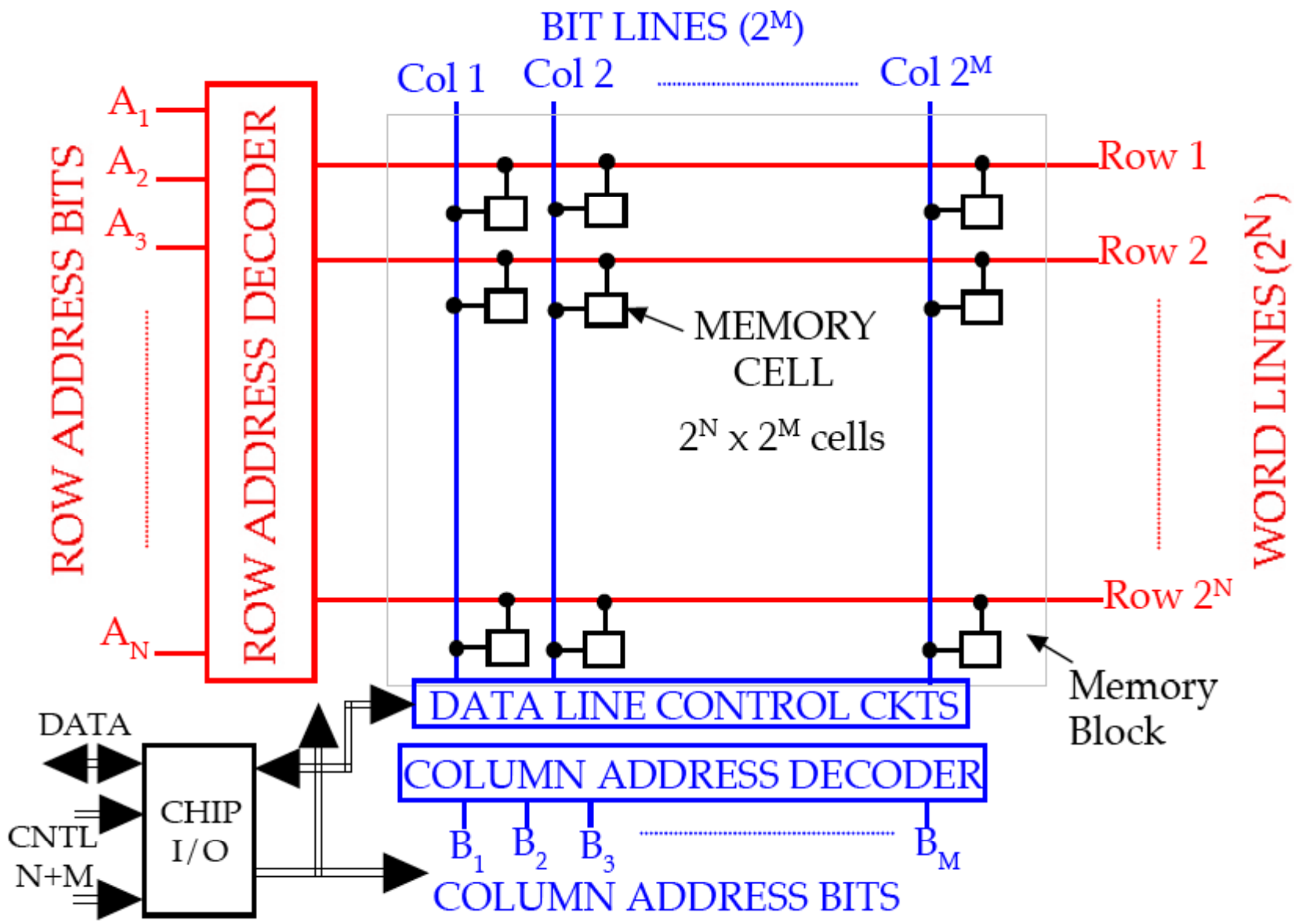
Semiconductor Memories


Semiconductor Memories
Read-only Memory (ROM)
Read/Write (R/W) Memory
or Random Access Memory (ROM)
1. Mask programmed
2. Programmable ROM (PROM)
b. Fuse ROM
a. Erasable PROM (EPROM)
c. Electrically Erasable PROM
(EEPROM)
d. Flash Memory
e. Ferroelectric RAM (FRAM)
Static RAM
(SRAM)
Dynamic RAM
(DRAM)

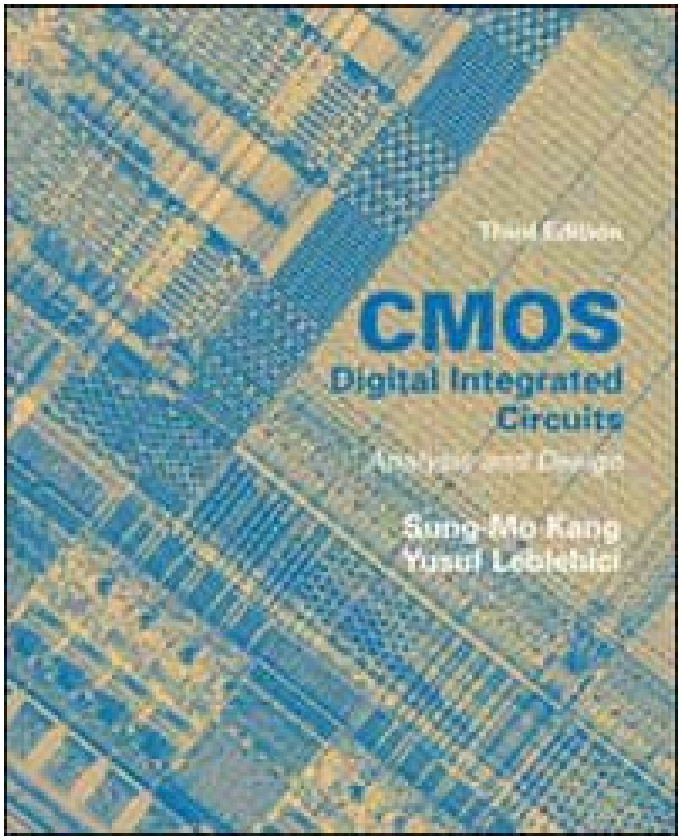
MEMORY DEVICE CHARACTERISTICS

	DRAM	SRAM	UV EPROM	EEPROM	FLASH	FRAM
Data volatility	Yes	Yes	No	No	No	No
Data Refresh Op	Required	No	No	No	No	No
Cell Structure	1T-1C	6T	1T	2T	1T (2 G)	1T-1C
Cell Density	High	Low	High	Low	High	High
Power Consm	High	High/low	High	Low	Low	High
Read Speed	≈50ns	≈10/70ns	≈50ns	≈50ns	≈50ns	≈100ns
Write Speed	≈40ns	≈5/40ns	≈10µs	≈5ms	≈10µs-1ms	≈100ns
Cost per Bit	Low	High	Low	High	Low	Low
Application Ex	Main Memory	Cashe/PDAs	Game Machines	ID Card	Memory Card, Solid-State Disk	Smart Card, Digital Camera

TYPICAL RANDOM ACCESS MEMORY ARRAY ORGANIZATION



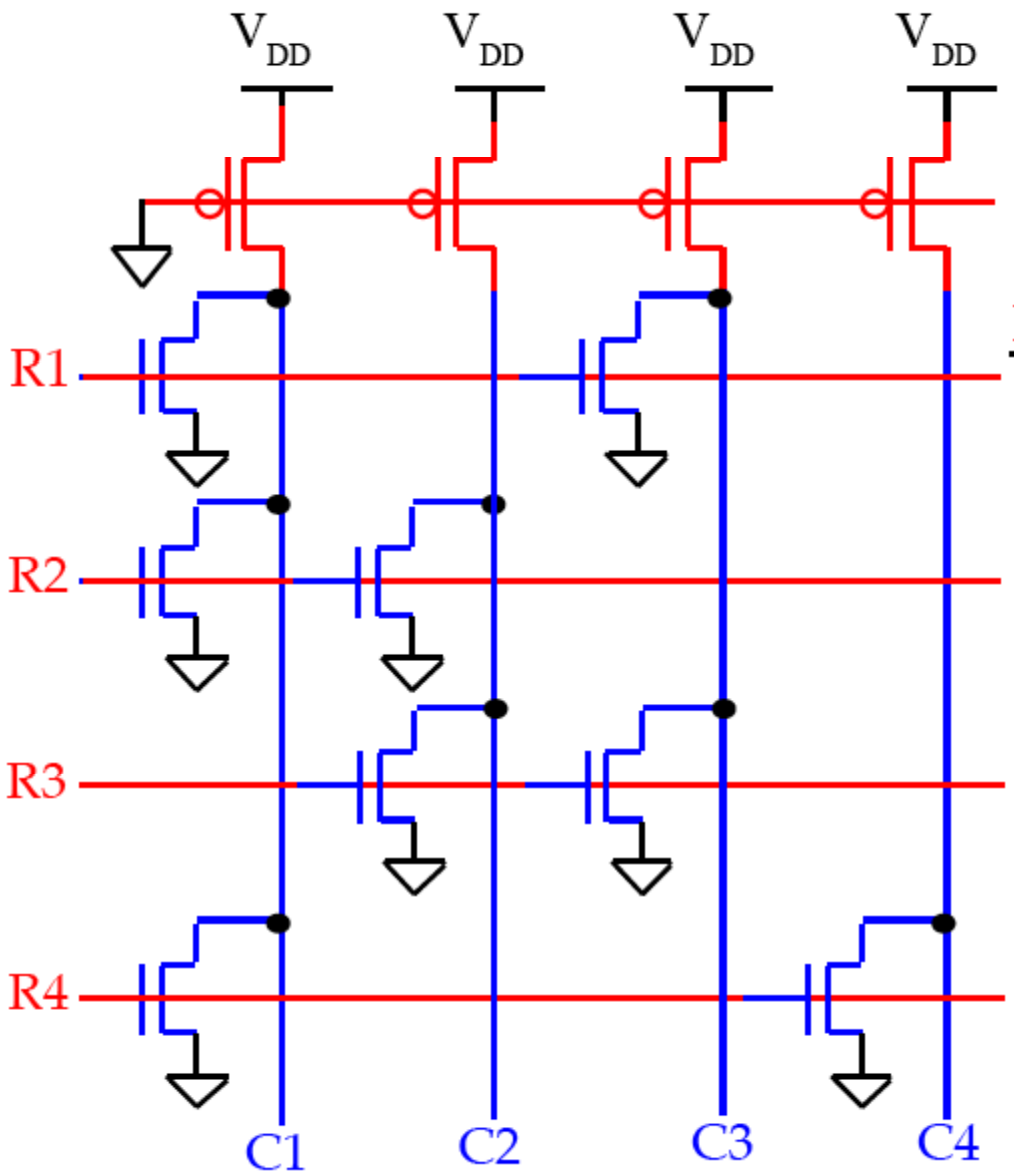
Digital IC Design and Architecture



Nonvolatile Memory

Nonvolatile Memory

ROM CIRCUITS 4 X 4 BIT NOR BASED ROM ARRAY

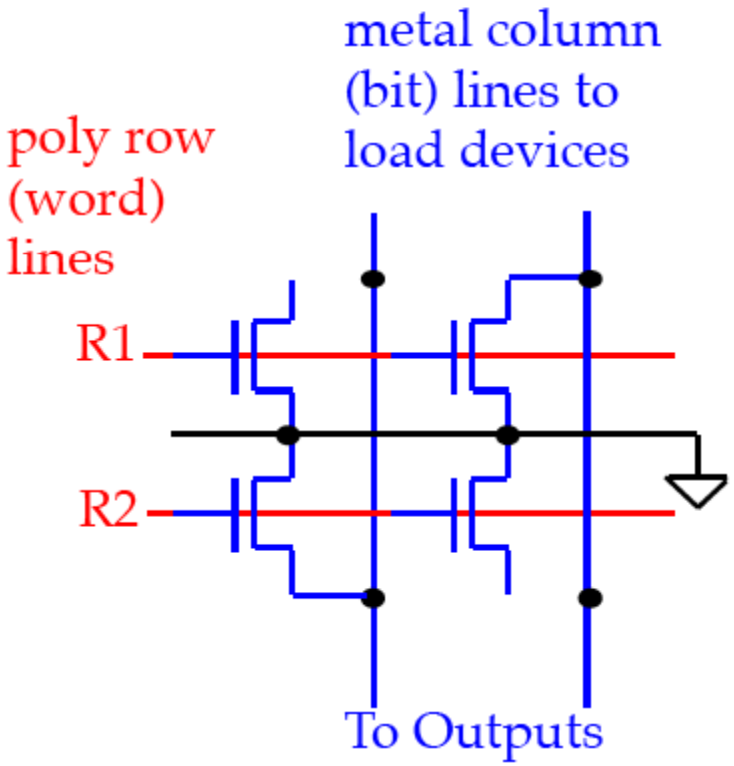


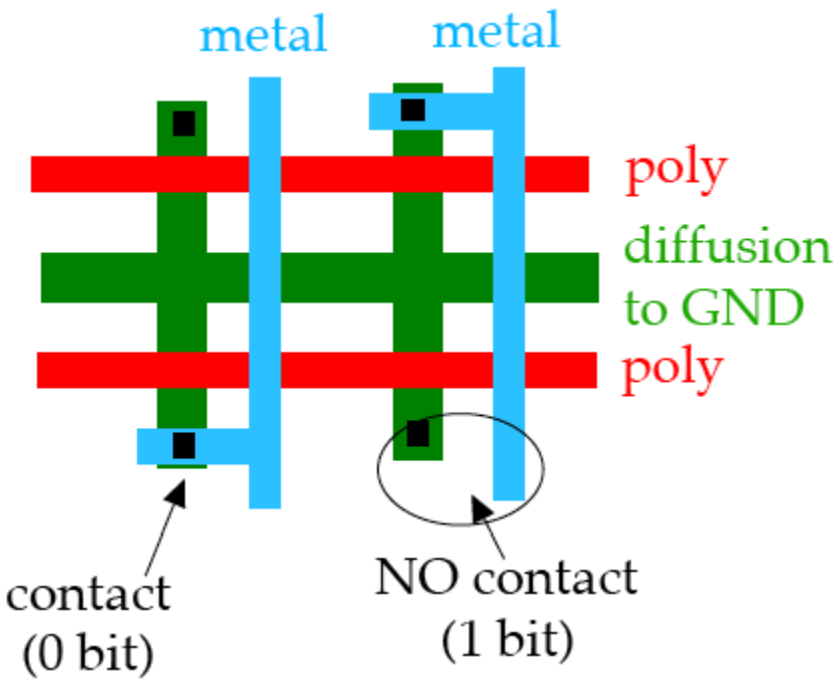
WORD LINES				BIT LINES			
R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0
default "0"				default "1"			

All word lines R_i are kept at logic "0" level, except the selected line is pulled up to "1" level.

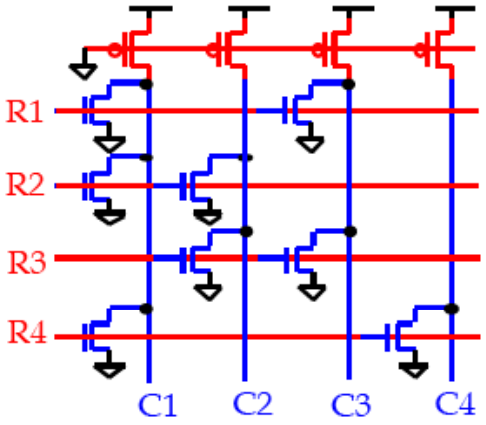
Absent Xstr => store "1"
Present Xstr => store "0"

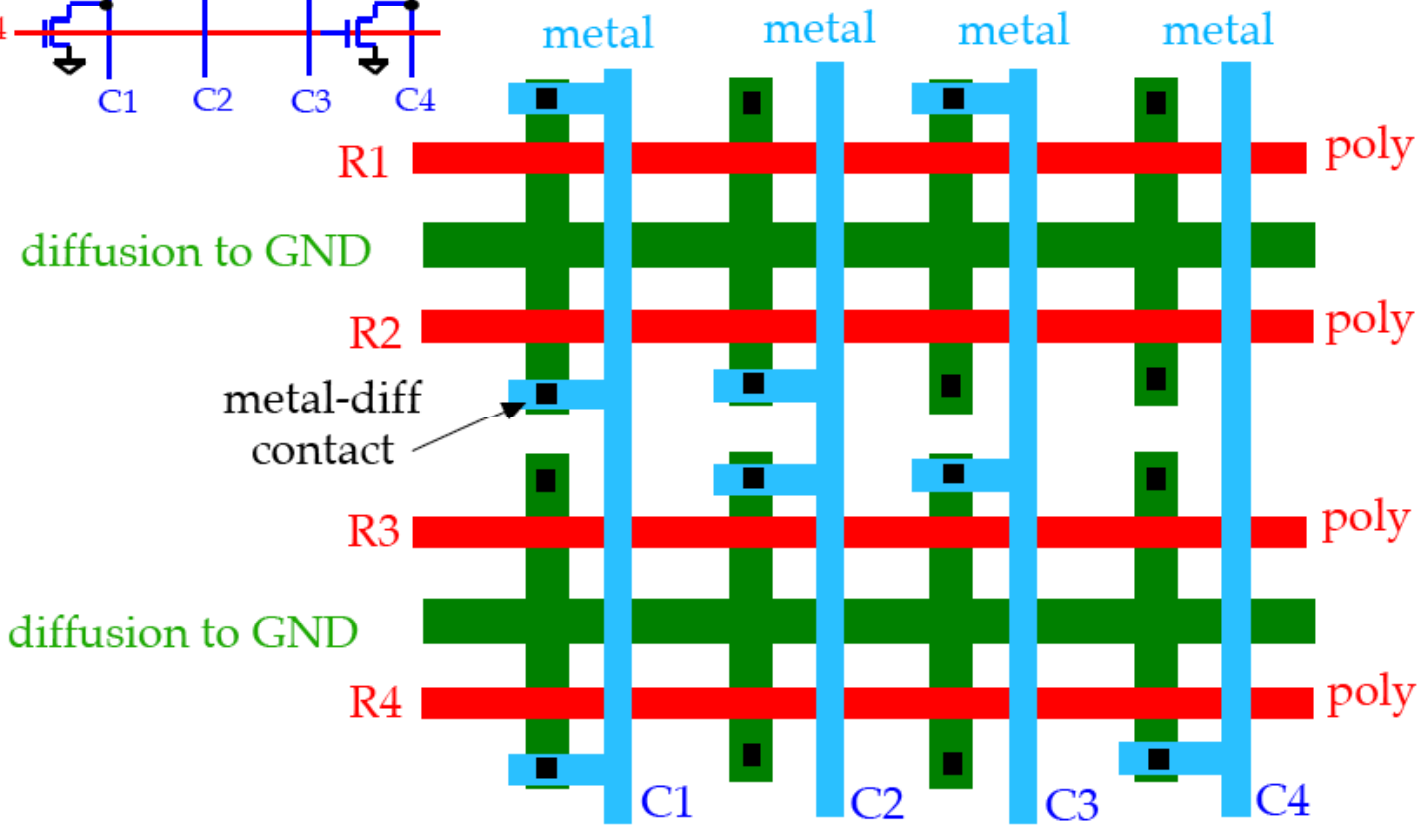
LAYOUT OF CONTACT - MASK PROGRAMMABLE NOR ROM





LAYOUT OF CONTACT -MASK PROGRAMMABLE 4 X 4 BIT NOR ROM

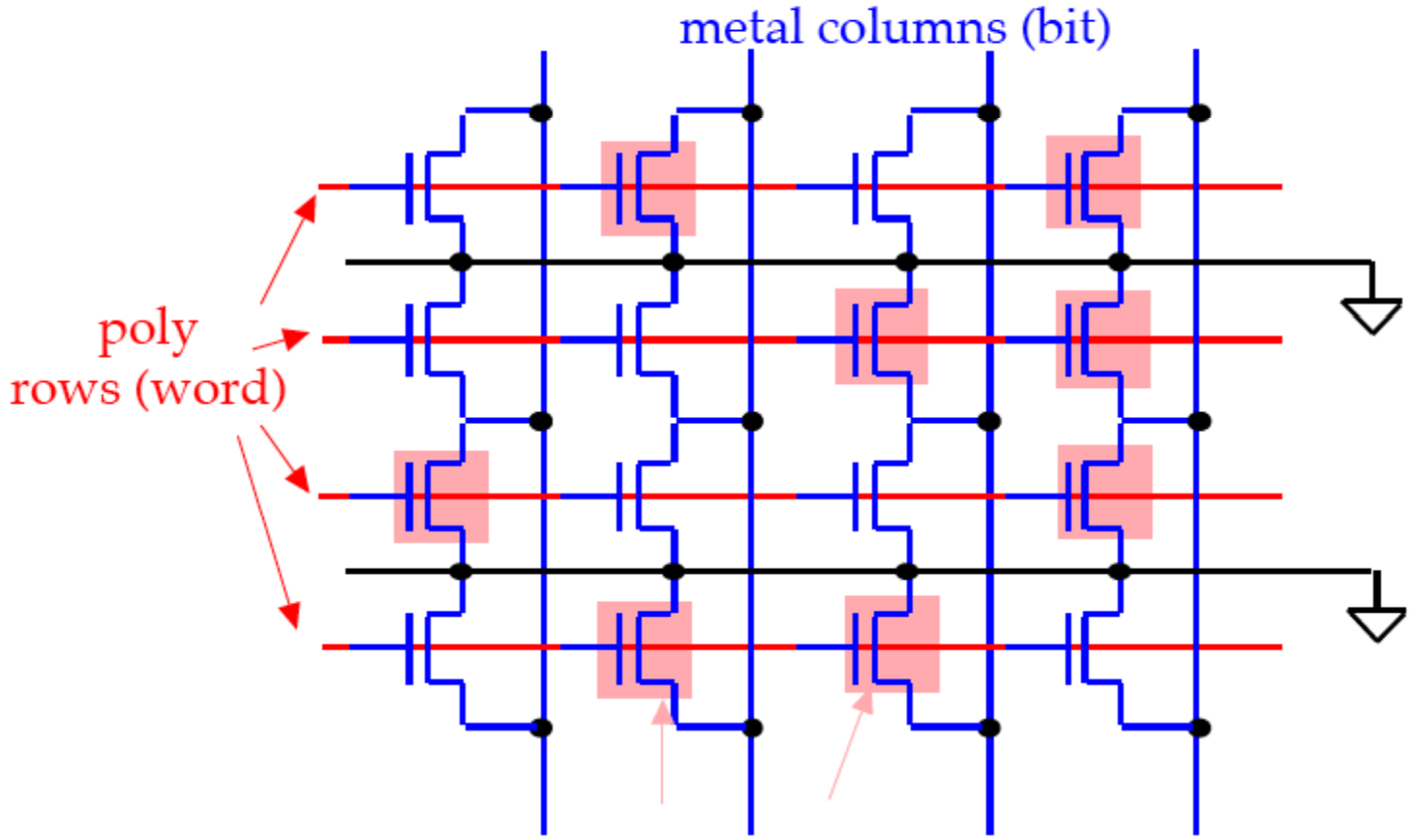




IMPLANT - MASK PROGRAMMABLE NOR ROM ARRAY

Absent Xstr => store "1"

Present Xstr => store "0"

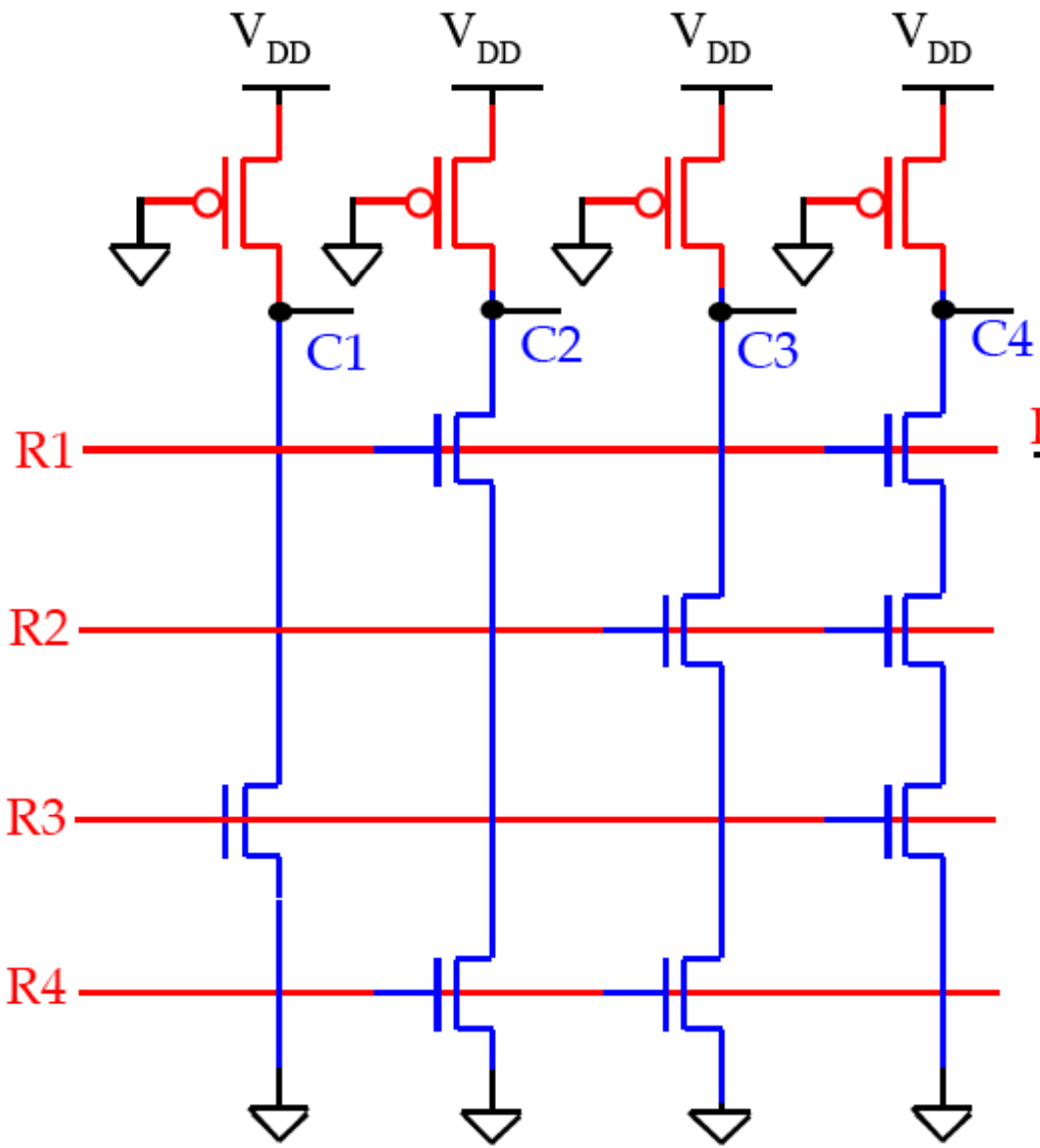


threshold voltage implant to activate 1 bit

$V_{T0} > V_{DD}$

permanent OFF transistor <=> contact disconnect

4 X 4 BIT NAND BASED ROM ARRAY



WORD LINES				BIT LINES			
R1	R2	R3	R4	C1	C2	C3	C4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0
default "1"				default "0"			

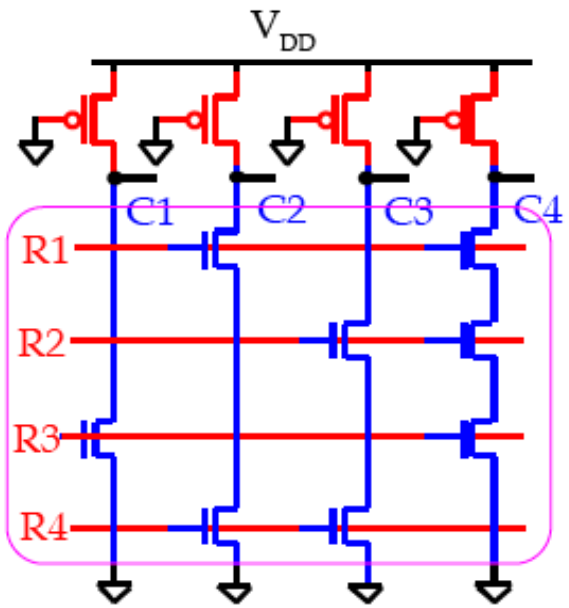
All word lines are kept at logic "1" level, except the selected line is pulled down by "0" level.

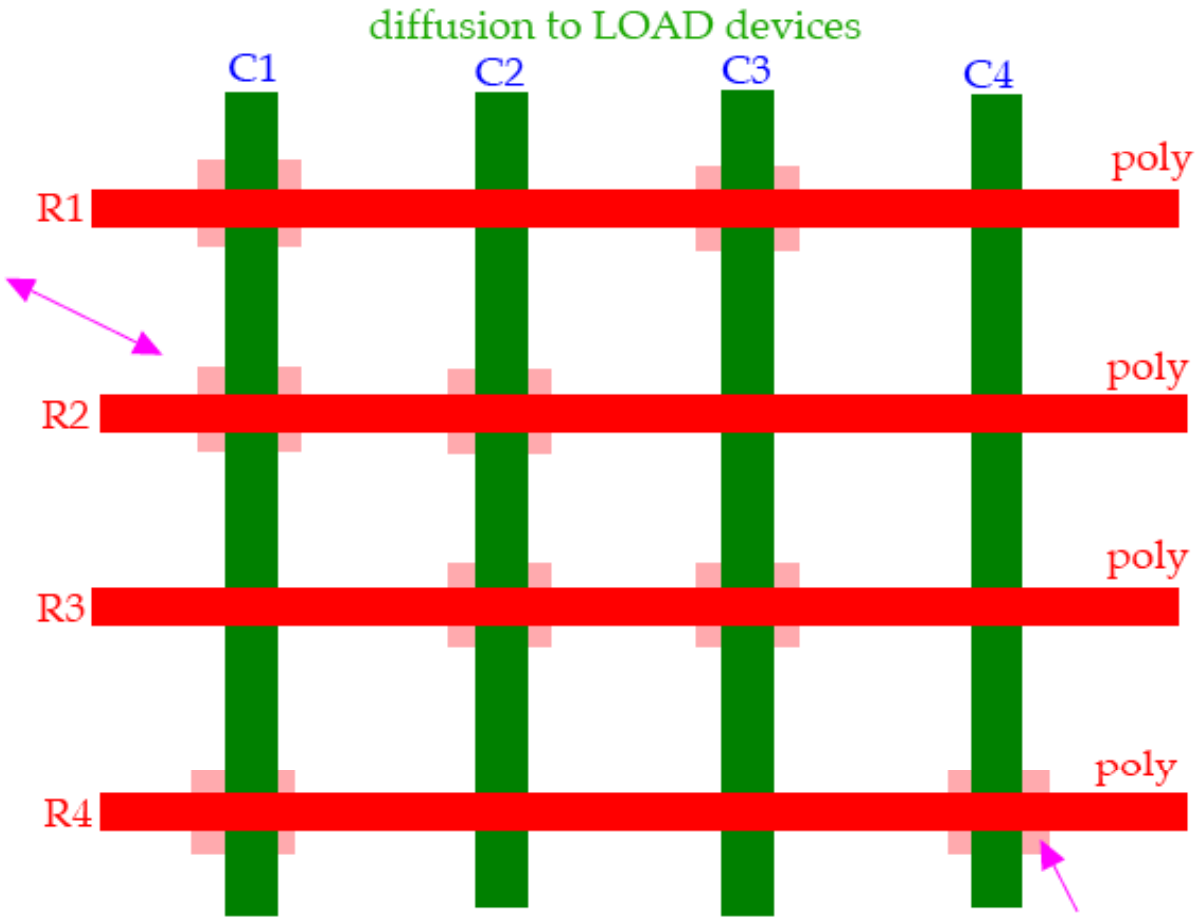
Absent Xstr => store "0"
Present Xstr => store "1"

IMPLANT - MASK PROGRAMMABLE 4 X 4 BIT NAND ROM LAYOUT

Absent Xstr => store "0" (short)

Present Xstr => store "1"





threshold voltage implant to make V_{T0} negative to store "0"

DESIGN OF ROW AND COLUMN DECODERS

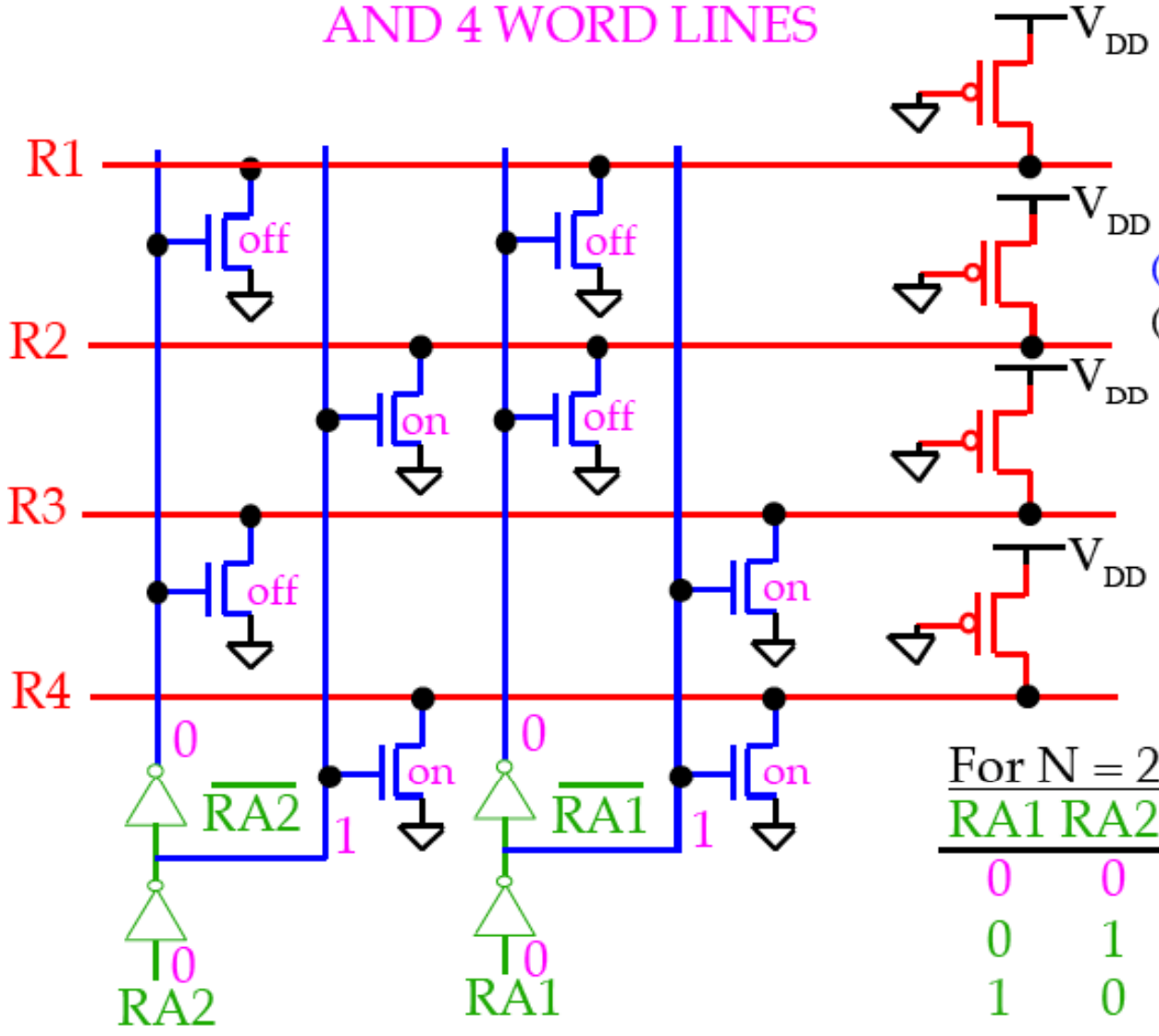
ROW ADDRESS DECODER FOR 2 ADDRESS BITS AND 4 WORD LINES EXAMPLE

RA1	RA2	R1	R2	R3	R4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

2 address bits plus complements

Select 1 of 4 rows or word lines

NOR BASED IMPLEMENTATION FOR A ROW DECODER WITH 2 ADDRESS BITS AND 4 WORD LINES



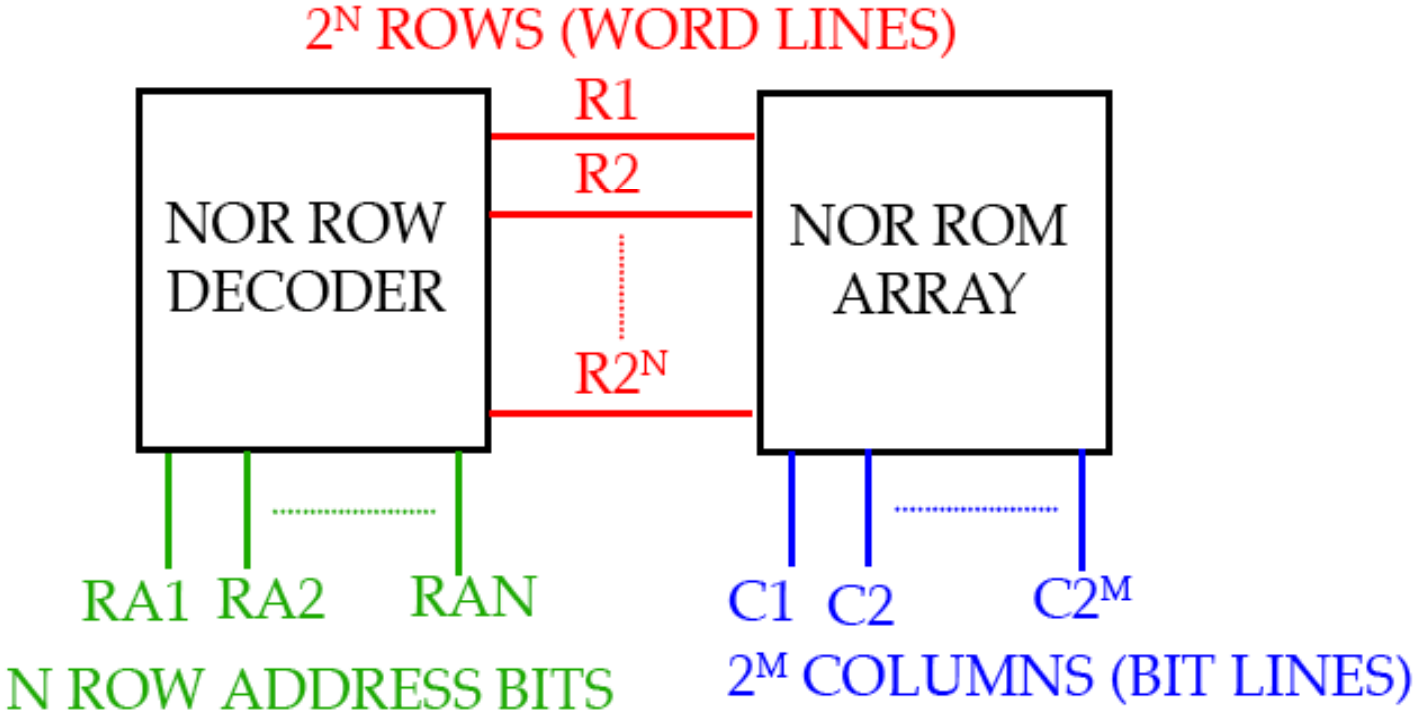
(2^N) nMOS + (N)pMOS = $(2^N + N)$ Xstrs

PLUS 2N INVERTERS

For N = 2

RA1	RA2	R1	R2	R3	R4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

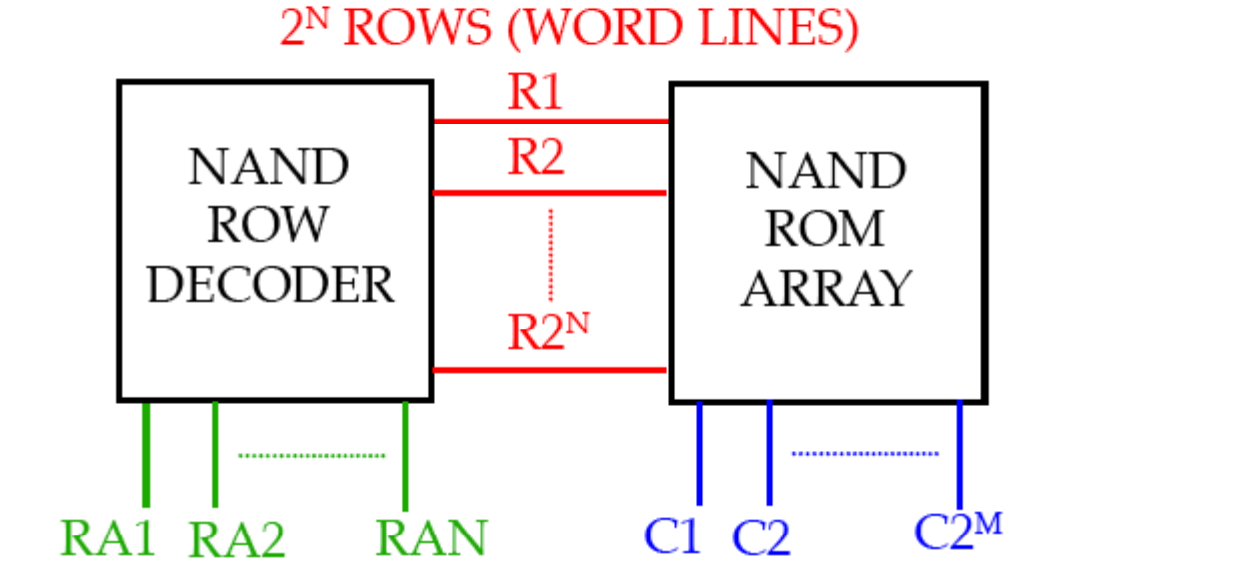
REALIZATION OF ROW DECODER AND ROM ARRAY AS TWO ADJACENT NOR PLANES



For N = 2

RA1	RA2	R1	R2	R3	R4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

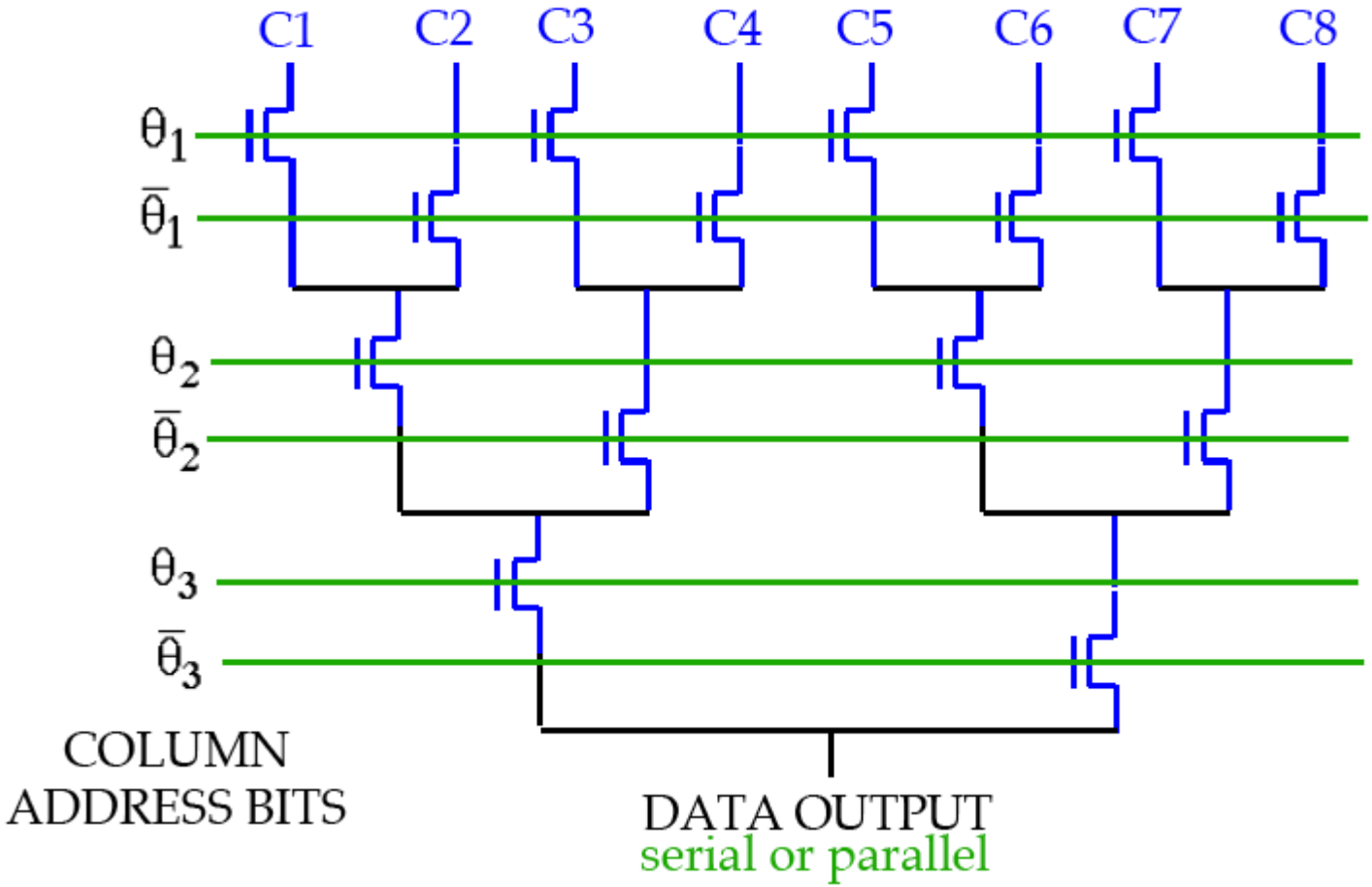
REALIZATION OF ROW DECODER AND ROM ARRAY AS TWO ADJACENT NAND PLANES



RA1	RA2	R1	R2	R3	R4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

ROW DECODER TRUTH TABLE FOR A 4X4 NAND ROM ARRAY

COLUMN DECODER FOR 8 BIT LINES IMPLEMENTED AS BINARY TREE

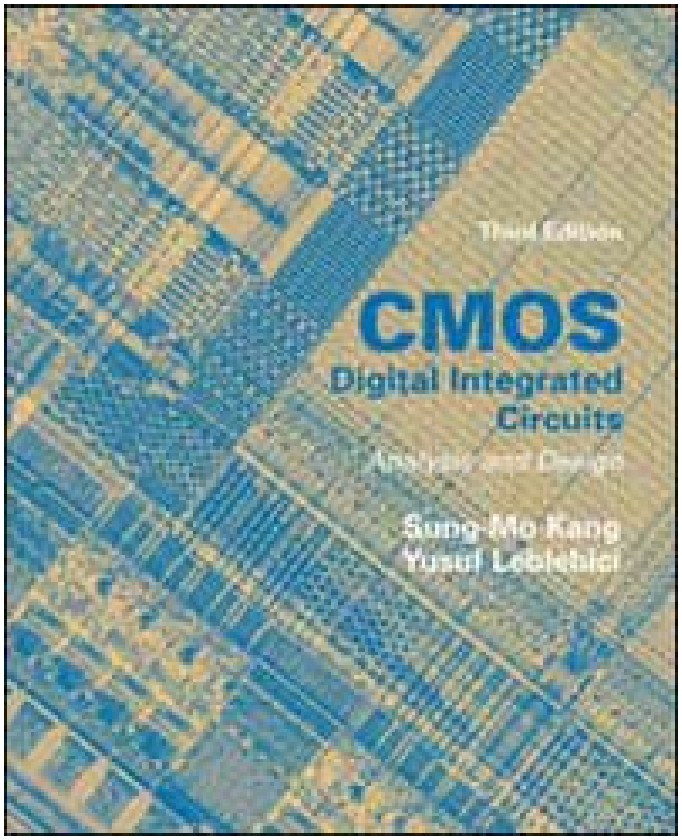


ADVG: Decoding is realized by tree structure; much reduced Xstr count.

DISADVG: Large number of series connected nMOS pass Xstrs.

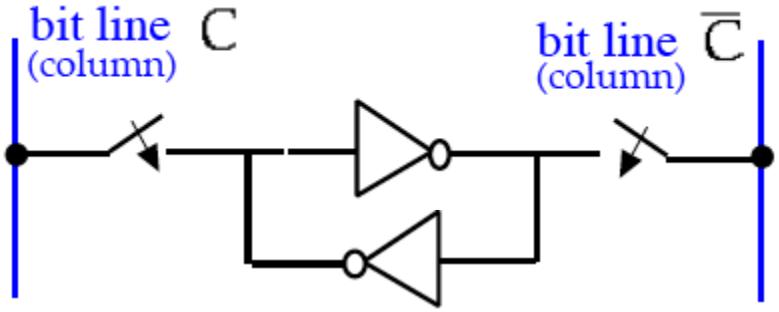
Fix with buffers or use of a combined tree and pass-transistor design.

Digital IC Design and Architecture



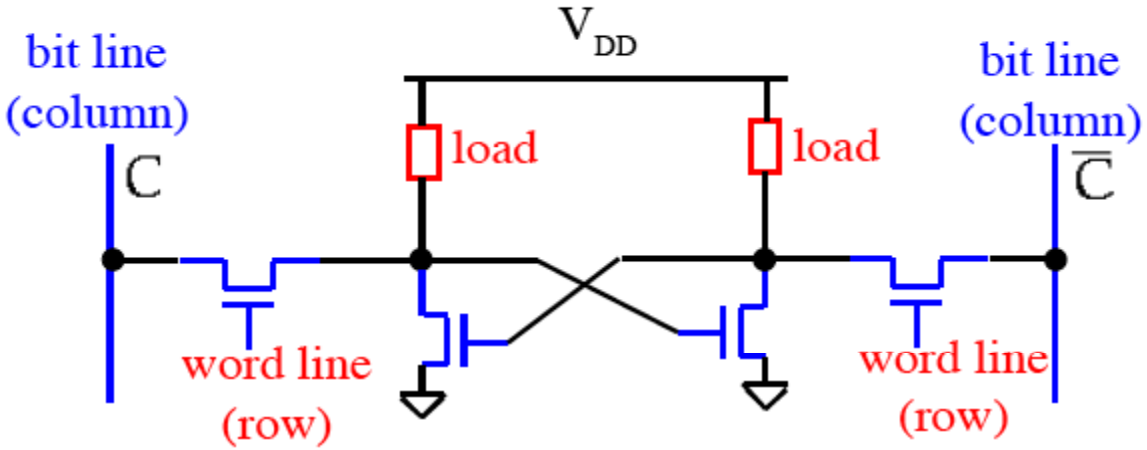
Static Random Access Memory (SRAM)

STATIC READ-WRITE MEMORY (SRAM) CIRCUITS



1 - BIT SRAM CELL

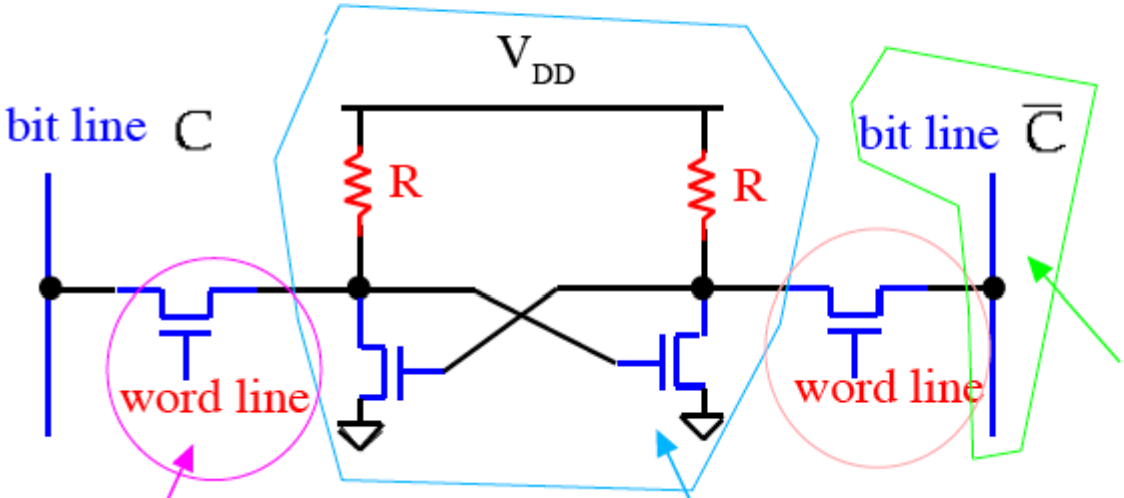
Complementary Column arrangement achieves more reliable operation



BASIC REQUIREMENTS THAT DICTATE DESIGN:

1. DATA-WRITE OP -> MODIFY STORED DATA IN SRAM CELL
2. DATA-READ OP -> NOT MODIFY STORED DATA IN SRAM CELL

RESISTIVE-LOAD SRAM CELL

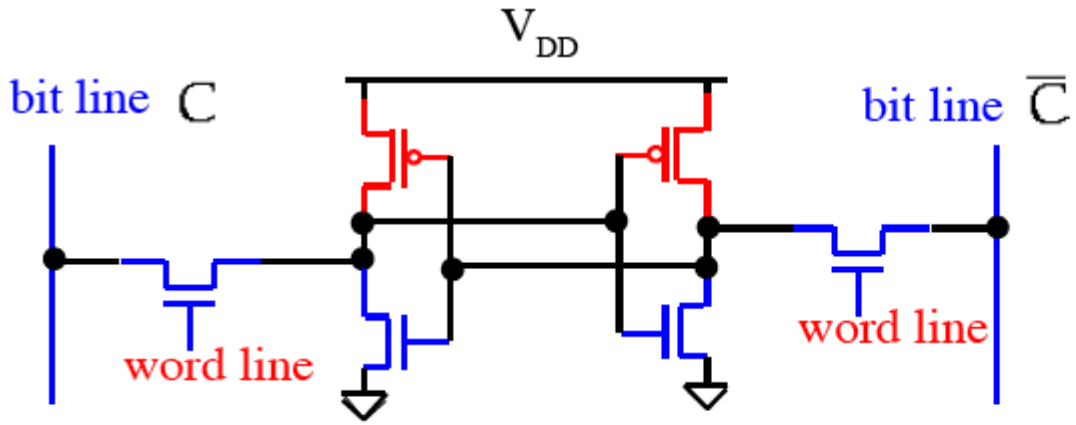


SRAM cell is accessed via two bit (column) lines C and its complement for more reliable and much faster operation

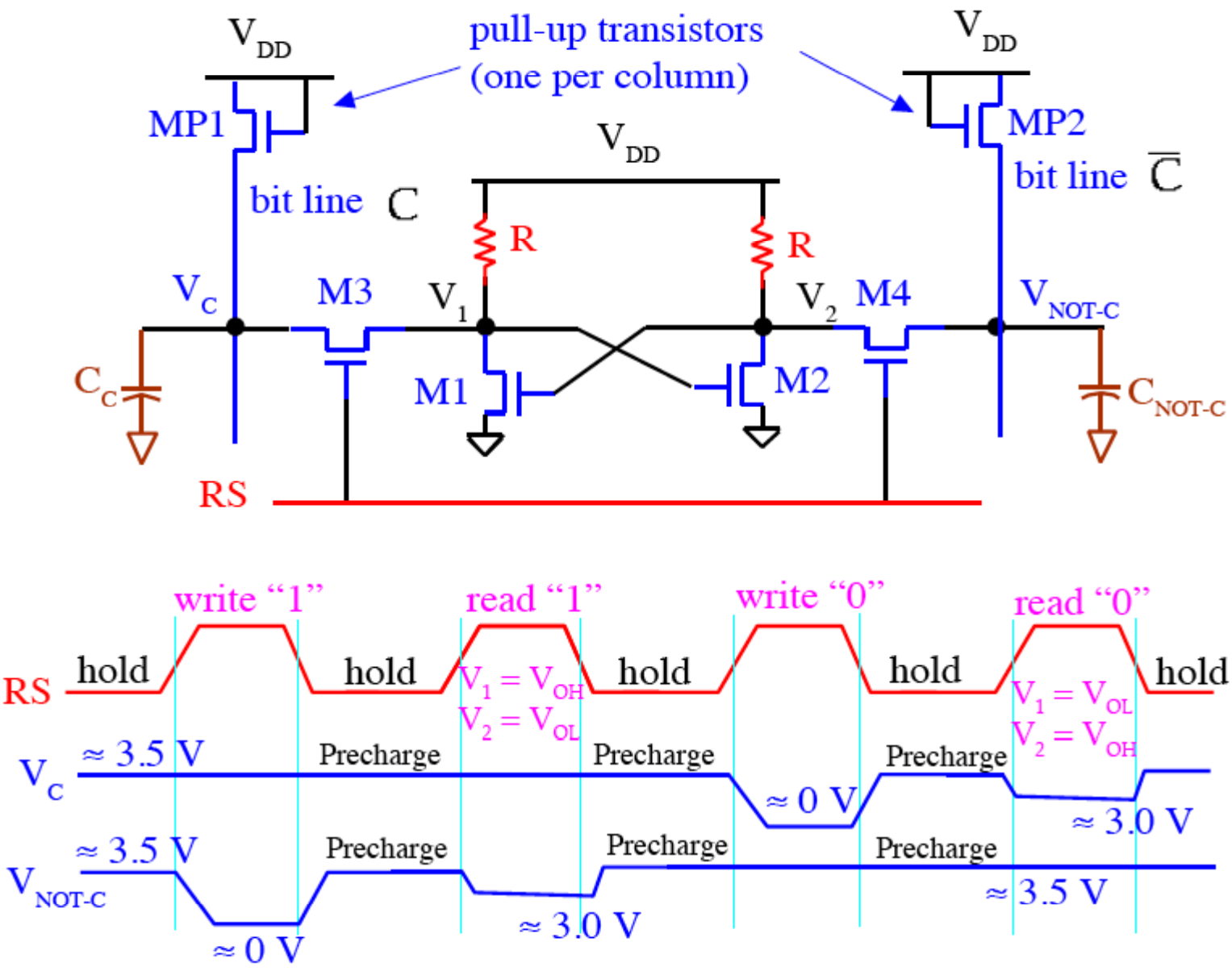
pass transistors to activated by a row select (RS) signal to enable read/write ops

basic cross-coupled 2-inverter latch with 2 stable op points for storing one-bit

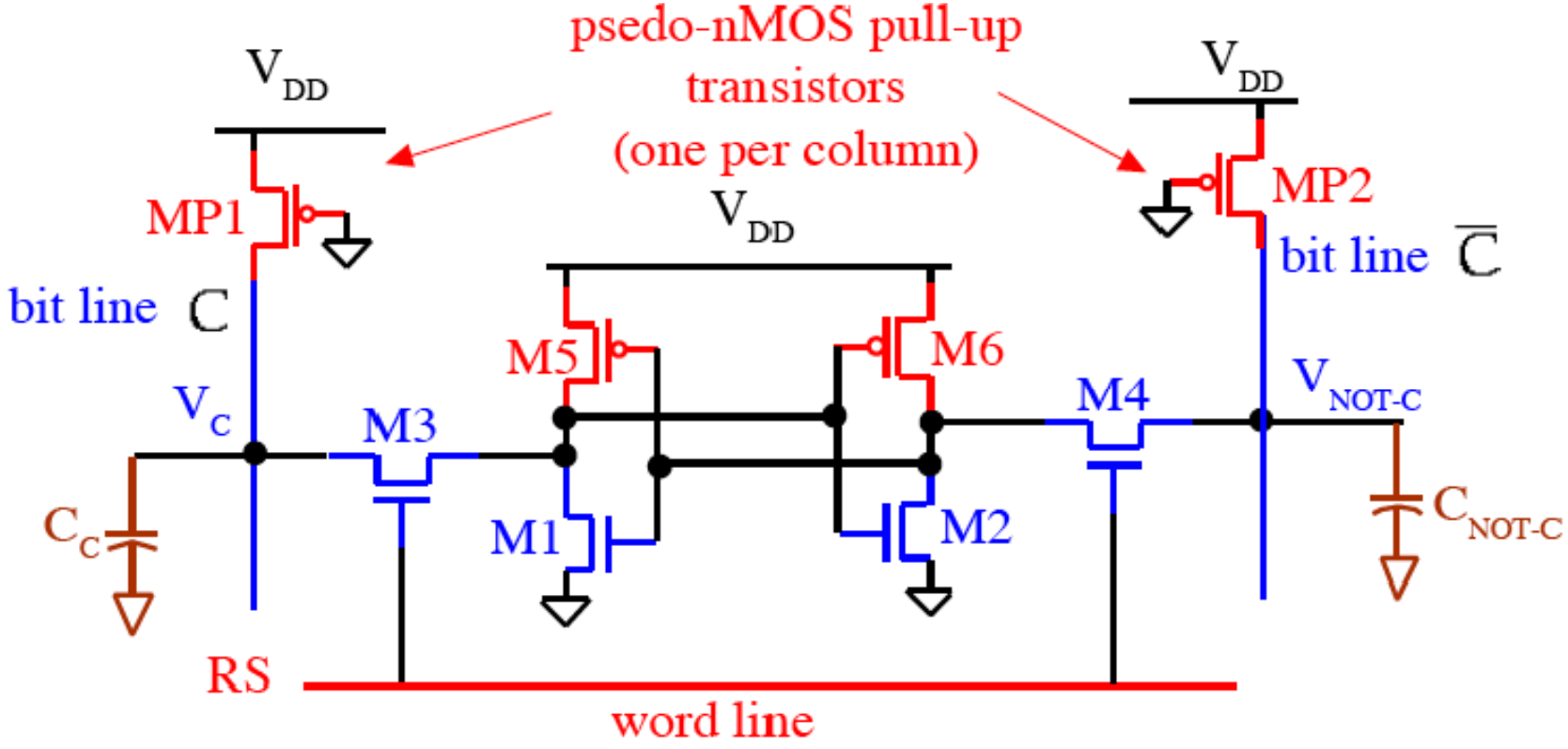
CMOS 6-T SRAM



Full CMOS SRAM Cell


V DD
pull-up transistors
(one per column)
V DD
MP1
V DD
MP2
bit line C
bit line $\overline{C}$
R
R
V C
M3
V 1
V 2
M4
V NOT-C
C C
M1
M2
C NOT-C
RS
write "1"
read "1"
write "0"
read "0"
RS
hold
hold
V 1 = V OH
V 2 = V OL
hold
hold
V 1 = V OL
V 2 = V OH
hold
V C
≈ 3.5 V
Precharge
Precharge
Precharge
≈ 0 V
≈ 3.0 V
V NOT-C
≈ 3.5 V
Precharge
Precharge
Precharge
≈ 0 V
≈ 3.0 V
≈ 3.5 V

CIRCUIT FOR CMOS SRAM CELL



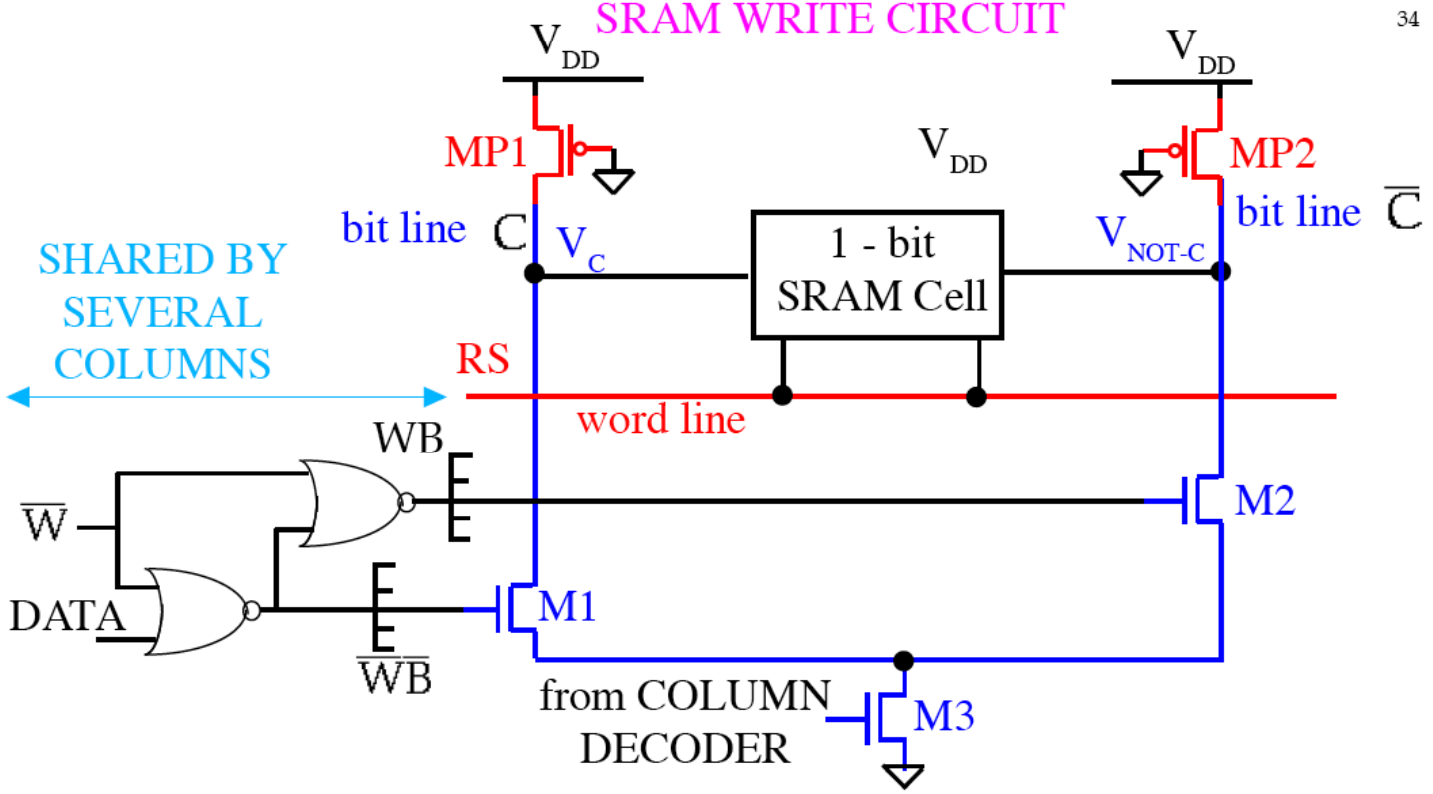
-> VERY LOW STANDBY POWER CONSUMPTION

-> LARGER NOISE MARGINS THAN R-LOAD SRAMS

-> OPERATE AT LOWER SUPPLY VOLTAGES THAN R-LOAD SRAMS

-> LARGER DIE AREA

SRAM WRITE CIRCUIT



Write OP: force V_C or $V_{NOT\text{-}C}$ to a logic low level when $\overline{W} = 0$.

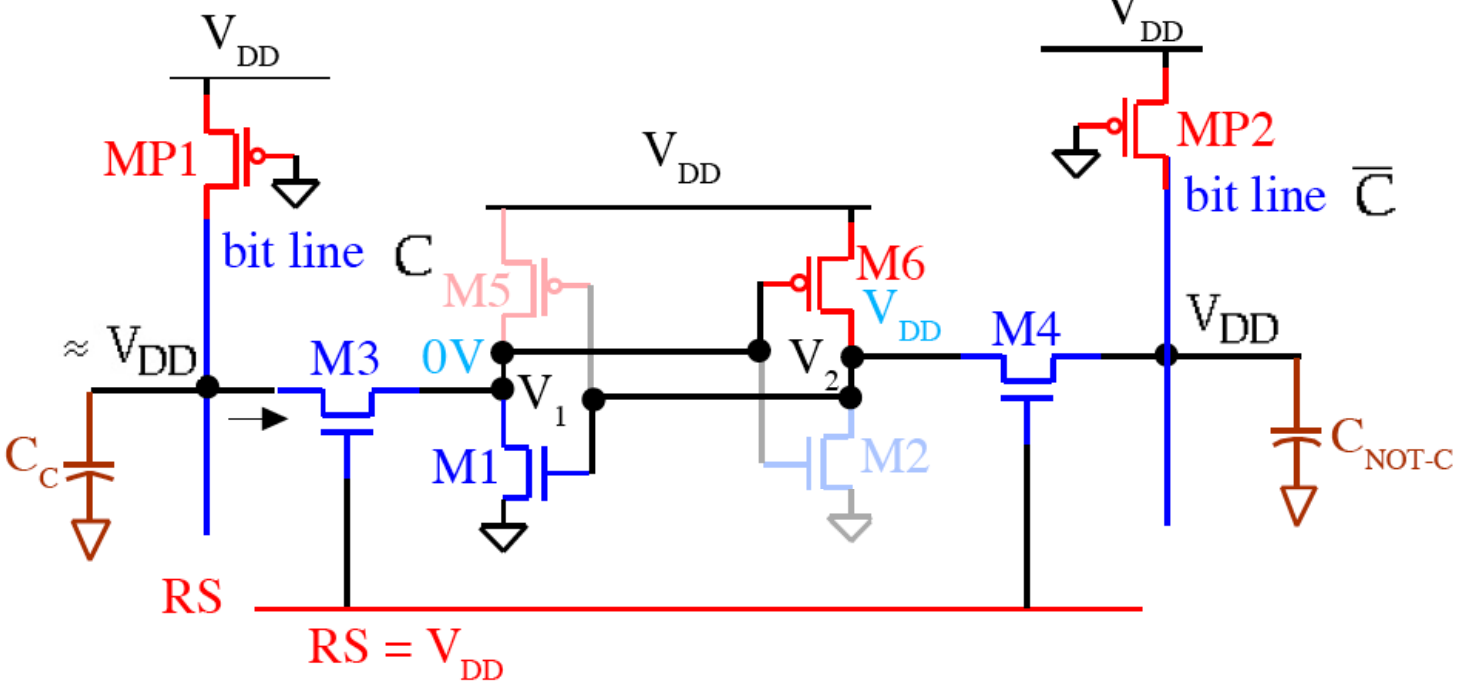
NOT-W	DATA	NOT-WB	WB	OPERATION (M3 ON)
0	1	0	1	M1 OFF, M2 ON -> $V_{NOT\text{-}C}$ LOW
0	0	1	0	M1 ON, M2 OFF -> V_C LOW
1	X	0	0	M1 OFF, M2 OFF -> $V_C = V_{NOT\text{-}C}$ HIGH

CMOS SRAM DESIGN STRATEGY

BASIC REQUIREMENTS THAT DICTATE (W/L) RATIOS:

1. DATA-WRITE OP -> MODIFY STORED DATA IN SRAM CELL
2. DATA-READ OP -> NOT MODIFY STORED DATA IN SRAM CELL

1. CONSIDER DATA-READ OP with "0" STORED IN CELL:



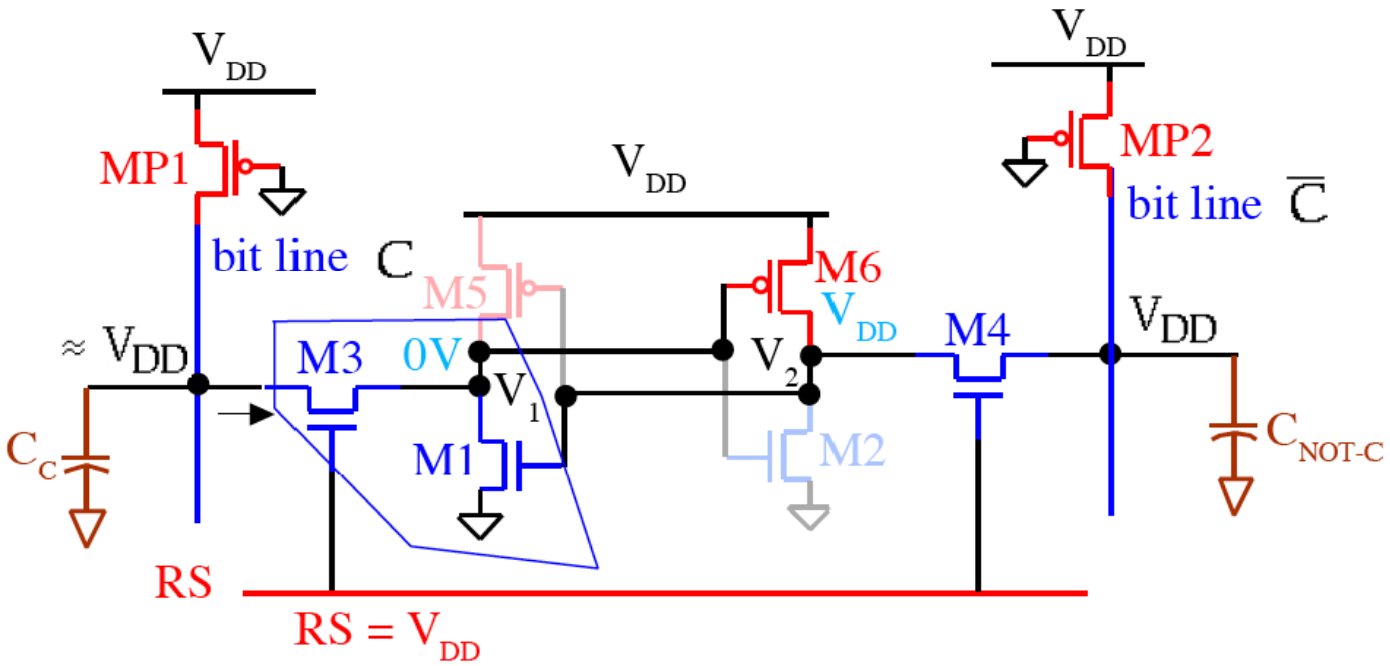
a. @ $t = 0^-$: M3, M4 OFF; M2, M5 OFF & M1, M6 LIN

b. @ $t = 0$: M3 SAT, M4 LIN; M2, M5 OFF & M1, M6 LIN

slow discharge of large C_c and V_1 increases

REQUIRE $V_1 \leq V_{T02}$ => LIMITS M3 W/L wrt M1 W/L

DESIGN FOR NON-DESTRUCTIVE DATA-READ "0" OP



DESIGN CONSTRAINT: $V_{1max} = V_{T02} = V_{T0n}$ i.e. KEEP M2 OFF

M3 SAT, M1 LIN =>

$$\frac{k_{n3}}{2}(V_{DD} - V_1 - V_{T0n})^2 = \frac{k_{n1}}{2}\left(2(V_{DD} - V_{T0n})V_1 - V_1^2\right)$$

$V_1 < V_{T0n}$:

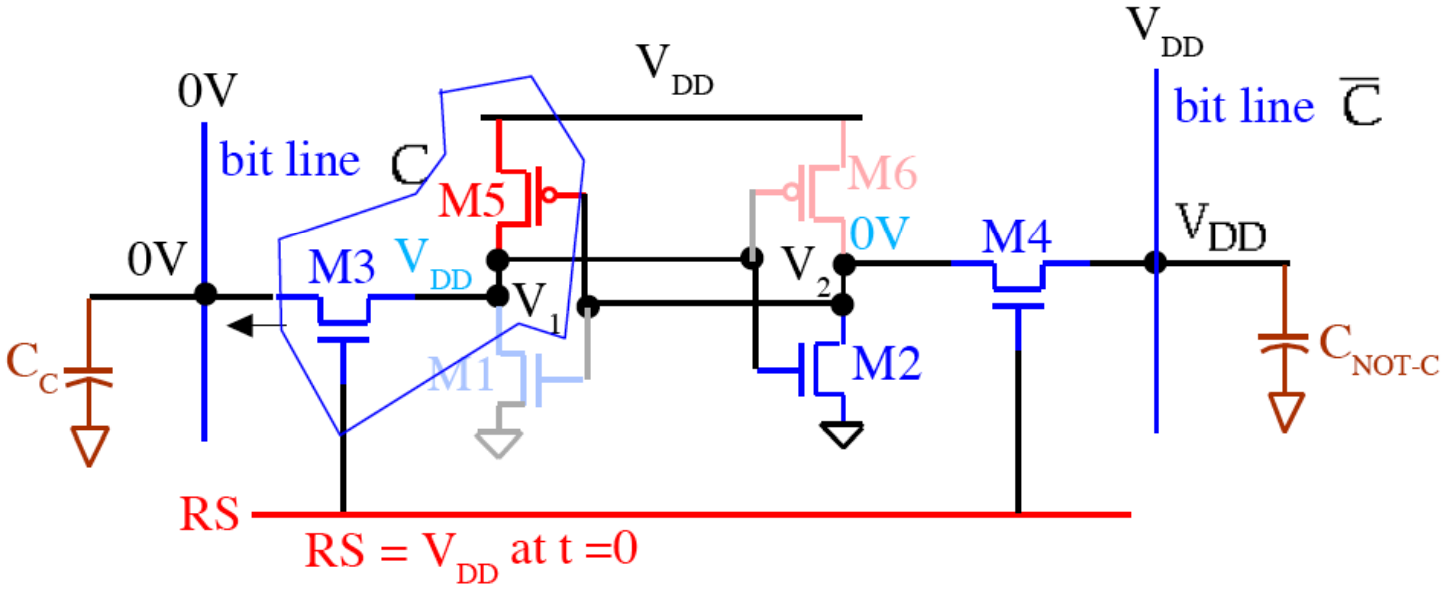
$$\frac{k_{n3}}{k_{n1}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} < \frac{2(V_{DD} - 1.5V_{T0n})V_{T0n}}{(V_{DD} - 2V_{T0n})^2} < 1$$

SYMMETRY:

SAME for $\frac{k_{n4}}{k_{n2}}$

(M1 & M6 OFF for Read '1")

2. CONSIDER DATA-WRITE "0" OP with "1" STORED IN CELL:



V_C IS SET "0" BY DATA-WRITE CIRCUIT

a. @ $t = 0^-$: M3, M4 OFF; M2, M5 LIN & M1, M6 OFF ("1" stored)

b. @ $t = 0$: M3 SAT, M4 SAT; M2, M5 LIN & M1, M6 OFF

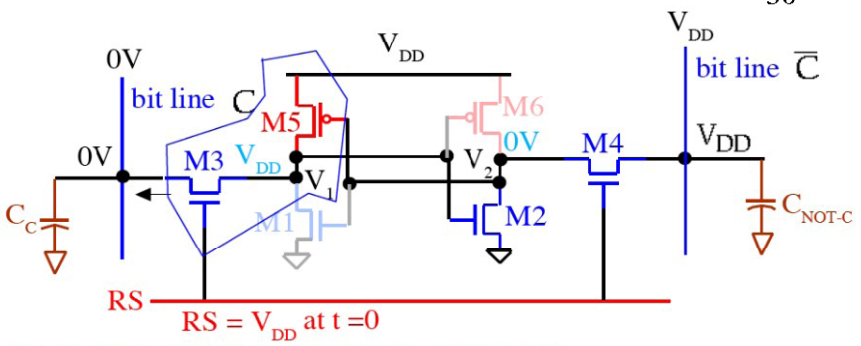
WRITE "0" => V_1: V_{DD} -> 0 (< V_{T0n}) AND V_2: 0 -> V_{DD} (M2 -> OFF)

DESIGN CONSTRAINT: $V_{1max} = V_{T02} = V_{T0n}$ i.e. KEEP M2 OFF

WHEN $V_1 = V_{1max} = V_{T0n}$: M3 LIN & M5 SAT =>

$$\frac{k_{p5}}{2}\left(0 - V_{DD} - V_{T0p}\right)^2 = \frac{k_{n3}}{2}\left(2\left(V_{DD} - V_{T0n}\right)V_{T0n} - V_{T0n}^2\right)$$

DESIGN FOR ROBUST DATA-WRITE"0" OP cont.



V_C IS SET "0" BY DATA-WRITE CIRCUIT

a. @ $t = 0^-$: M3, M4 OFF; M2, M5 LIN & M1, M6 OFF ("1" stored)

b. @ t = 0: M3 SAT, M4 SAT; M2, M5 LIN & M1, M6 OFF

WRITE "0" => V_1: V_{DD} -> 0 (< V_{T0n}) AND V_2: 0 -> V_{DD} (M2 -> OFF)

DESIGN CONSTRAINT: $V_{1max} = V_{T02} = V_{T0n}$ i.e. KEEP M2 OFF

$V_1 \le V_{T0n}$, i.e. M2 (M1) forced OFF

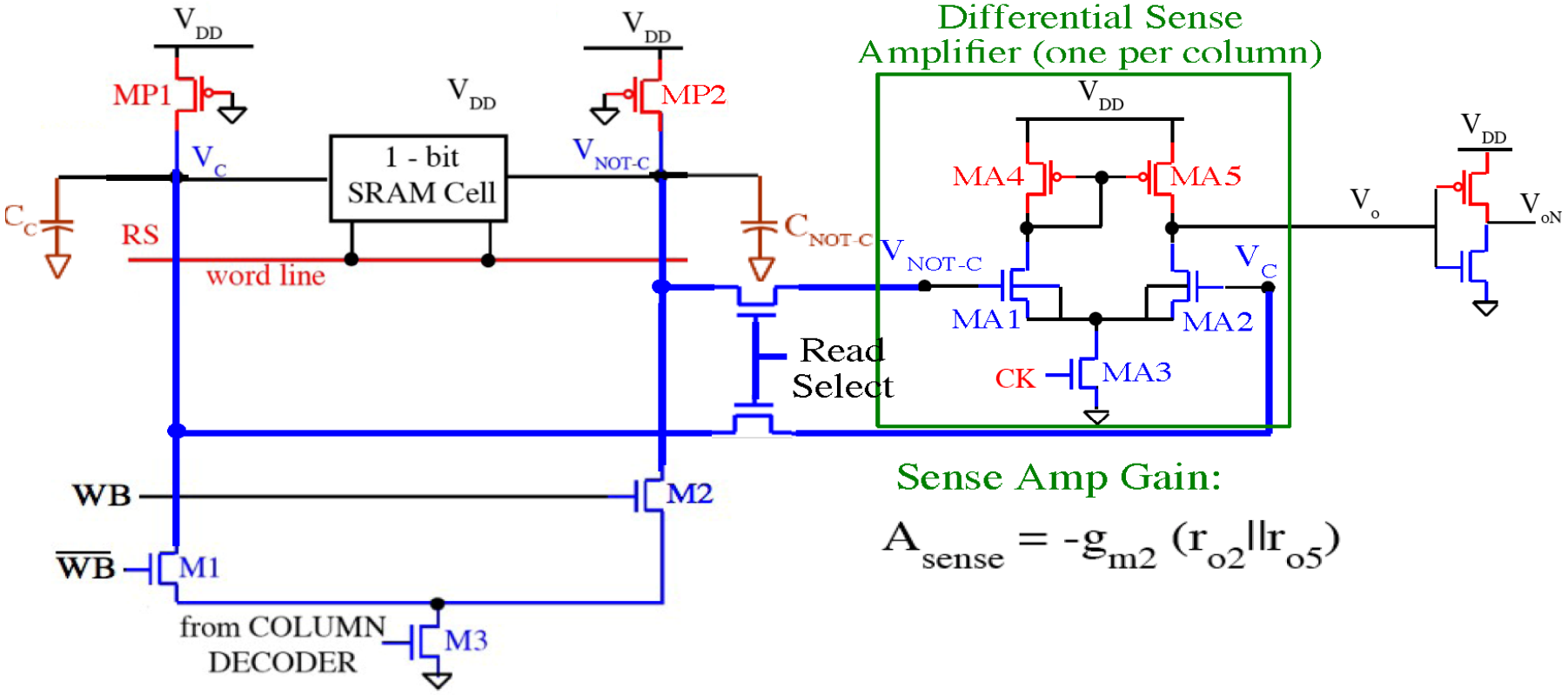
$$\frac{k_{p5}}{k_{n3}} = \frac{k_{p6}}{k_{n4}} < \frac{2(V_{DD} - 1.5V_{T0n})V_{T0n}}{(V_{DD} + V_{T0p})^2} \quad \Rightarrow$$

BY SYMMETRY to WRITE "1" when "0" is stored in cell.

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} < \frac{\mu_n}{\mu_p} \frac{2(V_{DD} - 1.5V_{T0n})V_{T0n}}{(V_{DD} + V_{T0p})^2} < 1$$

CMOS SRAM

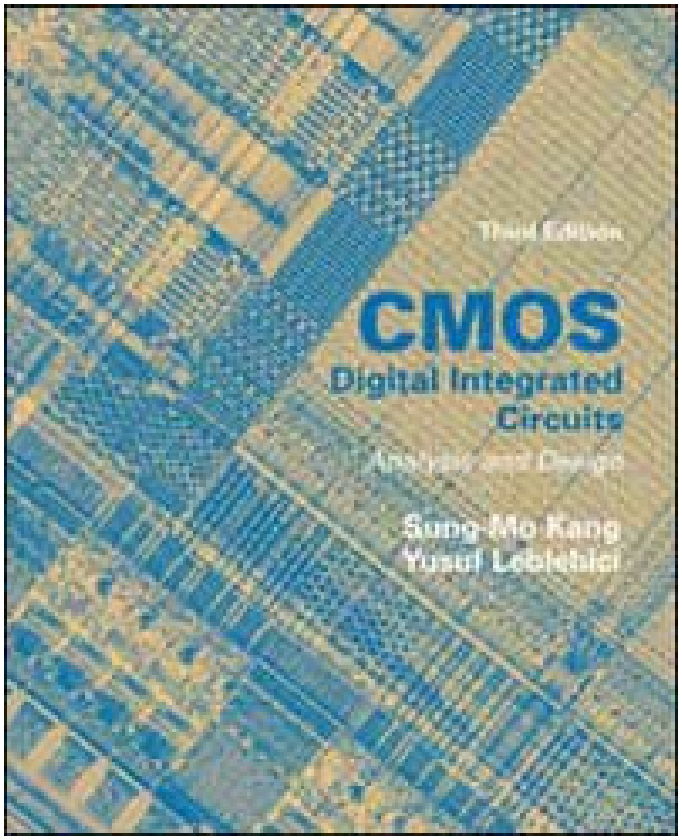
SRAM READ CIRCUIT



Sense Amp Gain:

$$A_{sense} = -g_{m2}\,(r_{o2} \| r_{o5})$$

Digital IC Design and Architecture

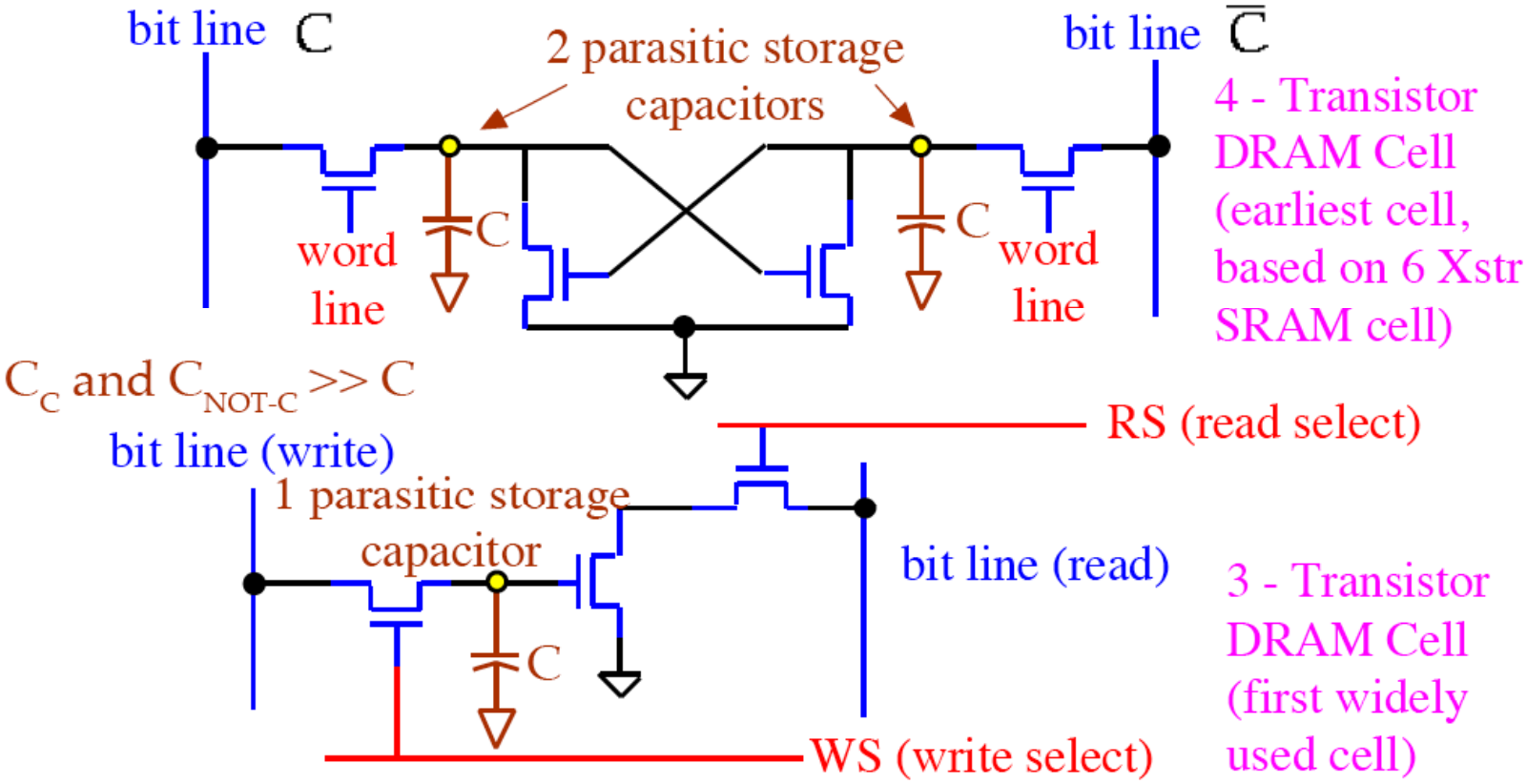


Dynamic Random Access Memory (DRAM)

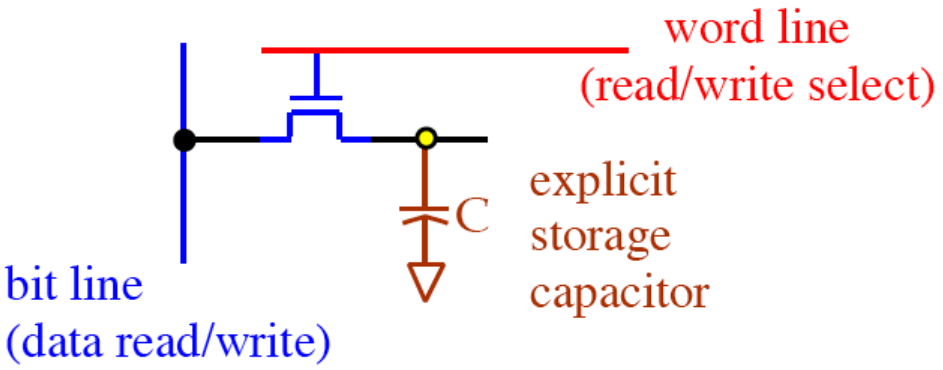
DYNAMIC READ-WRITE MEMORY (DRAM) CIRCUITS

SRAM -> 4 - 6 TRANSISTORS PER BIT
3 - 5 LINES CONNECTING EACH CELL

DRAM -> DATA BIT IS STORED AS CHARGE ON CAPACITOR
REDUCED DIE AREA VS. SRAM
REQUIRES PERIODIC REFRESH



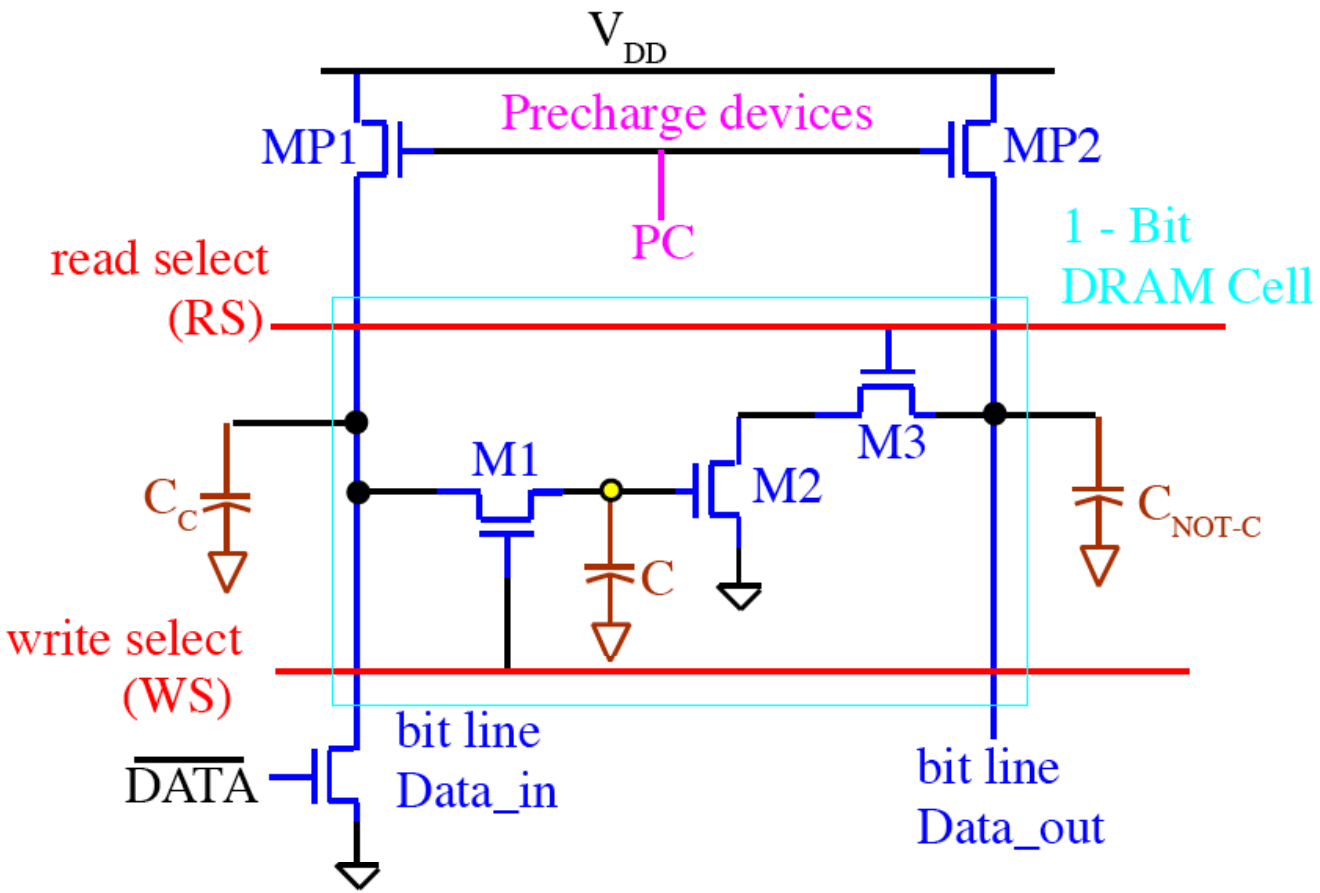
1-T DRAM Memory Cell



1 - Transistor
DRAM Cell
(most widely
used cell)

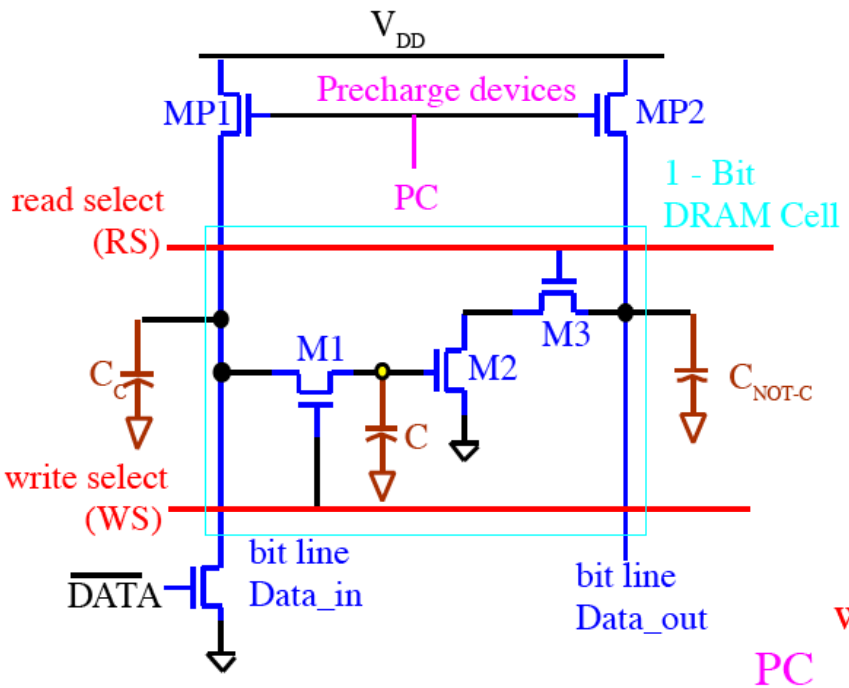
-> INDUSTRY STANDARD FOR HIGH DENSITY DRAM ARRAYS
-> SMALLEST COMPONET COUNT & SILICON AREA PER BIT
-> SEPARATE OR "EXPLICIT" CAPACITOR (DUAL POLY) PER CELL

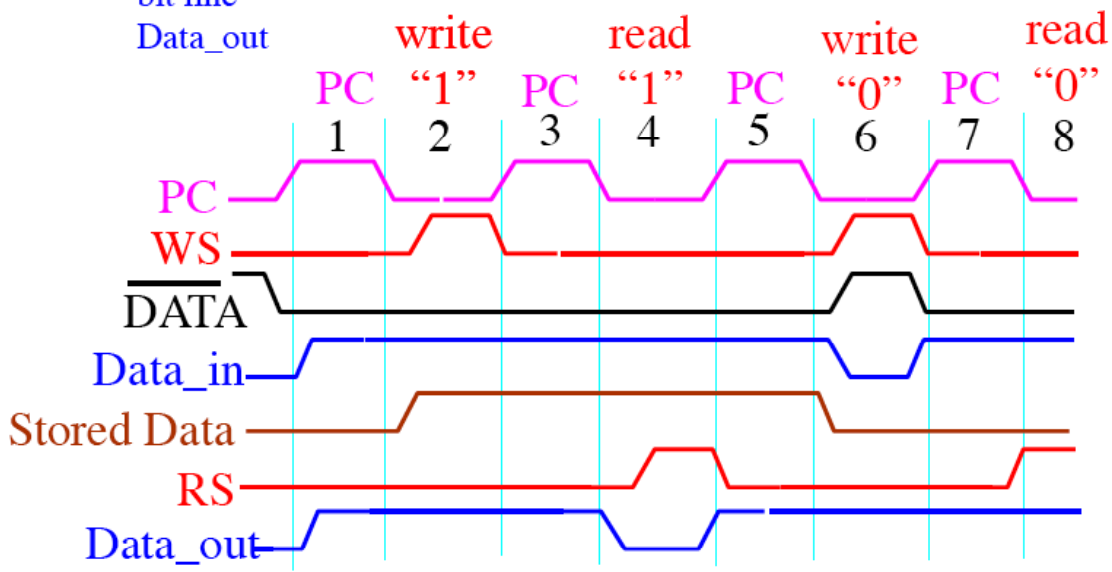
OPERATION OF 3 - TRANSISTOR DRAM CELL

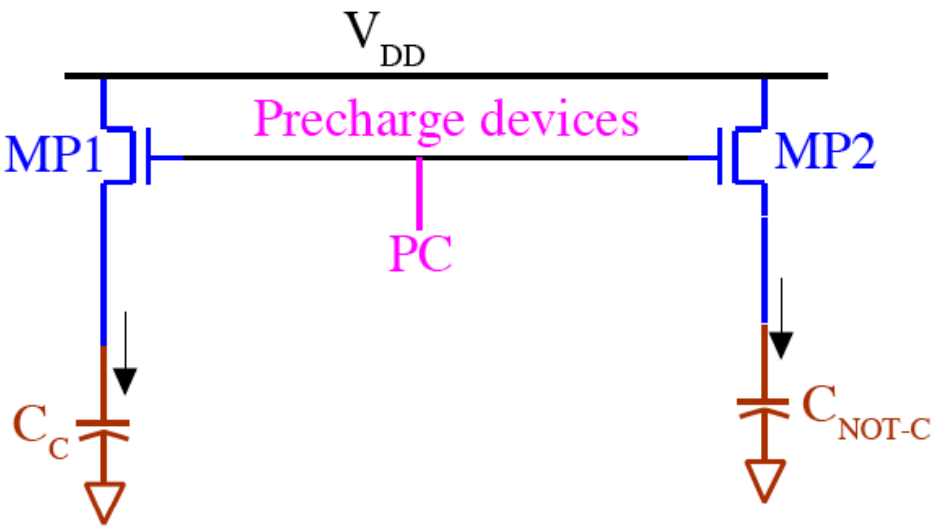


C_C, C_{NOT-C} >> C (> 10 C)

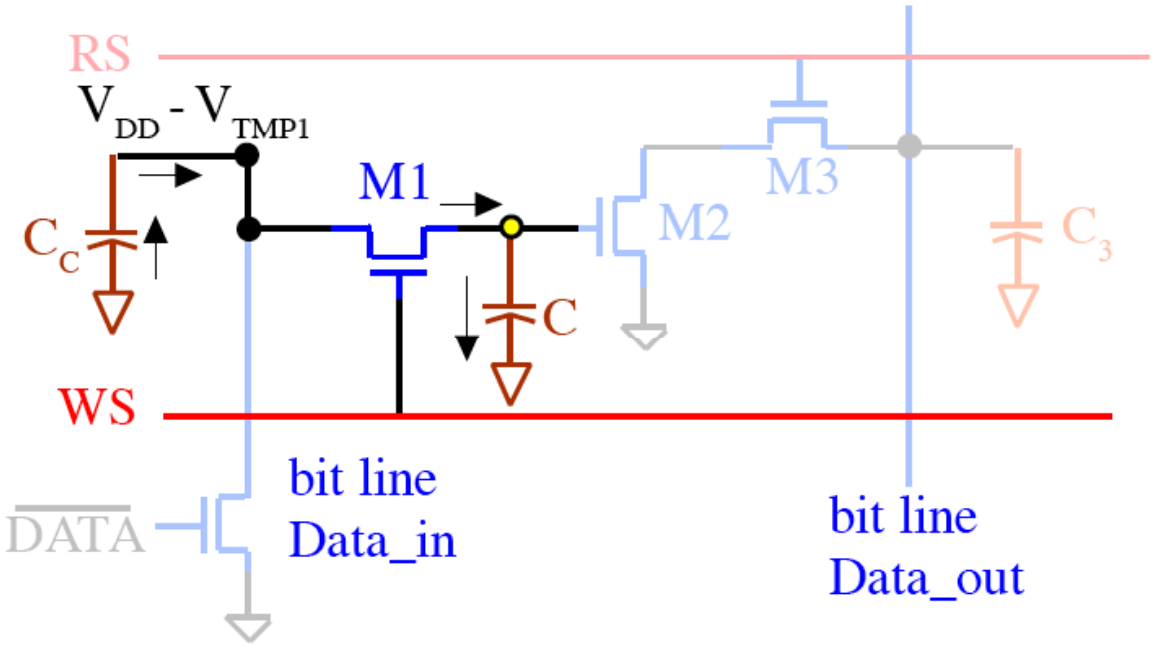
Uses two-phase non-overlapping clock scheme where $\phi 1$ = PC = precharge and $\phi 2$ = RS = read or WS = write.


V_{DD}
Precharge devices
MP1
MP2
PC
1 - Bit
DRAM Cell
read select
(RS)
M1
M2
M3
C_C
C
C_{NOT-C}
write select
(WS)
bit line
Data_in
bit line
Data_out
DATA


write
read
write
read
PC
"1"
PC
"1"
PC
"0"
PC
"0"
1
2
3
4
5
6
7
8
PC
WS
DATA
Data_in
Stored Data
RS
Data_out



PRECHARGE CYCLE

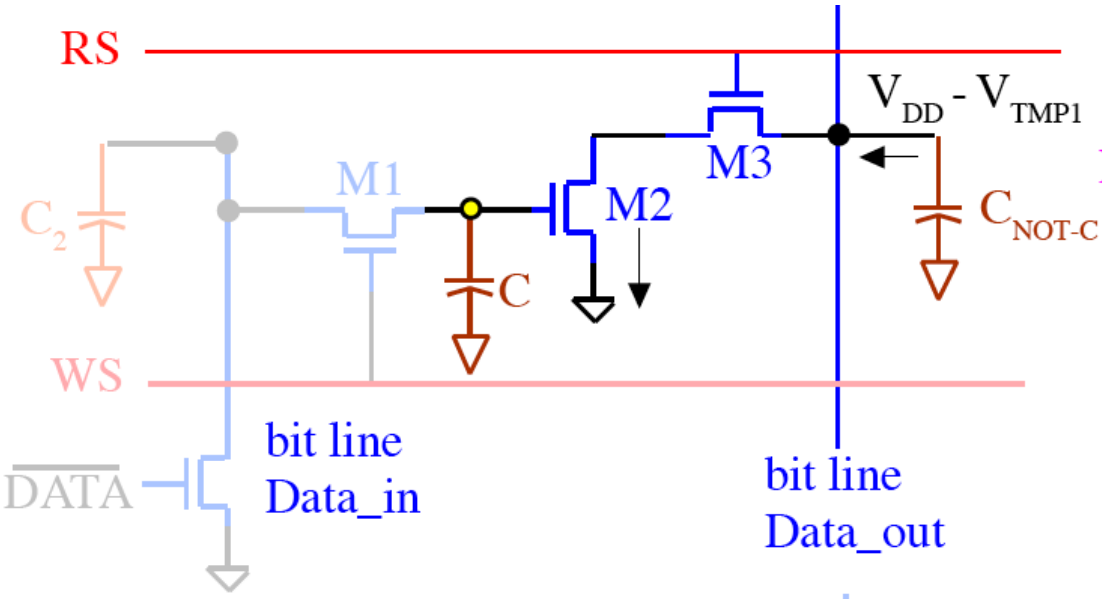


WRITE "1" OP

$\overline{DATA} = 0$

WS = 1; RS = 0

C_C, C SHARE CHARGE DUE TO M1 ON

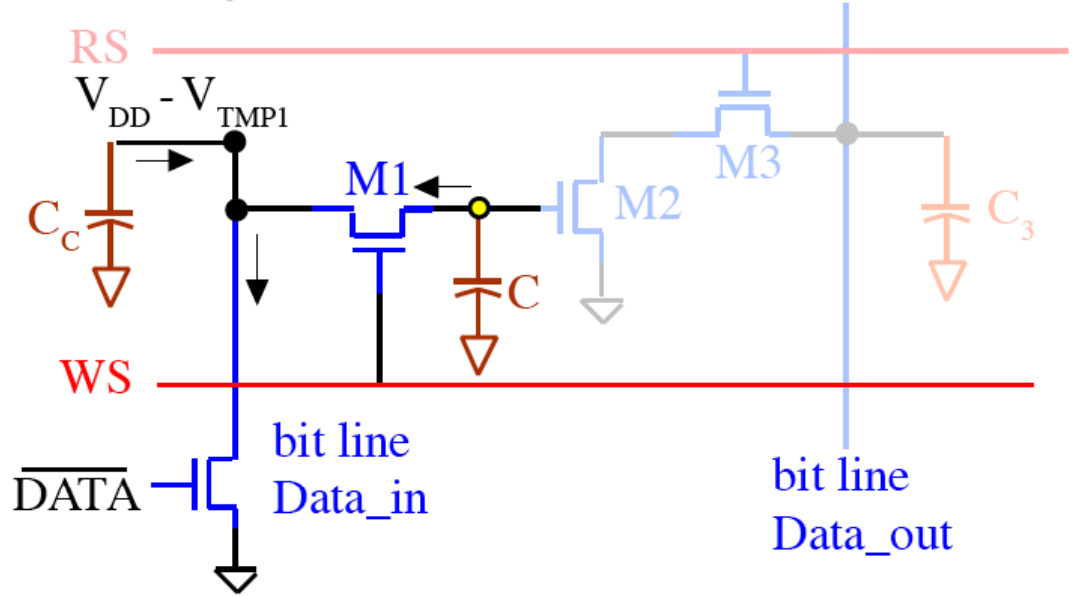


READ "1" OP

$\overline{DATA} = 0$

WS = 0; RS = 1

C_{NOT-C} DISCHARGES THROUGH M2 AND M3

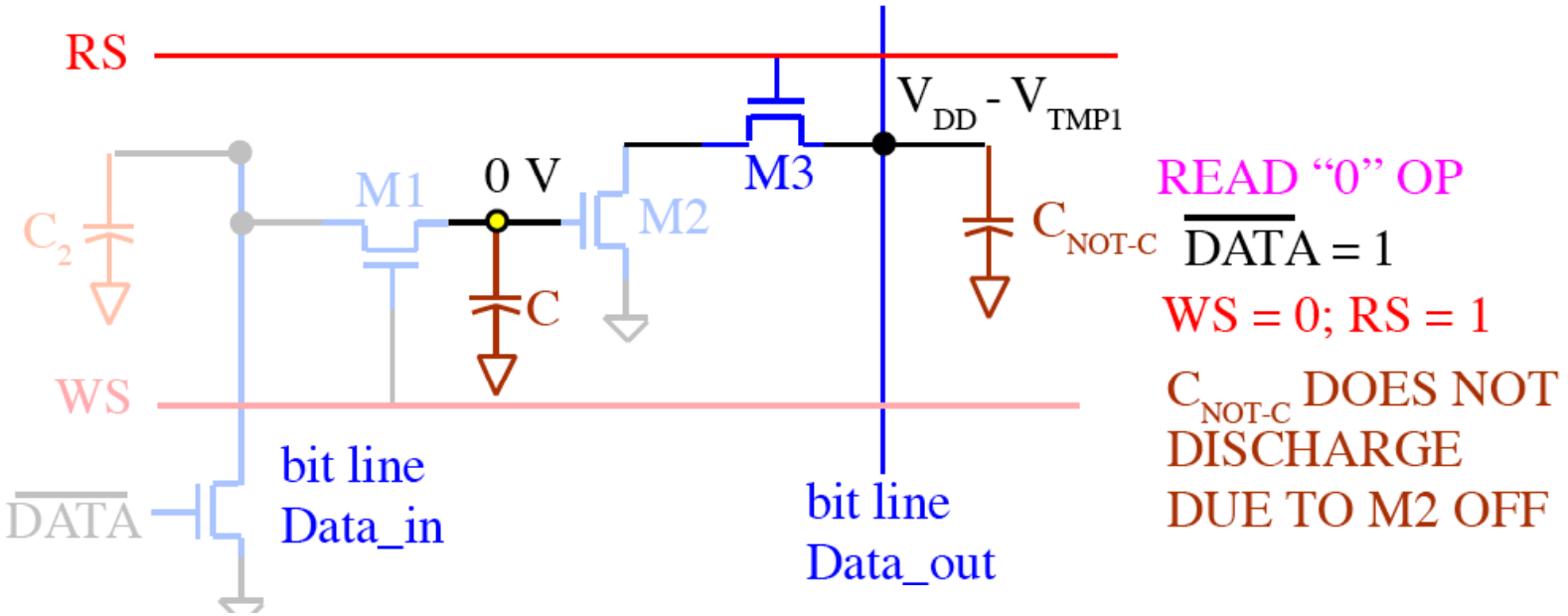


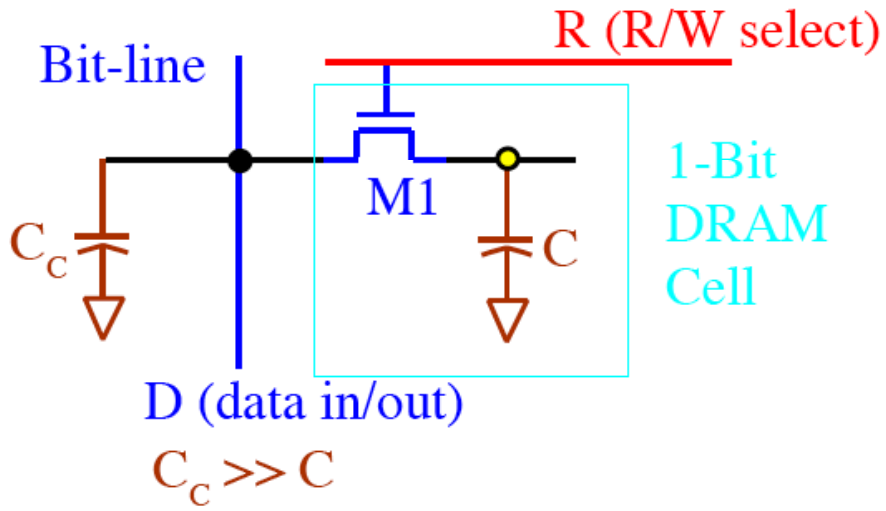
WRITE "0" OP

$\overline{DATA} = 1$

WS = 1; RS = 0

C_C, C DISCHARGED TO 0 THROUGH M1 AND DATA-IN nMOS


RS
V_{DD} - V_{TMP1}
M3
M1
0 V
M2
C_2
C
C_{NOT-C}
READ "0" OP
$\overline{DATA} = 1$
WS = 0; RS = 1
C_{NOT-C} DOES NOT DISCHARGE DUE TO M2 OFF
WS
$\overline{DATA}$
bit line
Data_in
bit line
Data_out



Uses two-phase non-overlapping clock scheme where $\phi 1$ = bit-line is precharged and $\phi 2$ = R = read/write.

WRITE "1" OP: D = 1, R = 1 (M1 ON) => C CHARGES TO "1"

WRITE "0" OP: D = 0, R = 1 (M1 ON) => C DISCHARGES TO "0"

READ OP: DESTROYS STORED CHARGE ON C => REFRESH IS NEEDED AFTER EVERY DATA READ OP