WP396 (v1.0) May 19, 2011

High-Volume Spartan-6 FPGAs: Performance and Power Leadership by Design

By: Maureen Smerdon

The rapid change in today's design environment requires a programmable solution that provides the highest performance and lowest power at the lowest cost. To meet the needs of high-volume systems, it is essential that the solution uses the latest 45 nm high-volume technology.

The purpose of this white paper is to describe how Spartan®-6 FPGAs address the needs of high-volume systems. The ability to connect efficiently and inexpensively to commodity memories, high-performance chip-to-chip interface capability, and innovative power down modes are just a few of the problems solved by high-performance, low-power, and low-cost Spartan-6 FPGAs.

Introduction

With the dramatic shifts in the market, designers of high-volume products are driven to deliver innovative systems with smaller budgets and tighter schedules. To meet these growing pressures, designers need flexible, easy to use system-on-chip type solutions.

To address the demands of the high-volume industry, Xilinx integrated design innovations derived from the successful Virtex®-5 FPGA architecture into Spartan-6 FPGAs. The Spartan-6 family offers high-volume system designers multiple advantages not found in alternative products. These advantages include:

- 45 nm Process Node
  - The industry's only high-volume FPGA family on 45 nm process node to deliver lowest cost and power with optimal performance.
- High-speed I/O
  - Highest performance chip-to-chip interfaces with 1,080 Mb/s LVDS and 3.2 Gb/s serial transceivers.
- Power-down Modes
  - The industry's lowest power, high-volume FPGA with innovative power-down capabilities.
- Embedded Memory Controller
  - Offering unparalleled memory interface speeds, e.g., DDR3 at 800 Mb/s.
- Comprehensive Targeted Design Platforms
  - Comprised of the silicon (FPGAs), development tools, IP, boards, and targeted reference designs, enabling faster time to market and differentiated products with less risk and cost.

Spartan-6 FPGAs deliver these requirements for high-volume applications like flat-panel displays, multifunction printers, industrial and home networking, automotive infotainment, motor control, portable medical and industrial instruments, D-SLR cameras and camcorders, eReaders, set-top boxes, software defined radios, and video surveillance.

Solving Key Challenges

Key technological breakthroughs have enabled the Spartan-6 family to redefine high-volume, high performance, and low power FPGAs. Spartan-6 FPGAs allow designers new-found flexibility in a low-cost FPGA family with tremendous capabilities in the areas of transceivers, DSP, high-speed I/O, clock management, security, memory capacity, and control. With Spartan-6 FPGAs, designers no longer have to choose between low-cost, low-capability FPGAs versus higher cost, feature-rich FPGAs.

As an example, Spartan-6 FPGAs offer high-speed serial transceivers, configurable I/O, dedicated memory controllers, and dedicated DSP capabilities that enable flat panel display manufacturers to improve image quality, reduce power consumption, reduce cost, and quickly implement design changes. The flexibility of the Spartan-6 FPGAs enables design teams to implement mainstream and emerging serial protocols in their designs with power and cost benefits that are not available in ASICs and ASSPs. With Spartan-6 FPGAs, flat panel display designers can implement

complex local dimming and illumination compensation algorithms for LED backlighting controllers, and produce direct-type illumination displays with differing numbers of LED zones as well as different arrangements of LEDs. Additionally, design teams can use Spartan-6 FPGAs to adjust illumination to match the physical properties of panels produced by different suppliers and add 3D capability to displays. A combination of Xilinx and 3rd party IP plus the Spartan-6 FPGA Consumer Video Kit accelerates the designers' ability to implement design modifications and add end-product differentiation features. Spartan-6 FPGA reprogrammability enables rapid deployment of advanced image enhancement algorithms and feature differentiation for a wide range of end-product price points. See the Spartan-6 FPGA usage in the 3DTV application example in Figure 1.

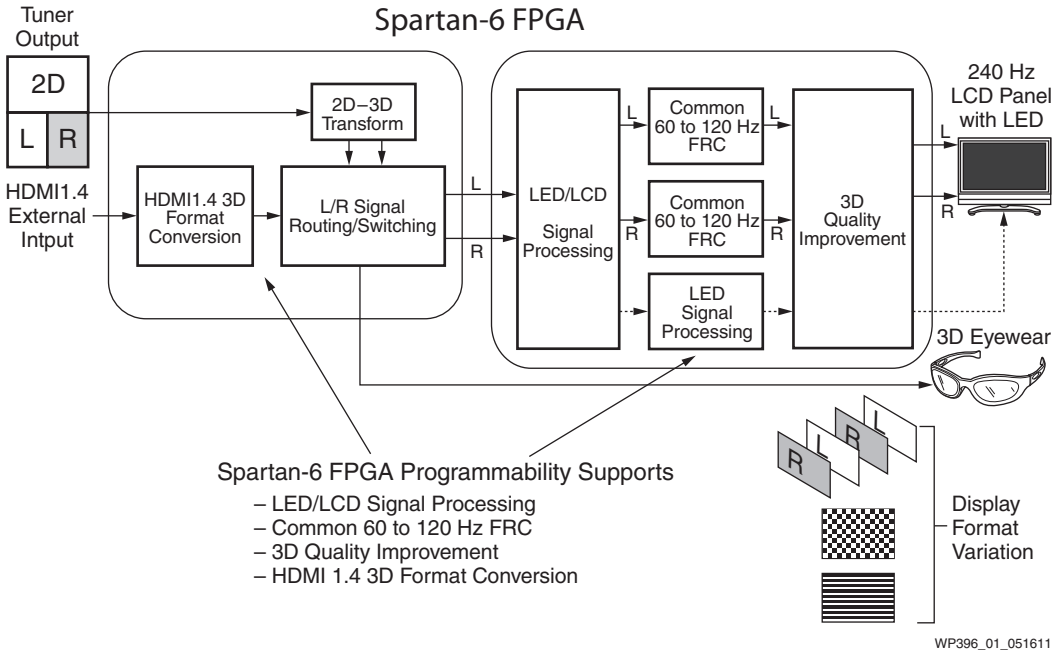

Figure 1: **Two Spartan-6 FPGAs Used in 3DTV Application**

To learn more about the availability of V-by-One HS, DisplayPort LogiCORE™ IP Tx/Rx IP cores, Imaging Processing and Video Processing solutions, and other Spartan-6 FPGA design kits visit the Spartan-6 FPGA web page: http://www.xilinx.com/products/boards_kits/spartan6.htm.

Integrated High-Speed Serial Transceivers Reduce Cost

Today's systems require significantly higher bandwidth for interfacing chip-to-chip across backplanes and long distance transmission over fiber optics. Parallel I/O reaches a speed limit around 1 GHz for single-ended pins and below 1.5 GHz for LVDS differential pin pairs, even with the latest standards.

Wide parallel connections also consume a significant number of I/O and the receivers burn a large amount of power. These connections create skew between data lanes as well as between clock and data lanes. Ultimately, this introduces crosstalk and other signal integrity issues.The integrated high-speed serial transceivers found in Spartan-6 LXT FPGAs solve all these problems.

The Spartan-6 LXT FPGAs complement low-cost logic capability with high-speed serial connectivity, which has up to eight GTP transceivers (3.2 Gb/s line rate).

Capitalizing on the vast SerDes capabilities in the Virtex FPGA families, Spartan-6 LXT devices deliver protocols at 3.2 Gb/s and below. See Table 1 for key transceiver protocol support comparisons.

Table 1: **Transceiver Protocol Support**

Speed	Spartan-6 FPGA High-Speed Serial Standards
3.125 Gb/s	XAUI, SRIO
3.072 Gb/s	OBSAI, CPRI
3.0 Gb/s	SAS II, SATA II, V-by-One
2.97 Gb/s	3G-SDI
2.7 Gb/s	DisplayPort
2.5 Gb/s	PCIe G1.1, Infiniband
2.488 Gb/s	OC-48
2.125 Gb/s	2G Fibre-Channel
1.485 Gb/s	HD-SDI
1.25 Gb/s	1 GbE

Another advantage unique to the Spartan-6 LXT FPGAs is that its logic interface is nearly identical to the interfaces of the Virtex-5 and Virtex-6 FPGA GTP transceivers, facilitating porting of designs to the lower cost Spartan-6 FPGAs. As listed in Table 1, Spartan-6 LXT FPGAs support a broad range of standards, supporting today's higher performance designs.

High Performance I/O Standards Simplify System Design

The Spartan-6 FPGA leads in I/O performance and functionality with the broadest support in its class. To support the wide range of I/O requirements found in high-volume systems, Spartan-6 FPGAs provide the fastest in class with LVDS—up to 1,080 Mb/s. This offers a significant advantage compared to Altera's Cyclone IV GX at 840 Mb/s. The Spartan-6 FPGA I/O enables a broad range of new applications, including but not limited to HD video, display, and other high-bandwidth interfaces. In addition to the LVDS I/O, Spartan-6 FPGAs have dedicated clock routing to reduce duty-cycle distortion and serializing/deserializing I/O, enabling up to 1:8 serial-to-parallel data conversion for easier-to-design high-speed differential interfaces. For detailed I/O standard support comparison details, see Table 2.

Table 2: **I/O Standard Support Comparison**

I/O Standards	Spartan-6 FPGA	Cyclone IV GX[1]
LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)	✓	✓
LVDS and Bus LVDS	✓[2]	✓
LVPECL (2.5V, 3.3V)	✓	✓[3]
PCI	✓	✓
I2C	✓	
HSTL (1.8V, 1.5V, Classes I, II, III)	✓	
HSTL_I_12 (unidirectional only)		✓
PPDS	✓	✓
TMDS	✓	
RSDS	✓	✓
Display Port Aux Channel	✓	
SSTL (3.3V, 2.5V, 1.8V, 1.5V Classes I, II)	✓	✓
DIFF_SSTL	✓	
DIFF_HSTL	✓	
LVTTL	✓	✓

Notes:

1. Source: Cyclone IV Handbook December 2010.
2. Sub LVDS is available upon request. Contact your local Xilinx Sales Representative for more information.
3. LVPECL supported only on dedicated clock input**s.**

Spartan-6 FPGAs also support true 3.3V standards with full 4.4V overshoot support and offer full 3.3V LVCMOS and LVTTL 24 mA output drive. Supporting true 3.3V standards simplifies board design with standard tolerance components and enables design teams to design the standards into high-speed environments with minimal simulation and reduced overshoot concerns. Designers using competing FPGAs need to overcome the limited output drives and the reduction of overshoot by adding buffers for high fanout signals or line drivers for backplanes and tighter board traces, thus adding to total system complexity, cost, and design time.

Spartan-6 LX devices only require two power rails—further simplifying and lowering system design costs. Lower power-supply complexity (fewer, cheaper regulators, and reduced bypass requirements) not only makes the board less expensive and more reliable, but easier to design. Designers who are using Spartan-6 FPGAs do not need to address power-rail isolation, tantalum capacitors, and ferrite beads for every power pin. With true 3.3V I/O capability, higher drive strength, and fewer power rails, system and board design is easier and lower cost with Spartan-6 FPGAs.

To learn more about Spartan-6 FPGA SelectIO™ technology go to UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*

Superior Logic Performance and Architecture Efficiency

To meet the high-volume industry's demands, it is essential that FPGAs for these applications provide the highest performance possible with the lowest cost logic architecture. The optimized Spartan-6 FPGA logic architecture meets these demands by using a dual-register 6-input look-up table (LUT) structure. The traditional 4-input LUT used by other FPGA families can provide an adequate solution for simple functions, but the increased logic cell capability of the 6-input LUT (with an additional flip-flop) minimizes the required levels of logic, reducing delay and improving system through-put by up to 25%. See Figure 2 for details on the LUT architectural comparison.

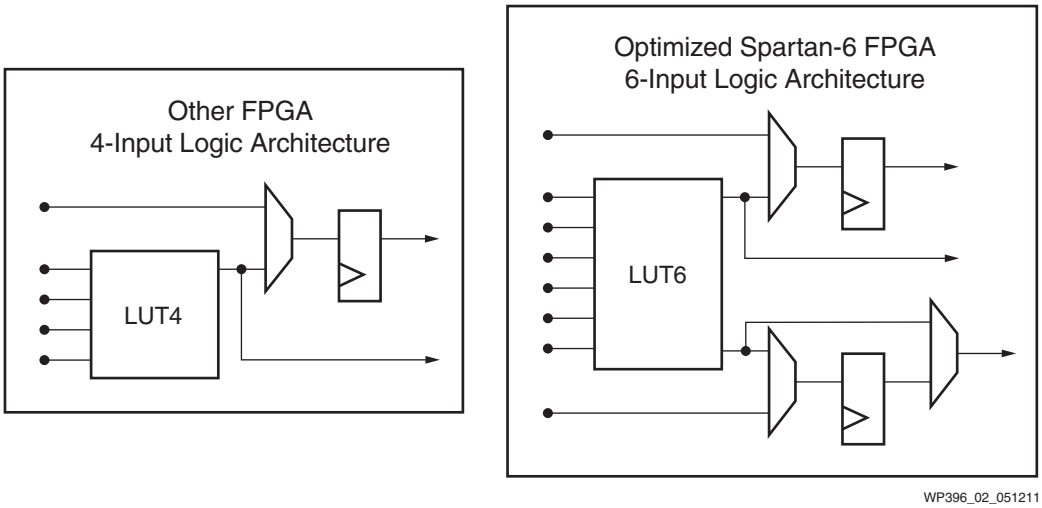

Figure 2: **6-Input LUT versus 4-Input LUT Alternative**

Design comparisons on logic performance also show a significant benefit with Spartan-6 FPGAs. Table 3 is the result of running a suite of benchmark designs using current tools from both Xilinx and Altera. Against all three speed grades, Spartan-6 FPGAs are faster versus the equivalent Cyclone IV devices.

Table 3: **FPGA Performance Benchmarking**

Speed Grade Benchmark[1]	Spartan-6 FPGA Advantage
Spartan-6 FPGA -2 speed grade vs. Cyclone IV -8	20%+ faster
Spartan-6 FPGA -3 speed grade vs. Cyclone IV -7	19% faster
Spartan-6 FPGA -3 speed grade vs. Cyclone IV -6	12% faster

Notes:

1. Using Xilinx ISE® 13.1 software and Quartus 10 Altera tools across a suite of 392 designs.

Integrated Memory Controller for 2X Greater Performance

Spartan-6 FPGAs are the only high-volume, low-cost FPGAs with hardened memory controller blocks (MCBs) for the lowest power and highest performance. All but the smallest Spartan-6 device include dedicated MCBs, with each MCB supporting DRAM standards (LPDDR, DDR, DDR2, and DDR3). The integrated MCBs have predictable timing and allow designers to quickly and easily design and implement DDR3-800 memory interfaces. Spartan-6 FPGAs with MCBs support access rates of up to 800 Mb/s compared to Cyclone IV GX DDR2 400 Mb/s soft controller capability. See the memory interface capability comparison in Figure 3.

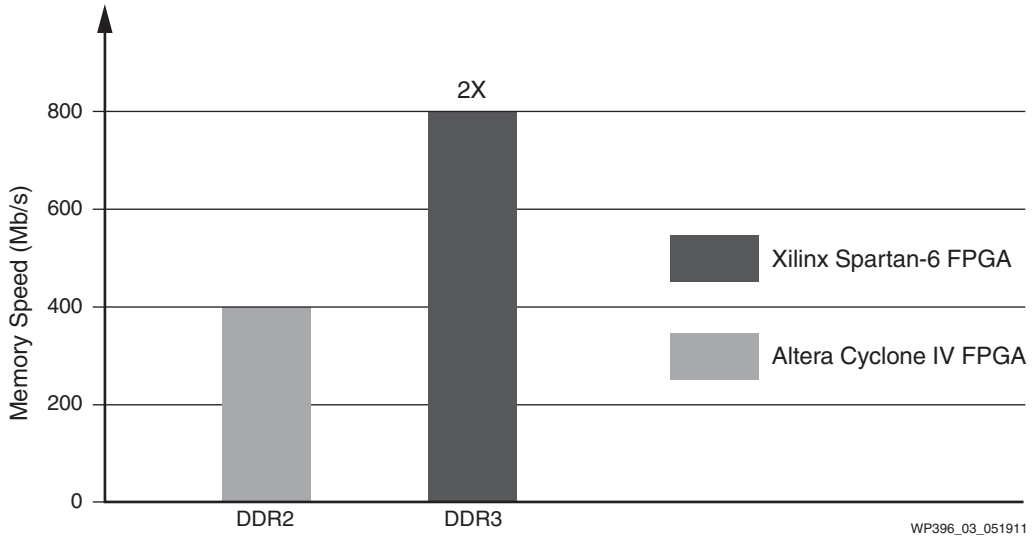

Figure 3: **DDR3 Memory Interface Speed Comparison**

Integrated Digital Signal Processing

To maximize performance while minimizing power consumption and silicon utilization, Spartan-6 devices support math-intensive applications with a high ratio of DSP48A1 slices to general-purpose logic. These DSP48A1 slices support many independent functions, including multiplier, multiplier-accumulator (MACC), pre-adder/subtracter followed by a multiply accumulator, multiplier followed by an adder, wide bus multiplexers, and wide counters. Multiple DSP48A1 slices can be connected together to implement wide math functions, DSP operations, filters, and complex arithmetic without wasting any general FPGA logic. Figure 4 shows an efficient DSP48A1 slice.

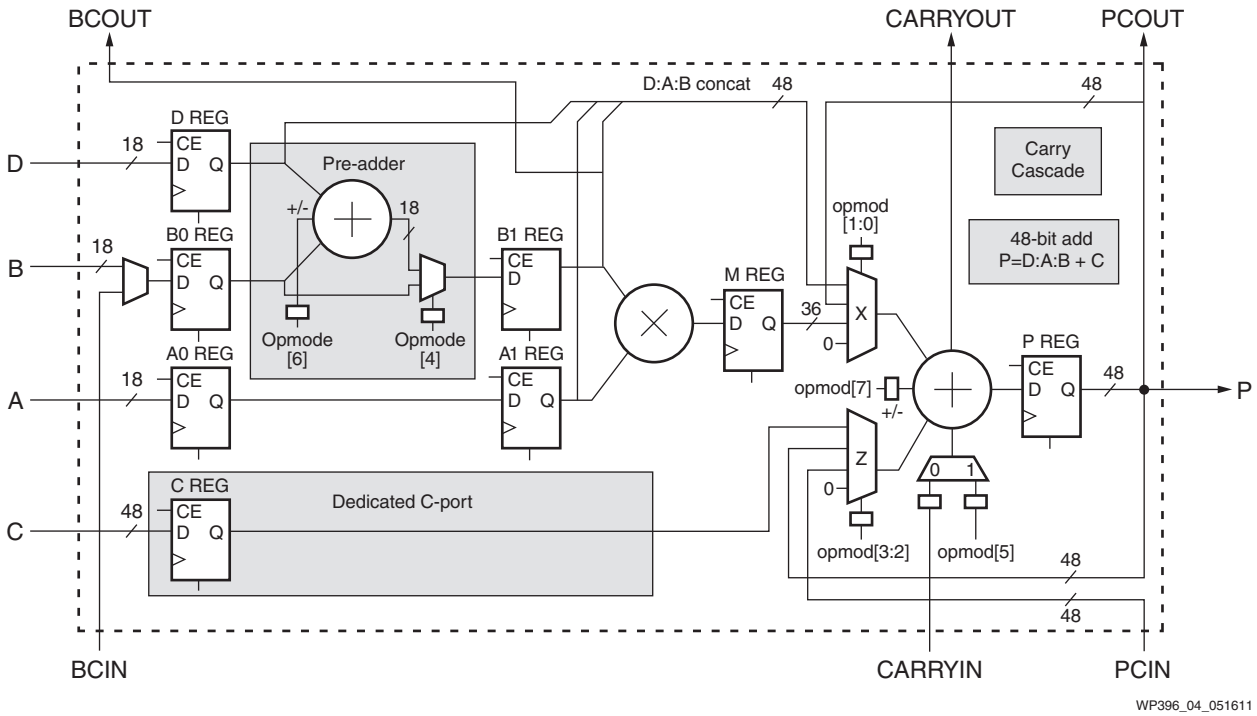

Figure 4: **Spartan-6 FPGA DSP48A1 Slice**

The enhanced DSP48A1 structure found in Spartan-6 devices includes the highly efficient pre-adder. The pre-adder provides many user benefits, including:

- Reduced power consumption by 50% compared to architectures without a pre-adder.
- Implementation with the smallest amount of logic while competing devices must perform the pre-adder function in the logic.
- A smaller footprint.
- Xilinx synthesis tools (XST) support, offering easy implementation.

Figure 5 shows an implementation of the symmetrical FIR filter in a leading alternative FPGA.

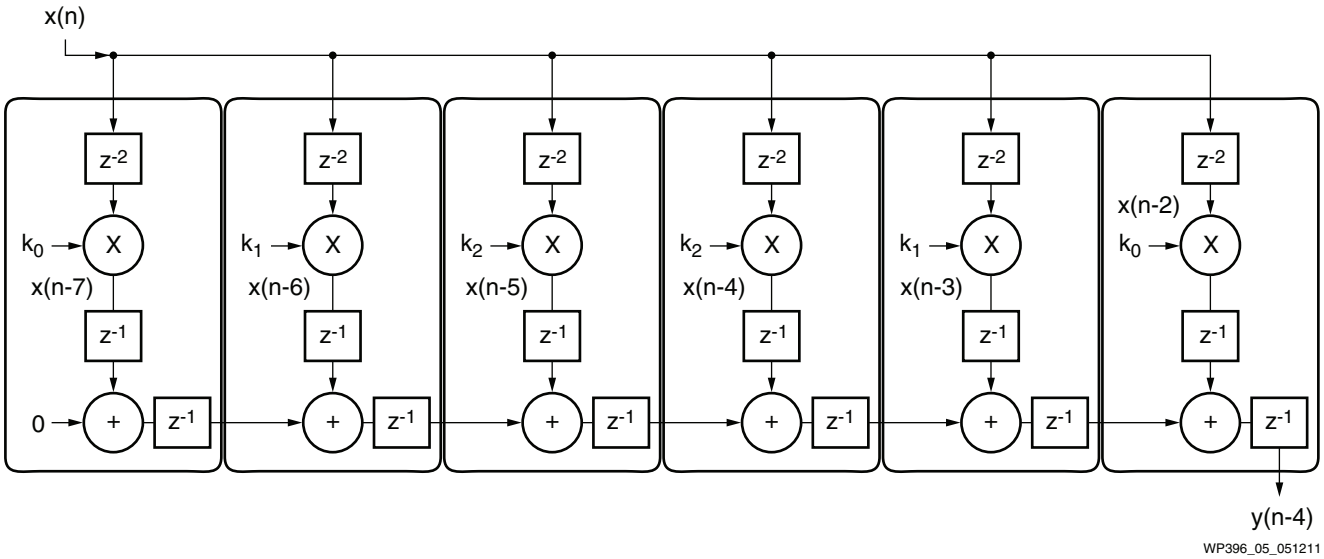

Figure 5: **Symmetrical FIR Filter in a Leading Alternative FPGA**

This same function in Spartan-6 devices requires much less logic and half the amount of DSP—and as much as 50% less power is consumed. See Figure 6. Ultimately, this enables a smaller device requirement and lower cost.

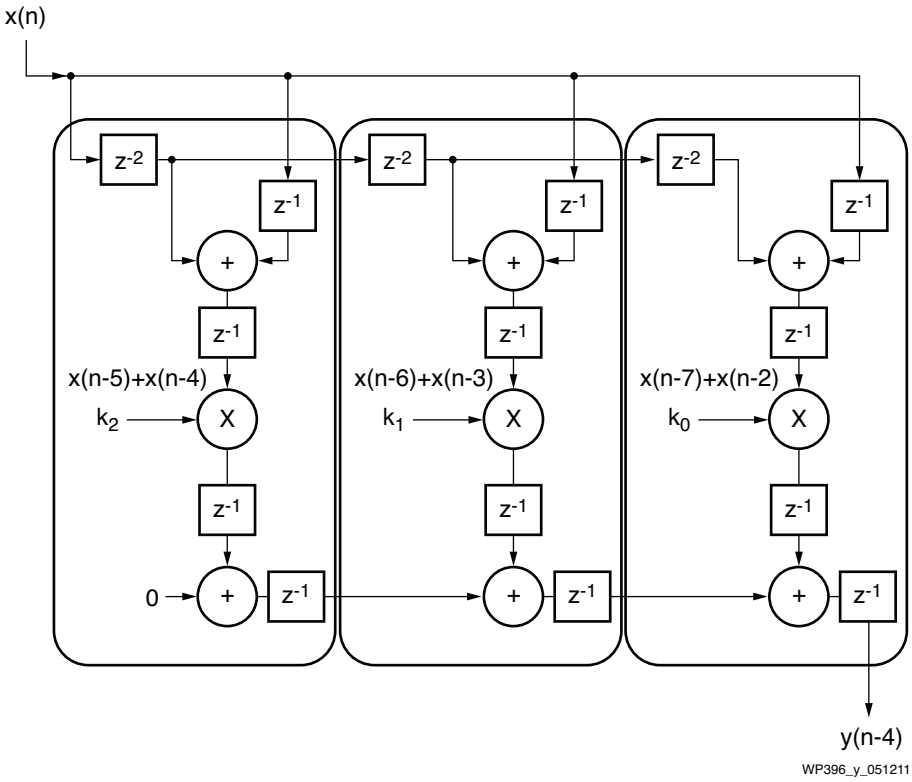

Figure 6: **Symmetrical FIR Filter in a Spartan-6 Device**

Integrated Endpoint Block for PCI Express

To streamline designs and lower development cost, the Spartan-6 FPGA includes the Integrated Endpoint Block for PCI Express® (Gen1) that interfaces seamlessly with the integrated Spartan-6 LXT FPGA serial I/O transceivers. Additionally, this integrated block is highly configurable to meet various design needs and has passed compliance testing performed at the PCI-SIG®. Spartan-6 FPGA hard block implementations not only save approximately 6,000 logic cells, allowing designs to fit into smaller Spartan-6 LXT FPGAs, but reduce cost, design complexity, and time to market due to the elimination of an external PHY chip.

High-Performance Clock Management

The digital clock managers (DCMs) and phase-locked loops (PLLs) in Spartan-6 FPGAs offer more flexibility than competing alternatives. The DCM adds finer phase shift capability than the PLLs available in Cyclone IV. Spartan-6 FPGAs offer up to six clock management tiles (CMTs), each consisting of two DCMs and one PLL, providing a rich clocking structure for internal and external clock distribution, maximizing system clock domain support.

Lowest Power with 45 nm Process Technology

Starting with the Spartan-3 FPGA family, 90 nm became the first process node where power (particularly from leakage) became a major focus. Using process, architectural, and software innovations, Xilinx has made major advances at the 45 nm process node in Spartan-6 FPGAs, reducing static, dynamic, and I/O power significantly over previous generations of FPGAs. The closest competitor is at 60 nm, which was a process shrink from an existing 65 nm set of devices. Comparing Spartan-6 FPGAs to Spartan-3A FPGAs, the average static power in the Spartan-6 devices is 50% lower and dynamic power is 40% lower. See Figure 7.

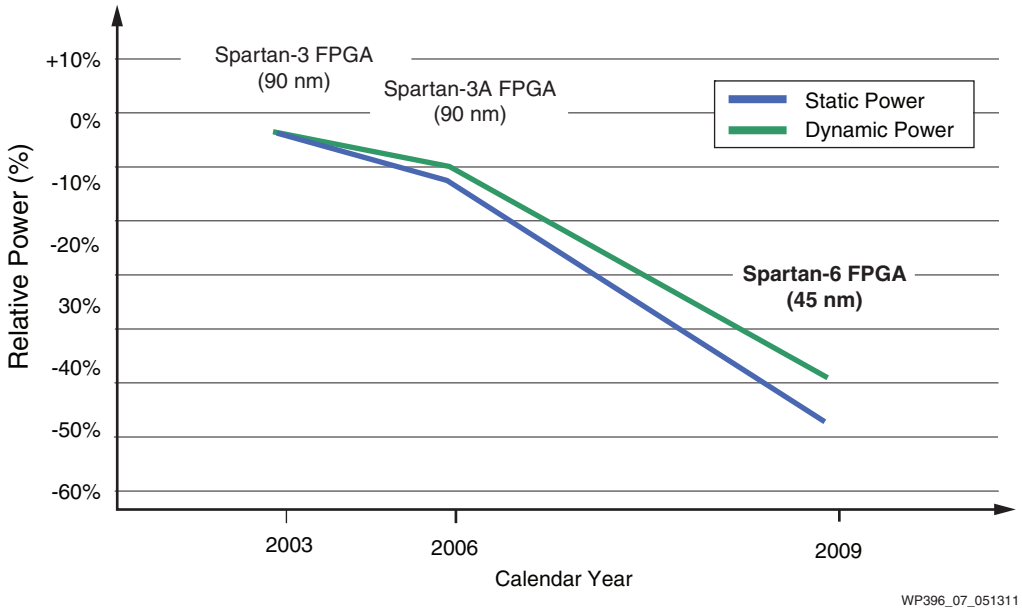

Figure 7: **Spartan FPGA Total Power Reduction over Time**

Process enhancements in Spartan-6 FPGAs include a transistor selection that balances power and performance, and capacitance reductions (geometry shrink and low-K dielectric).

Spartan-6 FPGAs achieve further power reductions through architectural enhancements like efficient 6-input LUTs, optimized feature mix, clock gating, various hard blocks like DSP, Integrated Endpoint Block for PCI Express, integrated memory controller, AES, programmable I/O slew rate and drive strength capability, system-level power management, and voltage scaling.

Innovative Power Management

Similar to Spartan-3 FPGAs, Spartan-6 FPGAs provide system-level power management features, such as suspend, hibernate, and clock gating. New to Spartan-6 FPGAs, designers now have much finer control with the introduction of the Multi-Pin Wake-Up technology. This feature gives designers the flexibility of using up to eight pins to control wake-up or exit from suspend mode, which maintains configuration and state. Suspend mode offers fast wake-up to respond to external system needs. On average, these features can reduce static power up to 30%—critical for highly power-sensitive applications, such as battery-powered and consumer applications, which can take advantage of dynamically controlled shutdown and wakeup.

Figure 8 shows the comparison of an equivalent Spartan-6 FPGA and Cyclone IV GX device. As illustrated, the example is a heavily utilized device with logic, DSP, and block RAM. In this example, the higher the frequency the greater the benefit, up to 25%, to the total power.

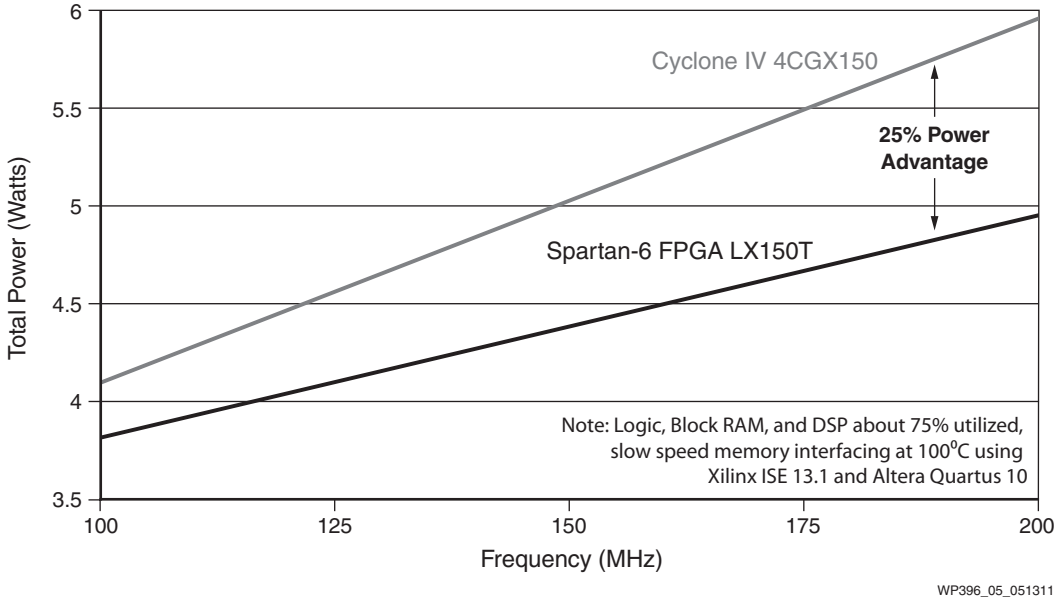

Figure 8: **Total Power Consumption Comparison**

Clock Gating and Voltage Scaling for Further Power Reduction

For additional power savings, designers can use Spartan-6 FPGA's fine-grain clock gating, which eliminates unnecessary clock activity while maintaining functionality and performance. With clock gating, local slice clock drivers or block RAM are dynamically turned off, or gated, when logic is not in use, enabling an excellent opportunity to further reduce dynamic power by up to 30%.

For designers of battery-operated systems who need the lowest possible power consumption, all Spartan-6 LX FPGAs offer the voltage-scaled -1L option, which lowers core voltage from 1.2V to 1.0V, reducing core power an additional 30–40%.

For additional Spartan-6 FPGA power management details, see WP298, *Power Consumption at 40 and 45 nm*.

Quick Design Differentiation with Targeted Design Platforms

The Targeted Design Platform strategy was developed by Xilinx to provide designers with simpler, smarter, and more strategically viable design platforms for the creation of world-class FPGA-based systems. Designers are provided a "kick-start," eliminating the need to develop all applications from the ground up, enabling a focus on innovation and product differentiation as soon as their development cycle begins.

These integrated platforms of hardware, software, IP, and targeted reference designs deliver productivity gains that greatly exceed the sum-of-the-parts of conventional evaluation boards and design examples. Xilinx and its partners offer a complete set of design kits. See Table 4.

Table 4: **Available Targeted Design Platforms**

Logic Evaluation Kits	**DSP Kits**
Atlys Spartan-6 FPGA Development Kit	Avnet Spartan-6 FPGA DSP Kit
Spartan-6 FPGA SP605 Evaluation Kit	Avnet TI OMAP/Spartan-6 FPGA co-processing Kit
Avnet Spartan-6/Intel Atom Development Kit	**Market-Specific Kits**
Avnet Spartan-6 LX150T Development Kit	Spartan-6 FPGA Broadcast Connectivity Kit
Spartan-6 FPGA SP601 Evaluation Kit	Spartan-6 FPGA Consumer Video Kit
Avnet Spartan-6 LX16 Evaluation Kit	Spartan-6 FPGA Industrial Ethernet Kit
Avnet Spartan-6 LX9 MicroBoard	Spartan-6 FPGA Industrial Video Processing Kit
Connectivity Kits	logiCRAFT6™ Development Board
Spartan-6 FPGA Connectivity Kit	logiCRAFT-CC™ Development Board
Embedded Kits	**Transceiver Characterization Kits**
Spartan-6 FPGA Embedded Kit	Spartan-6 FPGA SP623 Characterization Kit

No competing FPGA family offers this total solution combination, and Altera Cyclone IV currently offers a few development kits. For more details on Targeted Design Platforms, see WP306, *Introducing the Targeted Design Platform: Fulfilling the Programmable Imperative*.

Advanced Security

Extending low cost security leadership, Spartan-6 FPGAs provide proven Device DNA for cloning and overbuilding protection. Spartan-6 FPGAs also include hardened readback-disabling circuitry, internal configuration clearing (IPROG), and in the larger densities, advanced 256-bit AES support is available, previously only available in Virtex devices. For more information on Xilinx advanced FPGA security, see WP365, *Solving Today's Design Security Concerns*.

Conclusion

Xilinx understands the problems designers are trying to solve and has developed the low-cost, low-power Spartan-6 family, which resolves the performance gap found in alternative high-volume FPGA families. Table 5 lists the detailed competitive comparison between Spartan-6 FPGAs and Altera Cyclone IV GX FPGAs.

Table 5: **Spartan-6 FPGA versus Cyclone IV GX Capability Comparison**

Feature	Xilinx	Altera
	Spartan-6 FPGAs	Cyclone IV
Low-cost, low-power 45 nm Process	Yes	60 nm Process
Efficient 6-input LUT architecture	Yes	4-input LUT
3.2 Gb/s transceivers with dedicated PLL	Yes	3.125 Gb/s
1 Gb/s+ LVDS Capability	Yes	840 Mb/s
Integrated DDR3-800 memory controller	Yes	DDR2-400
Advanced power management	Yes	No
Integrated DSP Blocks	Yes	Multipliers only
Robust clock management	Yes	No
Advanced security	Yes	No
Targeted Design Platforms	Yes	No

Spartan-6 FPGA integrated blocks provide greater efficiency, superior ease-of-use, lower total power, lower cost, and unparalleled connectivity and memory capabilities. The superior I/O architecture and robust high-performance clocking in the 45 nm Spartan-6 FPGA family extends its low-cost, high-volume FPGA market leadership.

For specific Spartan-6 FPGA feature summaries by device, see DS160, *Spartan-6 Family Overview*. And for more Spartan-6 family application details, go to: http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/19/11	1.0	Initial Xilinx release.

Notice of Disclaimer