

Spartan-6 FPGA Packaging and Pinouts

Product Specification

UG385 (v2.3) May 12, 2014



NOTICE OF DISCLAIMER

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.

© Copyright 2009–2014 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/2009	1.0	Initial Xilinx release.
12/08/2009	1.1	<p>Revised User I/O and Differential Pair numbers in Table 1-4. Updated descriptions of SUSPEND, CMPCS_B_2, VFS, and RFUSE.</p> <p>Added data for the LX4 and LX75/LX75T devices and CPG196, FG(G)900, and CSG484 packages along with a complete revamping of Chapter 2, Pinout Tables and Chapter 3, Pinout and I/O Bank Diagrams including the LX45 in the FG(G)676 package.</p> <p>Added Figure 4-2, the mechanical drawing for the CPG196 package. Revised Figure 4-1, Figure 4-3, and Figure 4-5.</p> <p>Added values to Table 5-1, page 346.</p>
02/22/2010	1.2	<p>Added Table 1-5, page 17. In Table 1-6, updated the LDC, HDC, SCPn, V_{BATT}, VFS, and RFUSE descriptions. Added Spartan-6 FPGA Banks, GTP Transceiver Locations, Clock Inputs and BUFIO2 Clocking Regions, and Supply Voltages for I/O and Configuration Pins.</p> <p>Revised all the pinout tables in Chapter 2 to add the BUFIO2 clocking regions. Changed the CSG225 Package—LX4 discussion.</p> <p>Added a note to Figure 3-37 and updated Figure 3-65.</p> <p>Added MDDS and PCB design reference notes to Chapter 4.</p> <p>Added values to Table 5-1.</p> <p>Changed the package marking in Figure 6-1. Also updated descriptions in Table 6-1 for engineering samples and L1C.</p> <p>Added a new chapter: Chapter 7, Density Migration.</p>

Date	Version	Revision
10/12/2010	1.3	<p>In Table 1-6, revised description for IO_LXXY_ZZZ_#, Dn, VFS, RFUSE and added notes 1 and 2. Edited Clock Inputs and BUFIO2 Clocking Regions.</p> <p>In Table 2-3, revised the BUFIO2 regions for bank 3 pins D3, D4, E1, E2, F1, F2, F3, F4, H1, and H2. In Table 2-5, revised the BUFIO2 regions for bank 3 pins H1, K4, J3, G2, G1, K5, J4, F1, F3, J5, H4, G5, G3, H6, H5, F5, F4, E5, and E4.</p> <p>In Table 2-6, revised the BUFIO2 regions for bank 3 pins H13, H14, J11, J12, J13, K14, J6, H5, H4, H3, L4, and L5 to add separate information for the LX25 devices.</p> <p>In Table 2-7, revised the BUFIO2 regions for bank 1 pins C17, C18, F14, G14, D17, D18, H12, G13, E16, E18, K12, K13, F17, F18, H13, H14, H15, H16, G16, and G18, and to also add separate information for the LX25 device to bank 1 pins J13, K14, L12, L13, K15, and K16. Revised the BUFIO2 regions for bank 2 pins R15, T15, U16, V16, R13, T13, U15, V15, T14, V14, N12, P12, U13, V13, M11, N11, R11, T11, T12, V12, N10, P11, N9, U11, V11, R10, T10, U10, and V10. Revised the BUFIO2 regions for bank 3 pins N4, N3, P4, P3, L6, M5, U2, U1, T2, T1, P2, P1, N2, N1, M3, M1, L2, L1, K2, K1, L4, L3, J3, J1, H2, H1, K4, and K3, and to also add separate information for the LX25 device to bank 3 pins L5, K5, H4, H3, L7, and K6.</p> <p>In Table 2-8, revised the BUFIO2 regions for bank 1 pins C17, C18, F14, G14, D17, D18, H12, G13, E16, E18, K12, K13, F17, F18, H13, H14, H15, H16, G16, and G18, and to also add separate information for the LX25T device to bank 1 pins J13, K14, L12, L13, K15, and K16. Revised the BUFIO2 regions for bank 2 pins R15, T15, U16, V16, R13, T13, U15, V15, T14, V14, N12, P12, U13, V13, M11, N11, R11, T11, T12, V12, N10, P11, N9, U11, V11, R10, T10, U10, and V10. Revised the BUFIO2 regions for bank 3 pins N4, N3, P4, P3, L6, M5, U2, U1, T2, T1, P2, P1, N2, N1, M3, M1, L2, L1, K2, K1, L4, L3, J3, J1, H2, H1, K4, and K3, and to also add separate information for the LX25 device to bank 3 pins L5, K5, H4, H3, L7, and K6.</p> <p>In Table 2-9, revised the BUFIO2 regions to add separate information for the LX75 device to bank 0 pins E12, D12, F13, D13. Revised the BUFIO2 regions to add separate information for the LX25 device to bank 1 pins G20, G22, K20, K9, H21, H22. Revised the BUFIO2 regions to add separate information for the LX25 device to bank 3 pins K5, K4, K3, J4, K5, J6.</p> <p>In Table 2-10, revised the BUFIO2 regions to add separate information for the LX25T device to bank 0 pins J20, J22, M20, M19, K21, and K22.</p> <p>In Table 2-13, revised the BUFIO2 regions for bank 1 pins N25, N26, L19, K19, L23, L24, P20, N21, M23, N24, L17, K18, P24, P26, M19, L18, R25, R26, M18, N19, N22, N23, N17, N18, R23, R24, N20, M21, P21, and P22. Revised the BUFIO2 regions for bank 2 pins AD22, AF22, AE21, AF21, AD20, AF20, AE19, AF19, AC20, AD21, Y18, AA19, AC19, AD19, V16, W17, AD18, AF18, Y16, AA17, AA18, AB18, AE17, AF17, AD16, AF16, AE15, AF15, AB17, AC17, AC15, AD15, AC16, AD17, V15, W16, AB15, AC14, Y15, AA15, Y14, AA14, AD14, AF14, AE13, AF13. Revised the BUFIO2 regions for bank 3 pins AC7, AD7, AE3, AF2, AC4, AD4, AA7, Y6, AB7, AB6, AC5, AD5, AA5, AB5, W8, W7, AB4, AC3, AA4, AA3, W5, Y5, U8, U7, U5, V5, U4, U3, T8, T6, R5, T4, R7, R6, AB3, AB1, AD3, AD1, AC2, AC1, AE2, AE1, AA2, AA1, Y3, Y1, W2, W1, V3, V1, U2, U1, T3, T1, V4, and W3.</p> <p>In Table 5-1, added and updated values.</p> <p>Updated Chapter 6 to add more information about the various packages offered for Spartan-6 FPGAs.</p> <p>Added LX25 and LX25T Migration in Chapter 7.</p>
02/24/2011	2.0	<p>Revised the notation for the Ag content in Figure 4-4: FT(G)256 Fine-Pitch Thin BGA Package.</p> <p>Updated LX25 and LX25T Migration in Chapter 7.</p>

Date	Version	Revision
06/07/2011	2.1	Updated document descriptions in Additional Documentation . Added reference to <i>Spartan-6 FPGA PCB Design and Pin Planning Guide</i> in Introduction . Added reference to <i>Spartan-6 FPGA SelectIO Resources User Guide</i> to text preceding Table 1-4 . Added reference to <i>Spartan-6 FPGA SelectIO Resources User Guide</i> to Table 1-6 . Revised the tolerances for package type FG(G)676, symbol A in Figure 4-8 . Added reference to <i>Spartan-6 FPGA PCB Design and Pin Planning Guide</i> in Chapter 4, Summary . Added reference to <i>Spartan-6 FPGA PCB Design and Pin Planning Guide</i> in Chapter 7, Introduction .
08/24/2011	2.2	Updated the entire document to add the Defense-grade Spartan-6Q and XA Spartan-6 Automotive FPGAs. Added the CS484 package, where applicable, throughout the guide. Added Soldering Guidelines in Chapter 5 .
05/12/2014	2.3	Updated Figure 4-5: FG(G)484 Fine-Pitch BGA Package - Corner Gate Mold (CGM) and added Figure 4-6: FG(G)484 Fine-Pitch BGA Package - Pin Gate Mold (PGM) . Updated Figure 4-8: FG(G)676 Fine-Pitch BGA Package - Corner Gate Mold (CGM) and added Figure 4-9: FG(G)676 Fine-Pitch BGA Package - Pin Gate Mold (PGM) per XCN12023: Pin Gate Mold Implementation For FG(G) and BG(G) Wire Bond Packages . No change to form, fit, or function of the devices shipping. Added a note on page 346 above Table 5-1 and revised the θ_{JC} values for the CS(G)484 package. Updated NOTICE OF DISCLAIMER and About This Guide including links.

Table of Contents

Revision History	3
Preface: About This Guide	
Organization of This Guide	11
Additional Documentation	11
Additional Support Resources	12
Solution Centers	12
Chapter 1: Packaging Overview	
Summary	13
Introduction	13
Pb-free Packaging	14
Device/Package Combinations and Maximum I/Os	14
Pin Definitions	19
Spartan-6 FPGA Banks	23
Spartan-6 FPGA I/O Banks	23
Spartan-6 LXT FPGA GTP Transceiver Banks	23
Spartan-6 FPGA Bank Information	24
GTP Transceiver Locations	27
Clock Inputs and BUFIO2 Clocking Regions	27
Supply Voltages for I/O and Configuration Pins	28
Chapter 2: Pinout Tables	
Summary	29
TQG144 Package—LX4 and LX9	30
CPG196 Package—LX4, LX9, and LX16	35
CSG225 Package—LX4	42
CSG225 Package—LX9 and LX16	50
FT(G)256 Package—LX9, LX16, and LX25	58
CSG324 Package—LX9, LX16, LX25, and LX45	67
CSG324 Package—LX25T and LX45T	78
FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150	89
FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T	105
CS(G)484 Package—LX45, LX75, LX100, and LX150	121
CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T	137
FG(G)676 Package—LX45	153
FG(G)676 Package—LX75, LX100, and LX150	174
FG(G)676 Package—LX75T, LX100T, and LX150T	195
FG(G)900 Package—LX150	216

FG(G)900 Package—LX100T and LX150T	244
--	-----

Chapter 3: Pinout and I/O Bank Diagrams

Summary	273
TQG144 Package—LX4 and LX9	274
CPG196 Package—LX4, LX9, and LX16.....	276
CSG225 Package—LX4	277
CSG225 Package—LX9 and LX16	278
FT(G)256 Package—LX9, LX16, and LX25	279
CSG324 Package—LX9	280
CSG324 Package—LX16	281
CSG324 Package—LX25	282
CSG324 Package—LX25T.....	283
CSG324 Package—LX45	284
CSG324 Package—LX45T.....	285
FG(G)484 Package—LX25.....	286
FG(G)484 Package—LX25T	288
FG(G)484 Package—LX45.....	290
FG(G)484 Package—LX75.....	292
FG(G)484 Package—LX75T	294
FG(G)484 Package—LX100	296
FG(G)484 Package—LX150	298
FG(G)484 Package—LX45T, LX100T, and LX150T	300
CSG484 Package—LX45	302
CS(G)484 Package—LX75.....	304
CS(G)484 Package—LX100 and LX150.....	306
CS(G)484 Package—LX75T	308
CS(G)484 Package—LX45T, LX100T, and LX150T	310
FG(G)676 Package—LX45.....	312
FG(G)676 Package—LX75.....	314
FG(G)676 Package—LX75T	316
FG(G)676 Package—LX100	318
FG(G)676 Package—LX100T.....	320
FG(G)676 Package—LX150	322
FG(G)676 Package—LX150T.....	324
FG(G)900 Package—LX100T.....	326
FG(G)900 Package—LX150	328
FG(G)900 Package—LX150T.....	330

Chapter 4: Mechanical Drawings

Summary	333
TQG144 Thin Quad Flat-Pack Package Specifications (0.5 mm Pitch)	334
CPG196 Chip-Scale BGA Package Specifications (0.5 mm Pitch).....	335

CSG225 Chip-Scale BGA Package Specifications (0.8 mm Pitch)	336
FT(G)256 Fine-Pitch Thin BGA Package Specifications (1.00 mm Pitch)	337
CSG324 Chip-Scale BGA Package Specifications (0.8 mm Pitch)	338
FG(G)484 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)	339
CS(G)484 Chip-Scale BGA Package Specifications (0.8 mm Pitch)	341
FG(G)676 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)	342
FG(G)900 Chip-Scale BGA Package Specifications (1.00 mm Pitch)	344

Chapter 5: Thermal Specifications

Summary	345
Introduction	345
Package Strategy	348
Cavity-Up Plastic BGA Packages	348
Package Construction	348
Key Features/Advantages of Cavity-Up BGA Packages	348
Chip Scale Packages	348
Key Features/Advantages of CSP Packages	349
Support for Compact Thermal Models (CTM)	349
Soldering Guidelines	350
Sn/Pb Reflow Soldering	351
Notes for Figure 5-4 :	351
Pb-Free Reflow Soldering	351
References	354

Chapter 6: Package Marking

Chapter 7: Density Migration

Introduction	357
Compatibility	357
No Connects	358
Special Cases	360
MCBs and Parallel Configuration in the LX4	360
GTP Transceiver Connections in the LX25T	360
Encryption Pins	361
MCBs and I/O Banks in the FG(G)676 and FG(G)900	361
GTP Transceiver Banks	362
LX25 and LX25T Migration	362
Pin Names and Physical Pad Locations	362
Migrating Between Packages	362
PlanAhead Software Tool	363

About This Guide

This guide describes Spartan®-6 device pinouts and package specifications; it also includes pinout diagrams and thermal data.

Organization of This Guide

This document is comprised of the following chapters:

- [Chapter 1, Packaging Overview](#)
Provides an introduction to the Spartan-6 family with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- [Chapter 2, Pinout Tables](#)
Provides pinout information for all Spartan-6 devices and packages.
- [Chapter 3, Pinout and I/O Bank Diagrams](#)
Provides pinout diagrams for all Spartan-6 FPGA package/device combinations.
- [Chapter 4, Mechanical Drawings](#)
Provides mechanical drawings of Spartan-6 FPGA packages.
- [Chapter 5, Thermal Specifications](#)
Provides thermal data associated with Spartan-6 FPGA packages. Discusses Spartan-6 FPGA power management strategy and thermal management options.
- [Chapter 6, Package Marking](#)
Provides example and description of the marking on top of the package (topmark).
- [Chapter 7, Density Migration](#)
The guidelines in this chapter facilitate migration of designs between different Spartan-6 device/package combinations.

Additional Documentation

A complete suite of documentation is available for the commercial (XC) Spartan-6 FPGAs at: www.xilinx.com/support/documentation/spartan-6.htm.

Additional specific documentation for the Defense-grade Spartan-6Q FPGAs (XQ) is available at: www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/spartan-6q.html.

Additional specific documentation for the XA Spartan-6 Automotive FPGAs is available at: www.xilinx.com/support/documentation/automotive_xa_devices.htm.

Additional Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support: www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary: www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers: www.xilinx.com/support/solcenters.htm for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Packaging Overview

Summary

This chapter covers the following topics:

- [Introduction](#)
- [Pb-free Packaging](#)
- [Device/Package Combinations and Maximum I/Os](#)
- [Pin Definitions](#)
- [Spartan-6 FPGA Banks](#)
- [Clock Inputs and BUFIO2 Clocking Regions](#)
- [Supply Voltages for I/O and Configuration Pins](#)

Introduction

This section describes the pinouts for Spartan®-6 devices in various packages.

Spartan-6 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os. Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All of the Spartan-6 LX devices supported in a particular package are pinout compatible. All of the Spartan-6 LXT devices supported in a particular package are pinout compatible. The Spartan-6 LX devices are not pin compatible with the Spartan-6 LXT devices. Pins that are not available in some of the devices are listed in the “No Connects” column of each table.

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*). Global pins and power/ground pins, are listed at the end of each table. [Table 1-6](#) provides definitions for all pin types.

See [UG393](#), *Spartan-6 FPGA PCB Design and Pin Planning Guide* for recommendations for board layout, PCB design rules, and pin planning.

Pb-free Packaging

Xilinx offers lead-free devices (Pb-free) that comply with the European Union's RoHS directive (2002/95/EC). Information on the material composition of our Pb-free, RoHS compliant FPGAs is available as either material declaration data sheets or IPC 1752 forms, at <http://www.xilinx.com/support/documentation/spartan-6.htm#131532>. For more information on Pb-free packaging, see www.xilinx.com/pbfree.

The Pb-free packages include an extra G in the package code. For example, FTG256 is the Pb-free version of the FT256 package. When referenced together, the G is incorporated as FT(G)256. The Pb and Pb-free packages are identical in pin-out, size, and thermal characteristics.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the package specifications and the maximum number of user I/Os possible in Spartan-6 FPGA packages. Specific information on device/package combinations by family is available at:

- [DS160](#): *Spartan-6 Family Overview*
- [DS170](#): *XA Spartan-6 Automotive Family Overview*
- [DS172](#): *Defense-grade Spartan-6Q Family Overview*

Table 1-1: Spartan-6 FPGA Packages

	Packages								
	TQG144 ⁽¹⁾	CPG196	CSG225	FT(G)256 ⁽²⁾	CSG324	FG(G)484 ⁽²⁾	CS(G)484 ⁽²⁾	FG(G)676 ⁽²⁾	FG(G)900 ⁽²⁾
Package Type	Quad Flat Pack	Chip Scale	Chip Scale	BGA	Chip Scale	BGA	Chip Scale	BGA	BGA
Pitch (mm)	0.5	0.5	0.8	1.00	0.8	1.00	0.8	1.00	1.00
Size (mm)	22 x 22 ⁽¹⁾	8 x 8	13 x 13	17 x 17	15 x 15	23 x 23	19 x 19	27 x 27	31 x 31
Maximum I/Os	102	106	160	186	232	338	338	498	576

Notes:

1. The footprint for the TQG144 package (22 x 22 mm) is larger than the package body (20 x 20 mm).
2. These devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See the specific family overview for more information on packages offered by density.

The number of I/Os per package includes all user I/Os *except* the dedicated pins listed in [Table 1-2](#) and the GTP serial transceiver I/O channels for the devices listed in [Table 1-3](#).

Table 1-2: Spartan-6 FPGA Dedicated Configuration Pins

SUSPEND	PROGRAM_B_2	TDI	TMS	VFS ⁽¹⁾	VBATT ⁽¹⁾
DONE_2	CMPCS_B_2	TDO	TCK	RFUSE ⁽¹⁾	

Notes:

1. Only available in LX75, LX75T, LX100, LX100T, LX150, and LX150T devices.

Table 1-3: Number of Serial Transceivers (GTs) I/O Channels/Device

I/O Channels	Device				
	LX25T	LX45T	LX75T ⁽¹⁾	LX100T ⁽²⁾	LX150T ⁽²⁾
MGTRXP	2	4	4 or 8	4 or 8	4 or 8
MGTRXN	2	4	4 or 8	4 or 8	4 or 8
MGTTXP	2	4	4 or 8	4 or 8	4 or 8
MGTTXN	2	4	4 or 8	4 or 8	4 or 8

Notes:

1. The LX75T has 4 GTP I/O channels in the FG(G)484 and CS(G)484 packages and 8 GTP I/O channels in the FG(G)676 package.
2. The LX100T and the LX150T have 4 GTP I/O channels in the FG(G)484 and CS(G)484 packages and 8 GTP I/O channels in the FG(G)676 and FG(G)900 packages.

Table 1-4 shows the number of available I/Os and the number of differential pairs for each Spartan-6 FPGA device/package combination. Not all I/O standards can be used on all pins. For example, for many differential standards, the outputs are only available in banks 0 and 2. For information on banking rules, see [UG381, Spartan-6 FPGA SelectIO Resources User Guide](#).

Table 1-4: Available I/O Pin/Device/Package Combinations

Spartan-6 Device	User I/O Pins	Spartan-6 FPGA Package								
		TQG144	CPG196	CSG225	FT(G)256	CSG324	FG(G)484	CS(G)484	FG(G)676	FG(G)900
LX4	Available User I/Os	102	106	132	–	–	–	–	–	–
	Differential Pairs	51	53	66	–	–	–	–	–	–
LX9	Available User I/Os	102	106	160	186	200	–	–	–	–
	Differential Pairs	51	53	80	93	100	–	–	–	–
LX16	Available User I/Os	–	106	160	186	232	–	–	–	–
	Differential Pairs	–	53	80	93	116	–	–	–	–
LX25	Available User I/Os	–	–	–	186	226	266	–	–	–
	Differential Pairs	–	–	–	93	113	133	–	–	–
LX45	Available User I/Os	–	–	–	–	218	316	320	358	–
	Differential Pairs	–	–	–	–	109	158	160	179	–
LX75	Available User I/Os	–	–	–	–	–	280	328	408	–
	Differential Pairs	–	–	–	–	–	140	164	204	–
LX100	Available User I/Os	–	–	–	–	–	326	338	480	–
	Differential Pairs	–	–	–	–	–	163	169	240	–
LX150	Available User I/Os	–	–	–	–	–	338	338	498	576
	Differential Pairs	–	–	–	–	–	169	169	249	288
LX25T	Available User I/Os	–	–	–	–	190	250	–	–	–
	Differential Pairs	–	–	–	–	95	125	–	–	–
LX45T	Available User I/Os	–	–	–	–	190	296	296	–	–
	Differential Pairs	–	–	–	–	95	148	148	–	–
LX75T	Available User I/Os	–	–	–	–	–	268	292	348	–
	Differential Pairs	–	–	–	–	–	134	146	174	–
LX100T	Available User I/Os	–	–	–	–	–	296	296	376	498
	Differential Pairs	–	–	–	–	–	148	148	188	249
LX150T	Available User I/Os	–	–	–	–	–	296	296	396	540
	Differential Pairs	–	–	–	–	–	148	148	198	270

Table 1-5 shows the number of I/O available per bank for each Spartan-6 FPGA device/package combination. Bank diagram are shown in Chapter 3. For information on banking rules, see UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 1-5: Number of I/Os per Bank for Each Device/Package Combination

Package	Device	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Total I/O
TQG144	LX4	26	24	26	26	N/A	N/A	102
	LX9	26	24	26	26	N/A	N/A	102
CPG196	LX4	26	26	28	26	N/A	N/A	106
	LX9	26	26	28	26	N/A	N/A	106
	LX16	26	26	28	26	N/A	N/A	106
CSG225	LX4	34	32	34	32	N/A	N/A	132
	LX9	40	40	38	42	N/A	N/A	160
	LX16	40	40	38	42	N/A	N/A	160
FT(G)256	LX9	40	54	38	54	N/A	N/A	186
	LX16	40	54	38	54	N/A	N/A	186
	LX25	40	54	38	54	N/A	N/A	186
CSG324	LX9	44	56	44	56	N/A	N/A	200
	LX16	60	56	60	56	N/A	N/A	232
	LX25	54	56	60	56	N/A	N/A	226
	LX45	46	56	60	56	N/A	N/A	218
	LX25T	18	56	60	56	N/A	N/A	190
	LX45T	18	56	60	56	N/A	N/A	190
CS(G)484	LX45	46	112	58	104	N/A	N/A	320
	LX75	56	112	52	108	N/A	N/A	328
	LX100	56	112	62	108	N/A	N/A	338
	LX150	56	112	62	108	N/A	N/A	338
	LX45T	40	98	52	106	N/A	N/A	296
	LX75T	40	98	48	106	N/A	N/A	292
	LX100T	40	98	52	106	N/A	N/A	296
	LX150T	40	98	52	106	N/A	N/A	296

Table 1-5: Number of I/Os per Bank for Each Device/Package Combination (Cont'd)

Package	Device	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Total I/O
FG(G)484	LX25	58	64	80	64	N/A	N/A	266
	LX45	46	82	100	88	N/A	N/A	316
	LX75	56	82	54	88	N/A	N/A	280
	LX100	68	82	88	88	N/A	N/A	326
	LX150	68	82	100	88	N/A	N/A	338
	LX25T	46	64	76	64	N/A	N/A	250
	LX45T	46	82	82	86	N/A	N/A	296
	LX75T	46	82	54	86	N/A	N/A	268
	LX100T	46	82	82	86	N/A	N/A	296
	LX150T	46	82	82	86	N/A	N/A	296
FG(G)676	LX45	46	112	88	112	N/A	N/A	358
	LX75	56	92	56	98	52	54	408
	LX100	92	92	92	98	52	54	480
	LX150	110	92	92	98	52	54	498
	LX75T	56	62	56	68	52	54	348
	LX100T	70	62	70	68	52	54	376
	LX150T	80	62	80	68	52	54	396
FG(G)900	LX150	132	94	130	114	52	54	576
	LX100T	92	94	92	114	52	54	498
	LX150T	114	94	112	114	52	54	540

Pin Definitions

Table 1-6 lists the pin definitions used in Spartan-6 FPGA packages. Further details on pin functionality is available in the device user guides:

<http://www.xilinx.com/support/documentation/spartan-6.htm>.

Table 1-6: Spartan-6 FPGA Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/ Output	All user I/O pins are capable of differential signaling and can implement pairs ⁽¹⁾ . Each user I/O is labeled IO_LXXY_#, where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = [P N] for the positive/negative sides of the differential pair. # indicates the bank number.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled IO_LXXY_ZZZ_#, where ZZZ represents one or more of the following functions in addition to being general purpose user I/O. When not used for their special function, these pins can be user I/O.
Dn	Input/ Output (during readback)	In SelectMAP/BPI modes, D0 through D15 are configuration data pins. During slave SelectMAP readback, the pins become outputs when RDWR_B = 1. These pins become user I/Os after configuration, unless the SelectMAP port is retained.
D0_DIN_MISO_MISO1	Input	In Parallel (SelectMAP and BPI) modes, D0 is the LSB of the data bus. In Bit-serial modes, DIN is the single-data input. In SPI mode, MISO is the Master Input/Slave Output. In SPI x2 or x4 modes, MISO1 is the second bit of the SPI bus.
D1_MISO2, D2_MISO3	Input	In Parallel modes, D1 and D2 are lower-order bits of the data bus. In SPI x4 mode, MISO2 and MISO3 are two MSBs of the SPI bus.
An	Output	Address A0–A25 BPI address output. These pins become user I/O after configuration.
AWAKE	Output	Status output pin for the power-saving Suspend mode. SUSPEND is a dedicated pin and AWAKE is a multi-function pin. Unless Suspend mode is enabled in the application, AWAKE is available as user I/O.
MOSI_CSI_B_MISO0	Input/ Output	In SPI modes, Master Output/Slave Input (MOSI) connects from the FPGA to the SPI flash slave data input to send read commands and starting addresses. In SelectMAP mode, CSI_B is the active-low chip-select signal. In SPI x2 or x4 modes, MISO0 is the first bit of the SPI bus.
FCS_B	Output	BPI flash chip select.
FOE_B	Output	BPI flash output enable.
FWE_B	Output	BPI flash write enable.
LDC	Output	Low during configuration in BPI mode.

Table 1-6: Spartan-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
HDC	Output	High during configuration in BPI mode.
CSO_B	Output	In Parallel modes, parallel daisy-chain chip select. In SPI mode, SPI flash chip select.
IRDY1/2, TRDY1/2	Output	Used with LogiCORE IP for PCI designs. An instantiation of the Xilinx core requires the use of either IRDY1 and TRDY1 or IRDY2 and TRDY2. See the core documentation for more details. These pins are available as user I/O when not being used for PCI designs.
DOUT_BUSY	Output	In SelectMAP mode, BUSY indicates the device status. In Bit-serial modes, DOUT gives configuration data to down-stream devices in a daisy chain.
RDWR_B_VREF	Input	In SelectMAP mode, this is the active-low write-enable signal. After configuration and if needed, RDWR_B can become a V_{REF} in bank 2.
HSWAPEN	Input	When Low, enables I/O pullups before and during configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. Can be used after configuration (optional) to indicate POST_CRC status.
SCPn	Input	Suspend control pins SCP0-SCP7. Used for SUSPEND multi-pin wake-up feature.
CMPMOSI, CMPMISO, CMPCLK	N/A	Reserved for future use. Use these pins as general-purpose I/O.
M0, M1	Input	Configuration mode selection. M0 = Parallel (Low) or Serial (High). M1 = Master (Low) or Slave (High).
CCLK	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
USERCCLK	Input	Optional user configuration clock input in Master modes.
GCLK	Input	These clock pins connect to global clock buffers. These pins become regular user I/Os when not needed for clocks.
VREF_#	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank). When used as a reference voltage within a bank, all V_{REF} pins within that bank must be connected.
Multi-Function Memory Controller Pins⁽²⁾		
M#DQn	Input/ Output	Memory controller data D[0:15] in bank #.
M#LDQS	Input/ Output	Memory controller lower data strobe in bank #.
M#LDQSN	Input/ Output	Memory controller lower data strobe N in bank #.

Table 1-6: Spartan-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
M#UDQS	Input/ Output	Memory controller upper data strobe in bank #.
M#UDQSN	Input/ Output	Memory controller upper data strobe N in bank #.
M#An	Output	Memory controller address A[0:14] in bank #.
M#BA _n	Output	Memory controller bank address BA[0:2] in bank #.
M#LDM	Output	Memory controller lower data mask in bank #.
M#UDM	Output	Memory controller upper data mask in bank #.
M#CLK	Output	Memory controller clock in bank #.
M#CLK _N	Output	Memory controller active-Low clock in bank #.
M#CAS _N	Output	Memory controller active-Low column address strobe in bank #.
M#RAS _N	Output	Memory controller active-Low row address strobe in bank #.
M#ODT	Output	Memory controller on-die termination control for external memory in bank #.
M#WE	Output	Memory controller write enable in bank #.
M#CKE	Output	Memory controller clock enable in bank #.
M#RESET	Output	Memory controller reset in bank #.
Dedicated Pins⁽³⁾		
DONE ₂	Input/ Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
PROGRAM _{B_2}	Input	Active-Low asynchronous reset to configuration logic. This pin has a default weak pull-up resistor.
SUSPEND	Input	Active-High control input pin for the power-saving Suspend mode. SUSPEND is a dedicated pin and AWAKE is a multi-function pin. Must be enabled by configuration option. When Suspend mode is not used, connect this pin to GND.
TCK	Input	JTAG Boundary-scan clock.
TDI	Input	JTAG Boundary-scan data input.
TDO	Output	JTAG Boundary-scan data output.
TMS	Input	JTAG Boundary-scan mode select.

Table 1-6: Spartan-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
Reserved Pins		
NC	N/A	When found in a table or text file, an NC indicates that this pin is not connected in the specific device/package combination. However, in some devices in the same package, another pin name is used to describe this pin.
CMPCS_B_2	Input	Reserved. Leave unconnected or connect High (V_{CCO_2}).
Other Pins		
GND	N/A	Ground.
VBATT	N/A	Decryptor key RAM memory backup supply. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. If key RAM is not used, connecting V_{BATT} to V_{CCAUX} or GND is recommended, or the pin can be left unconnected. Only available in the LX75, LX75T, LX100, LX100T, LX150, and LX150T devices.
VCCAUX	N/A	Power-supply pins for auxiliary circuits.
VCCINT	N/A	Power-supply pins for the internal core logic.
VCCO_#	N/A	Power-supply pins for the output drivers (per bank).
VFS	Input	Decryptor key EFUSE power supply pin for programming. When not programming, tie this pin to a voltage between GND and 3.45V. When not using the key EFUSE, the recommendation is to connect VFS to V_{CCAUX} or GND, however, the pin can be left unconnected. Only available in the LX75, LX75T, LX100, LX100T, LX150, and LX150T devices.
RFUSE	Input	Decryptor key EFUSE resistor to GND for programming. When not programming or when not using the key EFUSE, connecting RFUSE to V_{CCAUX} or GND is recommended, however, the pin can be left unconnected. Only available in the LX75, LX75T, LX100, LX100T, LX150, and LX150T devices.

Table 1-6: Spartan-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
GTP Transceiver Pins (GTPA1_DUAL Primitive)⁽⁴⁾		
MGTAVCC	N/A	Power-supply pin for transceiver mixed-signal circuitry.
MGTAVTTTX, MGTAVTTRX	N/A	Power-supply pin for TX and RX circuitry.
MGTAVTTRCAL	N/A	Power-supply pin for the resistor calibration circuit.
MGTAVCCPLL0 MGTAVCCPLL1	N/A	Power-supply pin for PLL.
MGTREFCLK0/1P	Input	Positive differential reference clock.
MGTREFCLK0/1N	Input	Negative differential reference clock.
MGTRREF	Input	Precision reference resistor pin for internal calibration termination.
MGTRXP[0:1]	Input	Positive differential receive port.
MGTRXN[0:1]	Input	Negative differential receive port.
MGTTXP[0:1]	Output	Positive differential transmit port.
MGTTXN[0:1]	Output	Negative differential transmit port.

Notes:

1. See banking rules in [UG381: Spartan-6 FPGA SelectIO Resources User Guide](#).
2. For further information, see [UG388: Spartan-6 FPGA Memory Controller User Guide](#).
3. Dedicated pins without a bank number (JTAG and SUSPEND) are powered by V_{CCAUX}.
4. For further information, see [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Spartan-6 FPGA Banks

Bank designations at the end of each pin name indicate the bank number for that pin. There are both I/O banks and GTP transceiver banks in the Spartan-6 family.

Spartan-6 FPGA I/O Banks

Each Spartan-6 device contains either four or six I/O banks depending on device size and package. Each bank varies in the number of available and bonded I/O, with as few as 18 and as many as 114 I/O available in one bank.

- LX45/LX45T and smaller and all devices in the CS(G)484 and FG(G)484 packages have four I/O banks, one on each side of the device.
- LX75/LX75T and larger in the FG(G)676 and FG(G)900 packages have two I/O banks on the left and right sides for a total of six I/O banks.

Spartan-6 LXT FPGA GTP Transceiver Banks

There are from one to four GTPA1_DUAL tiles in each Spartan-6 LXT device. Each GTPA1_DUAL tile has its own power supplies and bank designation. GTP transceiver banks 101 and 123 are embedded in I/O bank 0, and GTP transceiver banks 245 and 267 are embedded in I/O bank 2.

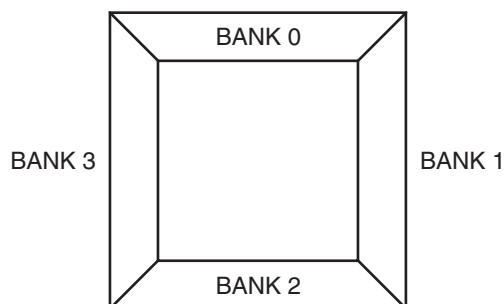
Spartan-6 FPGA Bank Information

Table 1-7 shows the bank names and locations. Not all banks are available in every device/package combination.

Table 1-7: Spartan-6 FPGA Bank Numbering

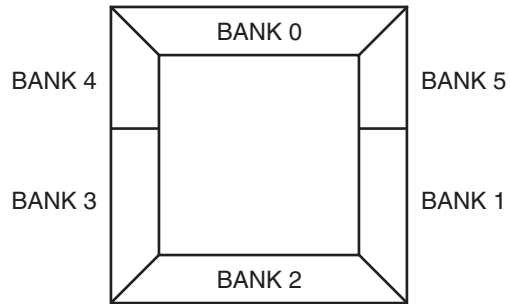
Bank	Locations	Description
0	Top	All devices
1	Right	All devices
2	Bottom	All devices; contains most configuration pins
3	Left	All devices
4	Left, Top	Extra bank in LX75/LX75T, LX100/LX100T, LX150/LX150T in FG(G)676 and FG(G)900 packages
5	Right, Top	Extra bank in LX75/LX75T, LX100/LX100T, LX150/LX150T in FG(G)676 and FG(G)900 packages
101	Top, Left	GTP transceiver bank in all LXT devices
123	Top, Right	GTP transceiver bank in LX45T, LX75T, LX100T, LX150T
245	Bottom, Left	GTP transceiver bank in LX75T, LX100T, LX150T in FG(G)676 and FG(G)900 packages
267	Bottom, Right	GTP transceiver bank in LX75T, LX100T, LX150T in FG(G)676 and FG(G)900 packages

Figure 1-1 through Figure 1-5 visually describe a device view of the FPGA bank numbering.



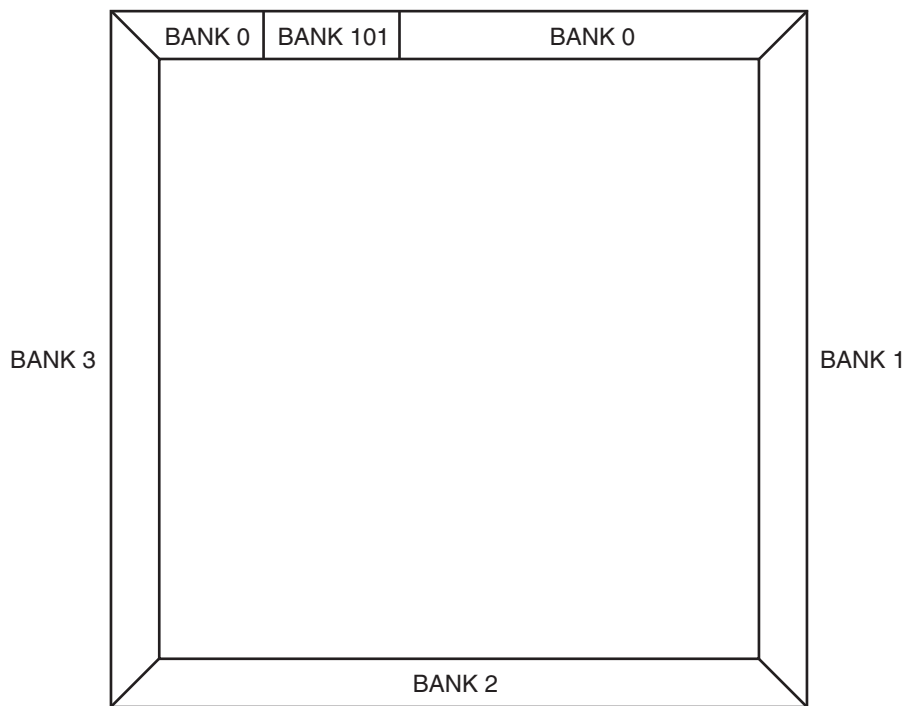
UG385_c1_01_012810

Figure 1-1: I/O Banks for All LX4, LX9, LX16, LX25, and LX45 Devices and for the LX75, LX100 and LX150 Devices in the CS(G)484 and FG(G)484 Packages



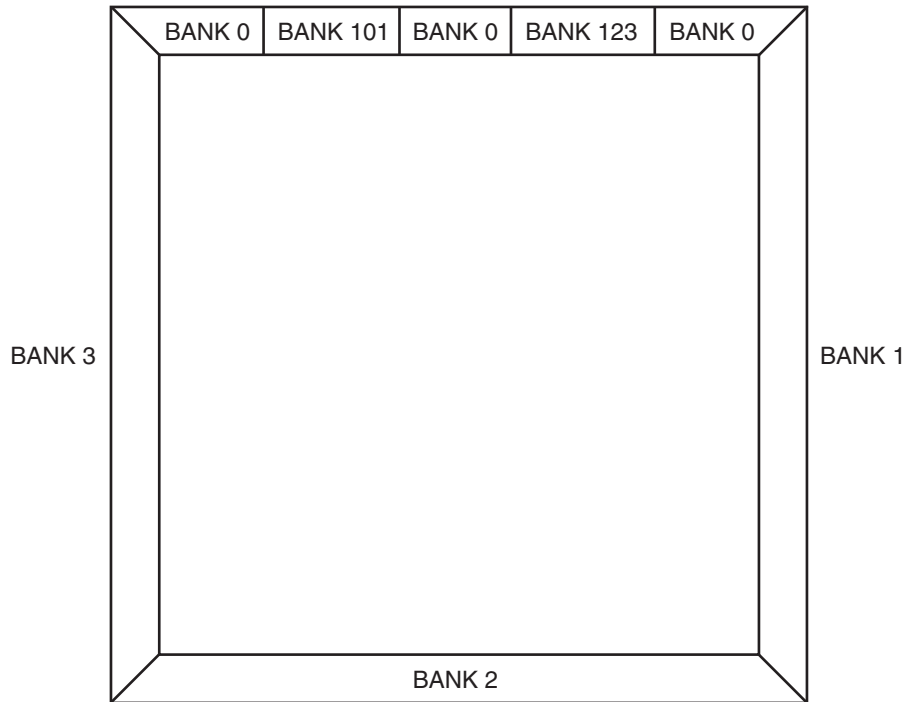
UG385_c1_02_020910

Figure 1-2: I/O Banks for LX75, LX100, and LX150 Devices in the FG(G)676 and FG(G)900 Packages



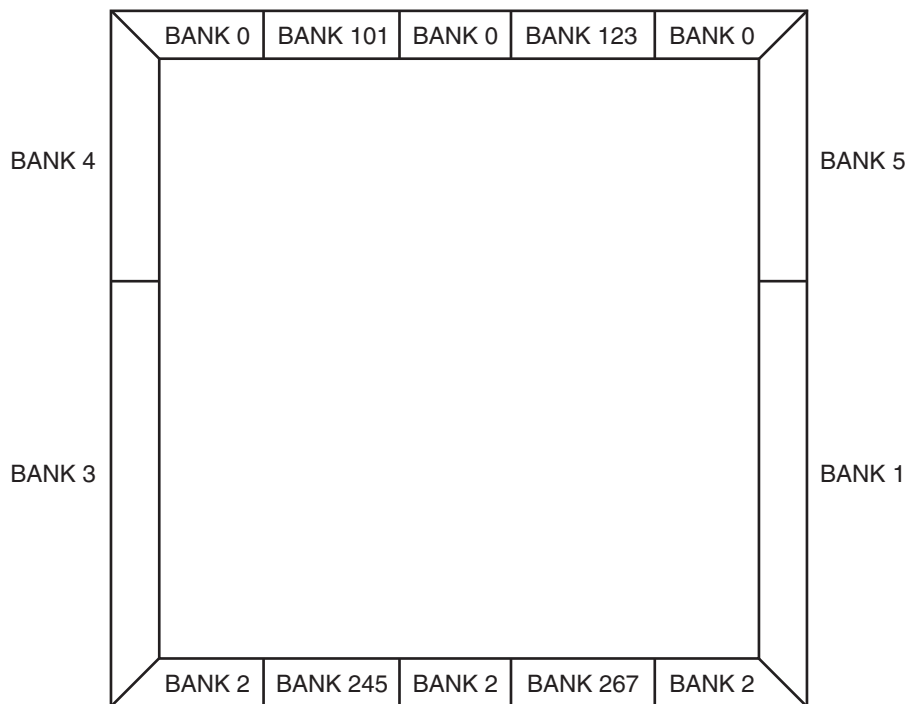
UG385_c1_03_012810

Figure 1-3: I/O and GTP Banks for All LX25T Devices



UG385_c1_04_012810

Figure 1-4: I/O and GTP Banks for LX45T, LX75T, LX100T, and LX150T Devices in the CSG324, FG(G)484, and CS(G)484 Packages



UG385_c1_05_020910

Figure 1-5: I/O and GTP Banks for LX75T, LX100T, and LX150T Devices in the FG(G)676 and FG(G)900 Packages

GTP Transceiver Locations

The position of GTPA1_DUAL tiles is specified by an XY coordinate system (where X = column, Y = row) for location constraints. The Spartan-6 LX25T and LX45T devices have all the GTP transceivers located in a row along the top of the device. For these devices with only a top row, the value of the Y coordinate is always 0. The LX75T, LX100T, and LX150T devices have one GTP transceiver row at the top and one GTP transceiver row at the bottom of the device. For these devices, the value of the Y coordinate of the bottom row is 0, and for the top row is 1. [Table 1-8](#) shows the association between GTP transceiver locations and GTP transceiver I/O banks. See [UG386](#), *Spartan-6 FPGA GTP Transceivers User Guide* for more information.

Table 1-8: GTP Transceiver Bank to GTP Transceiver Location

Devices	GTP Transceiver Bank Number	GTP Transceiver Location
LX25T, LX45T	101	X0Y0
LX75T, LX100T, LX150T		X0Y1
LX45T	123	X1Y0
LX75T, LX100T, LX150T		X1Y1
LX75T, LX100T, LX150T	245	X0Y0
LX75T, LX100T, LX150T	267	X1Y0

Clock Inputs and BUFIO2 Clocking Regions

Banks 0, 1, 2, and 3 each contain eight GCLK input pins, providing a total of 32 dual-purpose pins for use as clock inputs. The CPG196 package connects only four of the eight clock inputs in bank 2.

Global clock (GCLK) input pins can connect directly to the global clock buffers (BUFGs), to the BUFIO2 and then to local I/O clocking, or to the BUFIO2 and then to DCMs and PLLs. Each Spartan-6 device has 16 BUFGs. Each BUFG can be driven by one of two GCLK pins. When driving a global clock buffer directly with a global clock input, the global clock inputs from banks 0 and 1 share the same eight BUFGs. Similarly, banks 2 and 3 share eight BUFGs.

There are four high-speed I/O clocks in every half-edge of the device, driven by four dedicated BUFIO2 buffers. Each side of the device has two separated I/O clock regions. These BUFIO2 clocking regions are noted in the pinout tables in [Chapter 2](#). For example, TL indicates that the I/O is driven by the BUFIO2 clocking region in the left half of the top edge (bank 0) of the device. It is possible to span an entire bank with a single I/O clock input that is connected to the BUFIO2 buffers on both sides.

For further details on global and I/O clocks, see [UG382](#), *Spartan-6 FPGA Clocking Resources User Guide*.

Supply Voltages for I/O and Configuration Pins

Output buffers within a given I/O bank (banks 0 through 5) must share the same output drive source voltage, V_{CCO} .

The dedicated DONE and PROGRAM_B configuration pins are in bank 2. The other dedicated configuration pins are powered by V_{CCAUX} . Dual-purpose configuration pins are powered by the V_{CCO} of the bank in which they are located. For more details on configuration pins, see [UG380](#), *Spartan-6 FPGA Configuration User Guide*.

Pinout Tables

Summary

This chapter includes the pinout information tables for the packages cross-referenced by device in [Table 2-1](#). The ASCII text files of each device/package combination are available at <http://www.xilinx.com/support/packagefiles/spartan-6-pkgs.htm>.

Table 2-1: Cross-Reference for Pinout Tables

Device/ Package	TQG144	CPG196	CSG225	FT(G)256	CSG324	FG(G)484	CS(G)484	FG(G)676	FG(G)900
LX4	Table 2-2, page 30	Table 2-3, page 35	Table 2-4, page 42						
LX9	Table 2-2, page 30	Table 2-3, page 35	Table 2-5, page 50	Table 2-6, page 58	Table 2-7, page 67				
LX16		Table 2-3, page 35	Table 2-5, page 50	Table 2-6, page 58	Table 2-7, page 67				
LX25				Table 2-6, page 58	Table 2-7, page 67	Table 2-9, page 89			
LX25T					Table 2-8, page 78	Table 2-10, page 105			
LX45					Table 2-7, page 67	Table 2-9, page 89	Table 2-11, page 121	Table 2-13, page 153	
LX45T					Table 2-8, page 78	Table 2-10, page 105	Table 2-12, page 137		
LX75						Table 2-9, page 89	Table 2-11, page 121	Table 2-14, page 174	
LX75T						Table 2-10, page 105	Table 2-12, page 137	Table 2-15, page 195	
LX100						Table 2-9, page 89	Table 2-11, page 121	Table 2-14, page 174	
LX100T						Table 2-10, page 105	Table 2-12, page 137	Table 2-15, page 195	Table 2-17, page 244
LX150						Table 2-9, page 89	Table 2-11, page 121	Table 2-14, page 174	Table 2-16, page 216
LX150T						Table 2-10, page 105	Table 2-12, page 137	Table 2-15, page 195	Table 2-17, page 244

TQG144 Package—LX4 and LX9

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-2: TQG144 Package—LX4 and LX9

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	P144	TL	
0	IO_L1N_VREF_0	P143	TL	
0	IO_L2P_0	P142	TL	
0	IO_L2N_0	P141	TL	
0	IO_L3P_0	P140	TL	
0	IO_L3N_0	P139	TL	
0	IO_L4P_0	P138	TL	
0	IO_L4N_0	P137	TL	
0	IO_L34P_GCLK19_0	P134	TL	
0	IO_L34N_GCLK18_0	P133	TL	
0	IO_L35P_GCLK17_0	P132	TL	
0	IO_L35N_GCLK16_0	P131	TL	
0	IO_L36P_GCLK15_0	P127	TR	
0	IO_L36N_GCLK14_0	P126	TR	
0	IO_L37P_GCLK13_0	P124	TR	
0	IO_L37N_GCLK12_0	P123	TR	
0	IO_L62P_0	P121	TR	
0	IO_L62N_VREF_0	P120	TR	
0	IO_L63P_SCP7_0	P119	TR	

Table 2-2: TQG144 Package—LX4 and LX9 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L63N_SCP6_0	P118	TR	
0	IO_L64P_SCP5_0	P117	TR	
0	IO_L64N_SCP4_0	P116	TR	
0	IO_L65P_SCP3_0	P115	TR	
0	IO_L65N_SCP2_0	P114	TR	
0	IO_L66P_SCP1_0	P112	TR	
0	IO_L66N_SCP0_0	P111	TR	
NA	TCK	P109	NA	
NA	TDI	P110	NA	
NA	TMS	P107	NA	
NA	TDO	P106	NA	
1	IO_L1P_1	P105	RT	
1	IO_L1N_VREF_1	P104	RT	
1	IO_L32P_1	P102	RT	
1	IO_L32N_1	P101	RT	
1	IO_L33P_1	P100	RT	
1	IO_L33N_1	P99	RT	
1	IO_L34P_1	P98	RT	
1	IO_L34N_1	P97	RT	
1	IO_L40P_GCLK11_1	P95	RT	
1	IO_L40N_GCLK10_1	P94	RT	
1	IO_L41P_GCLK9_IRDY1_1	P93	RT	
1	IO_L41N_GCLK8_1	P92	RT	
1	IO_L42P_GCLK7_1	P88	RB	
1	IO_L42N_GCLK6_TRDY1_1	P87	RB	
1	IO_L43P_GCLK5_1	P85	RB	
1	IO_L43N_GCLK4_1	P84	RB	
1	IO_L45P_1	P83	RB	
1	IO_L45N_1	P82	RB	
1	IO_L46P_1	P81	RB	
1	IO_L46N_1	P80	RB	
1	IO_L47P_1	P79	RB	
1	IO_L47N_1	P78	RB	

Table 2-2: TQG144 Package—LX4 and LX9 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L74P_AWAKE_1	P75	RB	
1	IO_L74N_DOUT_BUSY_1	P74	RB	
NA	SUSPEND	P73	NA	
2	CMPCS_B_2	P72	NA	
2	DONE_2	P71	NA	
2	IO_L1P_CCLK_2	P70	BR	
2	IO_L1N_M0_CMPMISO_2	P69	BR	
2	IO_L2P_CMPCLK_2	P67	BR	
2	IO_L2N_CMPMOSI_2	P66	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P65	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	P64	BR	
2	IO_L12P_D1_MISO2_2	P62	BR	
2	IO_L12N_D2_MISO3_2	P61	BR	
2	IO_L13P_M1_2	P60	BR	
2	IO_L13N_D10_2	P59	BR	
2	IO_L14P_D11_2	P58	BR	
2	IO_L14N_D12_2	P57	BR	
2	IO_L30P_GCLK1_D13_2	P56	BR	
2	IO_L30N_GCLK0_USERCLK_2	P55	BR	
2	IO_L31P_GCLK31_D14_2	P51	BL	
2	IO_L31N_GCLK30_D15_2	P50	BL	
2	IO_L48P_D7_2	P48	BL	
2	IO_L48N_RDWR_B_VREF_2	P47	BL	
2	IO_L49P_D3_2	P46	BL	
2	IO_L49N_D4_2	P45	BL	
2	IO_L62P_D5_2	P44	BL	
2	IO_L62N_D6_2	P43	BL	
2	IO_L64P_D8_2	P41	BL	
2	IO_L64N_D9_2	P40	BL	
2	IO_L65P_INIT_B_2	P39	BL	
2	IO_L65N_CSO_B_2	P38	BL	
2	PROGRAM_B_2	P37	NA	
3	IO_L1P_3	P35	LB	

Table 2-2: TQG144 Package—LX4 and LX9 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L1N_VREF_3	P34	LB	
3	IO_L2P_3	P33	LB	
3	IO_L2N_3	P32	LB	
3	IO_L36P_3	P30	LB	
3	IO_L36N_3	P29	LB	
3	IO_L37P_3	P27	LB	
3	IO_L37N_3	P26	LB	
3	IO_L41P_GCLK27_3	P24	LB	
3	IO_L41N_GCLK26_3	P23	LB	
3	IO_L42P_GCLK25_TRDY2_3	P22	LB	
3	IO_L42N_GCLK24_3	P21	LB	
3	IO_L43P_GCLK23_3	P17	LT	
3	IO_L43N_GCLK22_IRDY2_3	P16	LT	
3	IO_L44P_GCLK21_3	P15	LT	
3	IO_L44N_GCLK20_3	P14	LT	
3	IO_L49P_3	P12	LT	
3	IO_L49N_3	P11	LT	
3	IO_L50P_3	P10	LT	
3	IO_L50N_3	P9	LT	
3	IO_L51P_3	P8	LT	
3	IO_L51N_3	P7	LT	
3	IO_L52P_3	P6	LT	
3	IO_L52N_3	P5	LT	
3	IO_L83P_3	P2	LT	
3	IO_L83N_VREF_3	P1	LT	
NA	GND	P108	NA	
NA	GND	P113	NA	
NA	GND	P13	NA	
NA	GND	P130	NA	
NA	GND	P136	NA	
NA	GND	P25	NA	
NA	GND	P3	NA	
NA	GND	P49	NA	

Table 2-2: TQG144 Package—LX4 and LX9 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	P54	NA	
NA	GND	P68	NA	
NA	GND	P77	NA	
NA	GND	P91	NA	
NA	GND	P96	NA	
NA	VCCAUX	P129	NA	
NA	VCCAUX	P20	NA	
NA	VCCAUX	P36	NA	
NA	VCCAUX	P53	NA	
NA	VCCAUX	P90	NA	
NA	VCCINT	P128	NA	
NA	VCCINT	P19	NA	
NA	VCCINT	P28	NA	
NA	VCCINT	P52	NA	
NA	VCCINT	P89	NA	
0	VCCO_0	P122	NA	
0	VCCO_0	P125	NA	
0	VCCO_0	P135	NA	
1	VCCO_1	P103	NA	
1	VCCO_1	P76	NA	
1	VCCO_1	P86	NA	
2	VCCO_2	P42	NA	
2	VCCO_2	P63	NA	
3	VCCO_3	P18	NA	
3	VCCO_3	P31	NA	
3	VCCO_3	P4	NA	

CPG196 Package—LX4, LX9, and LX16

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-3: CPG196 Package—LX4, LX9, and LX16

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B3	TL	
0	IO_L2N_0	A3	TL	
0	IO_L3P_0	B4	TL	
0	IO_L3N_0	A4	TL	
0	IO_L4P_0	B5	TL	
0	IO_L4N_0	A5	TL	
0	IO_L34P_GCLK19_0	B6	TL	
0	IO_L34N_GCLK18_0	A6	TL	
0	IO_L35P_GCLK17_0	B7	TL	
0	IO_L35N_GCLK16_0	A7	TL	
0	IO_L36P_GCLK15_0	D8	TR	
0	IO_L36N_GCLK14_0	C8	TR	
0	IO_L37P_GCLK13_0	B8	TR	
0	IO_L37N_GCLK12_0	A8	TR	
0	IO_L62P_0	B9	TR	
0	IO_L62N_VREF_0	A9	TR	
0	IO_L63P_SCP7_0	B10	TR	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L63N_SCP6_0	A10	TR	
0	IO_L64P_SCP5_0	B11	TR	
0	IO_L64N_SCP4_0	A11	TR	
0	IO_L65P_SCP3_0	B12	TR	
0	IO_L65N_SCP2_0	A12	TR	
0	IO_L66P_SCP1_0	D11	TR	
0	IO_L66N_SCP0_0	C11	TR	
NA	TCK	B13	NA	
NA	TDI	A13	NA	
NA	TMS	B14	NA	
NA	TDO	C14	NA	
1	IO_L1P_1	C12	RT	
1	IO_L1N_VREF_1	C13	RT	
1	IO_L32P_1	D13	RT	
1	IO_L32N_1	D14	RT	
1	IO_L33P_1	E13	RT	
1	IO_L33N_1	E14	RT	
1	IO_L34P_1	F11	RT	
1	IO_L34N_1	F12	RT	
1	IO_L40P_GCLK11_1	G13	RT	
1	IO_L40N_GCLK10_1	G14	RT	
1	IO_L41P_GCLK9_IRDY1_1	F13	RT	
1	IO_L41N_GCLK8_1	F14	RT	
1	IO_L42P_GCLK7_1	H13	RB	
1	IO_L42N_GCLK6_TRDY1_1	H14	RB	
1	IO_L43P_GCLK5_1	H11	RB	
1	IO_L43N_GCLK4_1	H12	RB	
1	IO_L45P_1	J13	RB	
1	IO_L45N_1	J14	RB	
1	IO_L46P_1	J11	RB	
1	IO_L46N_1	J12	RB	
1	IO_L47P_1	K13	RB	
1	IO_L47N_1	K14	RB	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L53P_1	L13	RB	
1	IO_L53N_VREF_1	L14	RB	
1	IO_L74P_AWAKE_1	M13	RB	
1	IO_L74N_DOUT_BUSY_1	M14	RB	
NA	SUSPEND	L12	NA	
2	CMPCS_B_2	M12	NA	
2	DONE_2	N14	NA	
2	IO_L1P_CCLK_2	N13	BR	
2	IO_L1N_M0_CPMISO_2	P13	BR	
2	IO_L2P_CMPCLK_2	N12	BR	
2	IO_L2N_CPMOSI_2	P12	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	N11	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	P11	BR	
2	IO_L12P_D1_MISO2_2	N10	BR	
2	IO_L12N_D2_MISO3_2	P10	BR	
2	IO_L13P_M1_2	N9	BR	
2	IO_L13N_D10_2	P9	BR	
2	IO_L14P_D11_2	L8	BR	
2	IO_L14N_D12_2	M8	BR	
2	IO_L30P_GCLK1_D13_2	N8	BR	
2	IO_L30N_GCLK0_USERCLK_2	P8	BR	
2	IO_L31P_GCLK31_D14_2	N7	BL	
2	IO_L31N_GCLK30_D15_2	P7	BL	
2	IO_L48P_D7_2	N6	BL	
2	IO_L48N_RDWR_B_VREF_2	P6	BL	
2	IO_L49P_D3_2	N5	BL	
2	IO_L49N_D4_2	P5	BL	
2	IO_L62P_D5_2	L4	BL	
2	IO_L62N_D6_2	M4	BL	
2	IO_L63P_2	N4	BL	
2	IO_L63N_2	P4	BL	
2	IO_L64P_D8_2	N3	BL	
2	IO_L64N_D9_2	P3	BL	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L65P_INIT_B_2	N2	BL	
2	IO_L65N_CSO_B_2	P2	BL	
2	PROGRAM_B_2	N1	NA	
3	IO_L1P_3	M2	LB	
3	IO_L1N_VREF_3	M1	LB	
3	IO_L2P_3	L2	LB	
3	IO_L2N_3	L1	LB	
3	IO_L36P_3	K2	LB	
3	IO_L36N_3	K1	LB	
3	IO_L37P_3	J4	LB	
3	IO_L37N_3	J3	LB	
3	IO_L41P_GCLK27_3	J2	LB	
3	IO_L41N_GCLK26_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_3	G2	LB	
3	IO_L42N_GCLK24_3	G1	LB	
3	IO_L43P_GCLK23_3	H2	LT	
3	IO_L43N_GCLK22_IRDY2_3	H1	LT	
3	IO_L44P_GCLK21_3	F2	LT	
3	IO_L44N_GCLK20_3	F1	LT	
3	IO_L49P_3	F4	LT	
3	IO_L49N_3	F3	LT	
3	IO_L50P_3	E2	LT	
3	IO_L50N_3	E1	LT	
3	IO_L51P_3	D4	LT	
3	IO_L51N_3	D3	LT	
3	IO_L52P_3	D2	LT	
3	IO_L52N_3	D1	LT	
3	IO_L83P_3	C1	LT	
3	IO_L83N_VREF_3	B1	LT	
NA	GND	A1	NA	
NA	GND	A14	NA	
NA	GND	C2	NA	
NA	GND	C3	NA	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	C6	NA	
NA	GND	C7	NA	
NA	GND	D10	NA	
NA	GND	D5	NA	
NA	GND	D6	NA	
NA	GND	D9	NA	
NA	GND	E11	NA	
NA	GND	E8	NA	
NA	GND	F7	NA	
NA	GND	F8	NA	
NA	GND	G5	NA	
NA	GND	G6	NA	
NA	GND	G7	NA	
NA	GND	G8	NA	
NA	GND	H10	NA	
NA	GND	H4	NA	
NA	GND	H7	NA	
NA	GND	H8	NA	
NA	GND	H9	NA	
NA	GND	J10	NA	
NA	GND	J7	NA	
NA	GND	J8	NA	
NA	GND	K8	NA	
NA	GND	L10	NA	
NA	GND	L11	NA	
NA	GND	L3	NA	
NA	GND	L5	NA	
NA	GND	L6	NA	
NA	GND	L9	NA	
NA	GND	M11	NA	
NA	GND	M3	NA	
NA	GND	M7	NA	
NA	GND	P1	NA	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	P14	NA	
NA	GND	G4	NA	
NA	VCCINT	E10	NA	
NA	VCCINT	E5	NA	
NA	VCCINT	E6	NA	
NA	VCCINT	E9	NA	
NA	VCCINT	F10	NA	
NA	VCCINT	F5	NA	
NA	VCCINT	F6	NA	
NA	VCCINT	F9	NA	
NA	VCCINT	J5	NA	
NA	VCCINT	J6	NA	
NA	VCCINT	J9	NA	
NA	VCCINT	K10	NA	
NA	VCCINT	K5	NA	
NA	VCCINT	K6	NA	
NA	VCCINT	K9	NA	
NA	VCCAUX	E7	NA	
NA	VCCAUX	G10	NA	
NA	VCCAUX	G9	NA	
NA	VCCAUX	H5	NA	
NA	VCCAUX	H6	NA	
NA	VCCAUX	K7	NA	
NA	VCCAUX	L7	NA	
NA	VCCAUX	D7	NA	
0	VCCO_0	C10	NA	
0	VCCO_0	C4	NA	
0	VCCO_0	C5	NA	
0	VCCO_0	C9	NA	
1	VCCO_1	D12	NA	
1	VCCO_1	E12	NA	
1	VCCO_1	G11	NA	
1	VCCO_1	G12	NA	

Table 2-3: CPG196 Package—LX4, LX9, and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	VCCO_1	K11	NA	
1	VCCO_1	K12	NA	
2	VCCO_2	M10	NA	
2	VCCO_2	M5	NA	
2	VCCO_2	M6	NA	
2	VCCO_2	M9	NA	
3	VCCO_3	G3	NA	
3	VCCO_3	E3	NA	
3	VCCO_3	E4	NA	
3	VCCO_3	H3	NA	
3	VCCO_3	K3	NA	
3	VCCO_3	K4	NA	

CSG225 Package—LX4

Although the LX4 devices are pin compatible with the LX9 and LX16 devices in the CSG225 package (see [Table 2-5, CSG225 Package—LX9 and LX16, on page 50](#)), the LX4 does not contain the Memory Controller block or support for BPI/Master Parallel mode. The dual-purpose pin names for these features are not the same as the LX4 pin names. For convenience, the No Connect column in [Table 2-5](#) lists the LX4 pins that are not connected.

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-4: CSG225 Package—LX4

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B3	TL	
0	IO_L2N_0	A3	TL	
0	IO_L3P_0	D5	TL	
0	IO_L3N_0	C5	TL	
0	IO_L4P_0	C4	TL	
0	IO_L4N_0	A4	TL	
0	IO_L6P_0	B5	TL	
0	IO_L6N_0	A5	TL	
0	IO_L33P_0	C6	TL	
0	IO_L33N_0	A6	TL	
0	IO_L34P_GCLK19_0	E7	TL	
0	IO_L34N_GCLK18_0	D8	TL	
0	IO_L35P_GCLK17_0	B7	TL	
0	IO_L35N_GCLK16_0	A7	TL	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L36P_GCLK15_0	C8	TR	
0	IO_L36N_GCLK14_0	A8	TR	
0	IO_L37P_GCLK13_0	B9	TR	
0	IO_L37N_GCLK12_0	A9	TR	
0	IO_L39P_0	D10	TR	
0	IO_L39N_0	C9	TR	
0	IO_L40P_0	F10	TR	
0	IO_L40N_0	E9	TR	
0	IO_L62P_0	C10	TR	
0	IO_L62N_VREF_0	A10	TR	
0	IO_L63P_SCP7_0	B11	TR	
0	IO_L63N_SCP6_0	A11	TR	
0	IO_L64P_SCP5_0	D11	TR	
0	IO_L64N_SCP4_0	C11	TR	
0	IO_L65P_SCP3_0	B13	TR	
0	IO_L65N_SCP2_0	A13	TR	
0	IO_L66P_SCP1_0	C12	TR	
0	IO_L66N_SCP0_0	A12	TR	
NA	TCK	A14	NA	
NA	TDI	E10	NA	
NA	TMS	E13	NA	
NA	TDO	D12	NA	
1	IO_L1P_1	B14	RT	
1	IO_L1N_VREF_1	B15	RT	
1	IO_L33P_1	C14	RT	
1	IO_L33N_1	C15	RT	
1	IO_L35P_1	D13	RT	
1	IO_L35N_1	D15	RT	
1	IO_L36P_1	J11	RT	
1	IO_L36N_1	J13	RT	
1	IO_L37P_1	E14	RT	
1	IO_L37N_1	E15	RT	
1	IO_L38P_1	K10	RT	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L38N_1	K11	RT	
1	IO_L39P_1	F13	RT	
1	IO_L39N_1	F15	RT	
1	IO_L40P_GCLK11_1	K12	RT	
1	IO_L40N_GCLK10_1	L12	RT	
1	IO_L41P_GCLK9_IRDY1_1	G14	RT	
1	IO_L41N_GCLK8_1	G15	RT	
1	IO_L42P_GCLK7_1	H13	RB	
1	IO_L42N_GCLK6_TRDY1_1	H15	RB	
1	IO_L43P_GCLK5_1	J14	RB	
1	IO_L43N_GCLK4_1	J15	RB	
1	IO_L44P_1	K13	RB	
1	IO_L44N_1	K15	RB	
1	IO_L45P_1	L14	RB	
1	IO_L45N_1	L15	RB	
1	IO_L46P_1	M13	RB	
1	IO_L46N_1	M15	RB	
1	IO_L47P_1	N14	RB	
1	IO_L47N_1	N15	RB	
1	IO_L74P_AWAKE_1	P14	RB	
1	IO_L74N_DOUT_BUSY_1	P15	RB	
NA	SUSPEND	L13	NA	
2	CMPCS_B_2	L10	NA	
2	DONE_2	R14	NA	
2	IO_L1P_CCLK_2	N12	BR	
2	IO_L1N_M0_CMPMISO_2	R12	BR	
2	IO_L2P_CMPCLK_2	P13	BR	
2	IO_L2N_CMPMOSI_2	R13	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P11	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	R11	BR	
2	IO_L12P_D1_MISO2_2	M11	BR	
2	IO_L12N_D2_MISO3_2	N11	BR	
2	IO_L13P_M1_2	N10	BR	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L13N_D10_2	R10	BR	
2	IO_L14P_D11_2	L9	BR	
2	IO_L14N_D12_2	M10	BR	
2	IO_L16P_2	P9	BR	
2	IO_L16N_VREF_2	R9	BR	
2	IO_L29P_GCLK3_2	N8	BR	
2	IO_L29N_GCLK2_2	R8	BR	
2	IO_L30P_GCLK1_D13_2	M8	BR	
2	IO_L30N_GCLK0_USERCLK_2	N7	BR	
2	IO_L31P_GCLK31_D14_2	K8	BL	
2	IO_L31N_GCLK30_D15_2	L8	BL	
2	IO_L32P_GCLK29_2	P7	BL	
2	IO_L32N_GCLK28_2	R7	BL	
2	IO_L48P_D7_2	N6	BL	
2	IO_L48N_RDWR_B_VREF_2	R6	BL	
2	IO_L49P_D3_2	P5	BL	
2	IO_L49N_D4_2	R5	BL	
2	IO_L62P_D5_2	L6	BL	
2	IO_L62N_D6_2	L5	BL	
2	IO_L63P_2	N4	BL	
2	IO_L63N_2	R4	BL	
2	IO_L64P_D8_2	M5	BL	
2	IO_L64N_D9_2	N5	BL	
2	IO_L65P_INIT_B_2	P3	BL	
2	IO_L65N_CSO_B_2	R3	BL	
2	PROGRAM_B_2	R2	NA	
3	IO_L1P_3	M4	LB	
3	IO_L1N_VREF_3	L3	LB	
3	IO_L2P_3	P2	LB	
3	IO_L2N_3	P1	LB	
3	IO_L37P_3	N2	LB	
3	IO_L37N_3	N1	LB	
3	IO_L38P_3	M3	LB	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L38N_3	M1	LB	
3	IO_L39P_3	L2	LB	
3	IO_L39N_3	L1	LB	
3	IO_L40P_3	K3	LB	
3	IO_L40N_3	K1	LB	
3	IO_L41P_GCLK27_3	J2	LB	
3	IO_L41N_GCLK26_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_3	H3	LB	
3	IO_L42N_GCLK24_3	H1	LB	
3	IO_L43P_GCLK23_3	K4	LT	
3	IO_L43N_GCLK22_IRDY2_3	J3	LT	
3	IO_L44P_GCLK21_3	G2	LT	
3	IO_L44N_GCLK20_3	G1	LT	
3	IO_L45P_3	K5	LT	
3	IO_L45N_3	J4	LT	
3	IO_L46P_3	F3	LT	
3	IO_L46N_3	F1	LT	
3	IO_L52P_3	E2	LT	
3	IO_L52N_3	E1	LT	
3	IO_L53P_3	D4	LT	
3	IO_L53N_3	E3	LT	
3	IO_L54P_3	D3	LT	
3	IO_L54N_3	D1	LT	
3	IO_L83P_3	C2	LT	
3	IO_L83N_VREF_3	C1	LT	
NA	GND	A1	NA	
NA	GND	A15	NA	
NA	GND	B10	NA	
NA	GND	B6	NA	
NA	GND	C13	NA	
NA	GND	C3	NA	
NA	GND	E11	NA	
NA	GND	F14	NA	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	F2	NA	
NA	GND	F6	NA	
NA	GND	G7	NA	
NA	GND	G9	NA	
NA	GND	H8	NA	
NA	GND	J7	NA	
NA	GND	J9	NA	
NA	GND	K14	NA	
NA	GND	K2	NA	
NA	GND	K6	NA	
NA	GND	L11	NA	
NA	GND	N13	NA	
NA	GND	N3	NA	
NA	GND	P10	NA	
NA	GND	P6	NA	
NA	GND	R1	NA	
NA	GND	R15	NA	
NA	VCCINT	F9	NA	
NA	VCCINT	G6	NA	
NA	VCCINT	G8	NA	
NA	VCCINT	H7	NA	
NA	VCCINT	H9	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K7	NA	
NA	VCCAUX	B1	NA	
NA	VCCAUX	E12	NA	
NA	VCCAUX	F7	NA	
NA	VCCAUX	G10	NA	
NA	VCCAUX	J6	NA	
NA	VCCAUX	K9	NA	
NA	VCCAUX	L4	NA	
NA	VCCAUX	M12	NA	

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	VCCO_0	B12	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	B8	NA	
0	VCCO_0	D9	NA	
1	VCCO_1	D14	NA	
1	VCCO_1	H14	NA	
1	VCCO_1	J12	NA	
1	VCCO_1	M14	NA	
2	VCCO_2	M7	NA	
2	VCCO_2	P12	NA	
2	VCCO_2	P4	NA	
2	VCCO_2	P8	NA	
3	VCCO_3	D2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	H2	NA	
3	VCCO_3	M2	NA	
NA	NOPAD/UNCONNECTED	E6		
NA	NOPAD/UNCONNECTED	D6		
NA	NOPAD/UNCONNECTED	D7		
NA	NOPAD/UNCONNECTED	C7		
NA	NOPAD/UNCONNECTED	F8		
NA	NOPAD/UNCONNECTED	E8		
NA	NOPAD/UNCONNECTED	G11		
NA	NOPAD/UNCONNECTED	G12		
NA	NOPAD/UNCONNECTED	F11		
NA	NOPAD/UNCONNECTED	F12		
NA	NOPAD/UNCONNECTED	H10		
NA	NOPAD/UNCONNECTED	H11		
NA	NOPAD/UNCONNECTED	H12		
NA	NOPAD/UNCONNECTED	G13		
NA	NOPAD/UNCONNECTED	M9		
NA	NOPAD/UNCONNECTED	N9		
NA	NOPAD/UNCONNECTED	L7		

Table 2-4: CSG225 Package—LX4 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	NOPAD/UNCONNECTED	M6		
NA	NOPAD/UNCONNECTED	J5		
NA	NOPAD/UNCONNECTED	H4		
NA	NOPAD/UNCONNECTED	G5		
NA	NOPAD/UNCONNECTED	G3		
NA	NOPAD/UNCONNECTED	H6		
NA	NOPAD/UNCONNECTED	H5		
NA	NOPAD/UNCONNECTED	F5		
NA	NOPAD/UNCONNECTED	F4		
NA	NOPAD/UNCONNECTED	E5		
NA	NOPAD/UNCONNECTED	E4		

CSG225 Package—LX9 and LX16

See [Table 2-4, CSG225 Package—LX4, on page 42](#) for LX4 pinouts.

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-5: CSG225 Package—LX9 and LX16

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B3	TL	
0	IO_L2N_0	A3	TL	
0	IO_L3P_0	D5	TL	
0	IO_L3N_0	C5	TL	
0	IO_L4P_0	C4	TL	
0	IO_L4N_0	A4	TL	
0	IO_L5P_0	E6	TL	LX4
0	IO_L5N_0	D6	TL	LX4
0	IO_L6P_0	B5	TL	
0	IO_L6N_0	A5	TL	
0	IO_L7P_0	D7	TL	LX4
0	IO_L7N_0	C7	TL	LX4
0	IO_L33P_0	C6	TL	
0	IO_L33N_0	A6	TL	
0	IO_L34P_GCLK19_0	E7	TL	
0	IO_L34N_GCLK18_0	D8	TL	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L35P_GCLK17_0	B7	TL	
0	IO_L35N_GCLK16_0	A7	TL	
0	IO_L36P_GCLK15_0	C8	TR	
0	IO_L36N_GCLK14_0	A8	TR	
0	IO_L37P_GCLK13_0	B9	TR	
0	IO_L37N_GCLK12_0	A9	TR	
0	IO_L38P_0	F8	TR	LX4
0	IO_L38N_VREF_0	E8	TR	LX4
0	IO_L39P_0	D10	TR	
0	IO_L39N_0	C9	TR	
0	IO_L40P_0	F10	TR	
0	IO_L40N_0	E9	TR	
0	IO_L62P_0	C10	TR	
0	IO_L62N_VREF_0	A10	TR	
0	IO_L63P_SCP7_0	B11	TR	
0	IO_L63N_SCP6_0	A11	TR	
0	IO_L64P_SCP5_0	D11	TR	
0	IO_L64N_SCP4_0	C11	TR	
0	IO_L65P_SCP3_0	B13	TR	
0	IO_L65N_SCP2_0	A13	TR	
0	IO_L66P_SCP1_0	C12	TR	
0	IO_L66N_SCP0_0	A12	TR	
NA	TCK	A14	NA	
NA	TDI	E10	NA	
NA	TMS	E13	NA	
NA	TDO	D12	NA	
1	IO_L1P_A25_1	B14	RT	
1	IO_L1N_A24_VREF_1	B15	RT	
1	IO_L30P_A21_M1RESET_1	G11	RT	LX4
1	IO_L30N_A20_M1A11_1	G12	RT	LX4
1	IO_L31P_A19_M1CKE_1	F11	RT	LX4
1	IO_L31N_A18_M1A12_1	F12	RT	LX4
1	IO_L32P_A17_M1A8_1	H10	RT	LX4

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L32N_A16_M1A9_1	H11	RT	LX4
1	IO_L33P_A15_M1A10_1	C14	RT	
1	IO_L33N_A14_M1A4_1	C15	RT	
1	IO_L34P_A13_M1WE_1	H12	RT	LX4
1	IO_L34N_A12_M1BA2_1	G13	RT	LX4
1	IO_L35P_A11_M1A7_1	D13	RT	
1	IO_L35N_A10_M1A2_1	D15	RT	
1	IO_L36P_A9_M1BA0_1	J11	RT	
1	IO_L36N_A8_M1BA1_1	J13	RT	
1	IO_L37P_A7_M1A0_1	E14	RT	
1	IO_L37N_A6_M1A1_1	E15	RT	
1	IO_L38P_A5_M1CLK_1	K10	RT	
1	IO_L38N_A4_M1CLKN_1	K11	RT	
1	IO_L39P_M1A3_1	F13	RT	
1	IO_L39N_M1ODT_1	F15	RT	
1	IO_L40P_GCLK11_M1A5_1	K12	RT	
1	IO_L40N_GCLK10_M1A6_1	L12	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	G14	RT	
1	IO_L41N_GCLK8_M1CASN_1	G15	RT	
1	IO_L42P_GCLK7_M1UDM_1	H13	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	H15	RB	
1	IO_L43P_GCLK5_M1DQ4_1	J14	RB	
1	IO_L43N_GCLK4_M1DQ5_1	J15	RB	
1	IO_L44P_A3_M1DQ6_1	K13	RB	
1	IO_L44N_A2_M1DQ7_1	K15	RB	
1	IO_L45P_A1_M1LDQS_1	L14	RB	
1	IO_L45N_A0_M1LDQSN_1	L15	RB	
1	IO_L46P_FCS_B_M1DQ2_1	M13	RB	
1	IO_L46N_FOE_B_M1DQ3_1	M15	RB	
1	IO_L47P_FWE_B_M1DQ0_1	N14	RB	
1	IO_L47N_LDC_M1DQ1_1	N15	RB	
1	IO_L74P_AWAKE_1	P14	RB	
1	IO_L74N_DOUT_BUSY_1	P15	RB	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	SUSPEND	L13	NA	
2	CMPCS_B_2	L10	NA	
2	DONE_2	R14	NA	
2	IO_L1P_CCLK_2	N12	BR	
2	IO_L1N_M0_CMPMISO_2	R12	BR	
2	IO_L2P_CMPCLK_2	P13	BR	
2	IO_L2N_CMPMOSI_2	R13	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P11	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	R11	BR	
2	IO_L12P_D1_MISO2_2	M11	BR	
2	IO_L12N_D2_MISO3_2	N11	BR	
2	IO_L13P_M1_2	N10	BR	
2	IO_L13N_D10_2	R10	BR	
2	IO_L14P_D11_2	L9	BR	
2	IO_L14N_D12_2	M10	BR	
2	IO_L15P_2	M9	BR	LX4
2	IO_L15N_2	N9	BR	LX4
2	IO_L16P_2	P9	BR	
2	IO_L16N_VREF_2	R9	BR	
2	IO_L29P_GCLK3_2	N8	BR	
2	IO_L29N_GCLK2_2	R8	BR	
2	IO_L30P_GCLK1_D13_2	M8	BR	
2	IO_L30N_GCLK0_USERCCLK_2	N7	BR	
2	IO_L31P_GCLK31_D14_2	K8	BL	
2	IO_L31N_GCLK30_D15_2	L8	BL	
2	IO_L32P_GCLK29_2	P7	BL	
2	IO_L32N_GCLK28_2	R7	BL	
2	IO_L47P_2	L7	BL	LX4
2	IO_L47N_2	M6	BL	LX4
2	IO_L48P_D7_2	N6	BL	
2	IO_L48N_RDWR_B_VREF_2	R6	BL	
2	IO_L49P_D3_2	P5	BL	
2	IO_L49N_D4_2	R5	BL	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L62P_D5_2	L6	BL	
2	IO_L62N_D6_2	L5	BL	
2	IO_L63P_2	N4	BL	
2	IO_L63N_2	R4	BL	
2	IO_L64P_D8_2	M5	BL	
2	IO_L64N_D9_2	N5	BL	
2	IO_L65P_INIT_B_2	P3	BL	
2	IO_L65N_CSO_B_2	R3	BL	
2	PROGRAM_B_2	R2	NA	
3	IO_L1P_3	M4	LB	
3	IO_L1N_VREF_3	L3	LB	
3	IO_L2P_3	P2	LB	
3	IO_L2N_3	P1	LB	
3	IO_L37P_M3DQ0_3	N2	LB	
3	IO_L37N_M3DQ1_3	N1	LB	
3	IO_L38P_M3DQ2_3	M3	LB	
3	IO_L38N_M3DQ3_3	M1	LB	
3	IO_L39P_M3LDQS_3	L2	LB	
3	IO_L39N_M3LDQSN_3	L1	LB	
3	IO_L40P_M3DQ6_3	K3	LB	
3	IO_L40N_M3DQ7_3	K1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	J2	LB	
3	IO_L41N_GCLK26_M3DQ5_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	H3	LB	
3	IO_L42N_GCLK24_M3LDM_3	H1	LB	
3	IO_L43P_GCLK23_M3RASN_3	K4	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	J3	LT	
3	IO_L44P_GCLK21_M3A5_3	G2	LT	
3	IO_L44N_GCLK20_M3A6_3	G1	LT	
3	IO_L45P_M3A3_3	K5	LT	
3	IO_L45N_M3ODT_3	J4	LT	
3	IO_L46P_M3CLK_3	F3	LT	
3	IO_L46N_M3CLKN_3	F1	LT	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L47P_M3A0_3	J5	LT	LX4
3	IO_L47N_M3A1_3	H4	LT	LX4
3	IO_L48P_M3BA0_3	G5	LT	LX4
3	IO_L48N_M3BA1_3	G3	LT	LX4
3	IO_L49P_M3A7_3	H6	LT	LX4
3	IO_L49N_M3A2_3	H5	LT	LX4
3	IO_L50P_M3WE_3	F5	LT	LX4
3	IO_L50N_M3BA2_3	F4	LT	LX4
3	IO_L51P_M3A10_3	E5	LT	LX4
3	IO_L51N_M3A4_3	E4	LT	LX4
3	IO_L52P_M3A8_3	E2	LT	
3	IO_L52N_M3A9_3	E1	LT	
3	IO_L53P_M3CKE_3	D4	LT	
3	IO_L53N_M3A12_3	E3	LT	
3	IO_L54P_M3RESET_3	D3	LT	
3	IO_L54N_M3A11_3	D1	LT	
3	IO_L83P_3	C2	LT	
3	IO_L83N_VREF_3	C1	LT	
NA	GND	A1	NA	
NA	GND	A15	NA	
NA	GND	B10	NA	
NA	GND	B6	NA	
NA	GND	C13	NA	
NA	GND	C3	NA	
NA	GND	E11	NA	
NA	GND	F14	NA	
NA	GND	F2	NA	
NA	GND	F6	NA	
NA	GND	G7	NA	
NA	GND	G9	NA	
NA	GND	H8	NA	
NA	GND	J7	NA	
NA	GND	J9	NA	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	K14	NA	
NA	GND	K2	NA	
NA	GND	K6	NA	
NA	GND	L11	NA	
NA	GND	N13	NA	
NA	GND	N3	NA	
NA	GND	P10	NA	
NA	GND	P6	NA	
NA	GND	R1	NA	
NA	GND	R15	NA	
NA	VCCAUX	B1	NA	
NA	VCCAUX	E12	NA	
NA	VCCAUX	F7	NA	
NA	VCCAUX	G10	NA	
NA	VCCAUX	J6	NA	
NA	VCCAUX	K9	NA	
NA	VCCAUX	L4	NA	
NA	VCCAUX	M12	NA	
NA	VCCINT	F9	NA	
NA	VCCINT	G6	NA	
NA	VCCINT	G8	NA	
NA	VCCINT	H7	NA	
NA	VCCINT	H9	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K7	NA	
0	VCCO_0	B12	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	B8	NA	
0	VCCO_0	D9	NA	
1	VCCO_1	D14	NA	
1	VCCO_1	H14	NA	
1	VCCO_1	J12	NA	

Table 2-5: CSG225 Package—LX9 and LX16 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	VCCO_1	M14	NA	
2	VCCO_2	M7	NA	
2	VCCO_2	P12	NA	
2	VCCO_2	P4	NA	
2	VCCO_2	P8	NA	
3	VCCO_3	D2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	H2	NA	
3	VCCO_3	M2	NA	

FT(G)256 Package—LX9, LX16, and LX25

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	C4	TL	
0	IO_L1N_VREF_0	A4	TL	
0	IO_L2P_0	B5	TL	
0	IO_L2N_0	A5	TL	
0	IO_L3P_0	D5	TL	
0	IO_L3N_0	C5	TL	
0	IO_L4P_0	B6	TL	
0	IO_L4N_0	A6	TL	
0	IO_L5P_0	F7	TL	
0	IO_L5N_0	E6	TL	
0	IO_L6P_0	C7	TL	
0	IO_L6N_0	A7	TL	
0	IO_L7P_0	D6	TL	
0	IO_L7N_0	C6	TL	
0	IO_L33P_0	B8	TL	
0	IO_L33N_0	A8	TL	
0	IO_L34P_GCLK19_0	C9	TL	
0	IO_L34N_GCLK18_0	A9	TL	
0	IO_L35P_GCLK17_0	B10	TL	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L35N_GCLK16_0	A10	TL	
0	IO_L36P_GCLK15_0	E7	TR	
0	IO_L36N_GCLK14_0	E8	TR	
0	IO_L37P_GCLK13_0	E10	TR	
0	IO_L37N_GCLK12_0	C10	TR	
0	IO_L38P_0	D8	TR	
0	IO_L38N_VREF_0	C8	TR	
0	IO_L39P_0	C11	TR	
0	IO_L39N_0	A11	TR	
0	IO_L40P_0	F9	TR	
0	IO_L40N_0	D9	TR	
0	IO_L62P_0	B12	TR	
0	IO_L62N_VREF_0	A12	TR	
0	IO_L63P_SCP7_0	C13	TR	
0	IO_L63N_SCP6_0	A13	TR	
0	IO_L64P_SCP5_0	F10	TR	
0	IO_L64N_SCP4_0	E11	TR	
0	IO_L65P_SCP3_0	B14	TR	
0	IO_L65N_SCP2_0	A14	TR	
0	IO_L66P_SCP1_0	D11	TR	
0	IO_L66N_SCP0_0	D12	TR	
NA	TCK	C14	NA	
NA	TDI	C12	NA	
NA	TMS	A15	NA	
NA	TDO	E14	NA	
1	IO_L1P_A25_1	E13	RT	
1	IO_L1N_A24_VREF_1	E12	RT	
1	IO_L29P_A23_M1A13_1	B15	RT	
1	IO_L29N_A22_M1A14_1	B16	RT	
1	IO_L30P_A21_M1RESET_1	F12	RT	
1	IO_L30N_A20_M1A11_1	G11	RT	
1	IO_L31P_A19_M1CKE_1	D14	RT	
1	IO_L31N_A18_M1A12_1	D16	RT	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L32P_A17_M1A8_1	F13	RT	
1	IO_L32N_A16_M1A9_1	F14	RT	
1	IO_L33P_A15_M1A10_1	C15	RT	
1	IO_L33N_A14_M1A4_1	C16	RT	
1	IO_L34P_A13_M1WE_1	E15	RT	
1	IO_L34N_A12_M1BA2_1	E16	RT	
1	IO_L35P_A11_M1A7_1	F15	RT	
1	IO_L35N_A10_M1A2_1	F16	RT	
1	IO_L36P_A9_M1BA0_1	G14	RT	
1	IO_L36N_A8_M1BA1_1	G16	RT	
1	IO_L37P_A7_M1A0_1	H15	RT	
1	IO_L37N_A6_M1A1_1	H16	RT	
1	IO_L38P_A5_M1CLK_1	G12	RT	
1	IO_L38N_A4_M1CLKN_1	H11	RT	
1	IO_L39P_M1A3_1	H13	RT (RB in LX25)	
1	IO_L39N_M1ODT_1	H14	RT (RB in LX25)	
1	IO_L40P_GCLK11_M1A5_1	J11	RT (RB in LX25)	
1	IO_L40N_GCLK10_M1A6_1	J12	RT (RB in LX25)	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	J13	RT (RB in LX25)	
1	IO_L41N_GCLK8_M1CASN_1	K14	RT (RB in LX25)	
1	IO_L42P_GCLK7_M1UDM_1	K12	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	K11	RB	
1	IO_L43P_GCLK5_M1DQ4_1	J14	RB	
1	IO_L43N_GCLK4_M1DQ5_1	J16	RB	
1	IO_L44P_A3_M1DQ6_1	K15	RB	
1	IO_L44N_A2_M1DQ7_1	K16	RB	
1	IO_L45P_A1_M1LDQS_1	N14	RB	
1	IO_L45N_A0_M1LDQSN_1	N16	RB	
1	IO_L46P_FCS_B_M1DQ2_1	M15	RB	
1	IO_L46N_FOE_B_M1DQ3_1	M16	RB	
1	IO_L47P_FWE_B_M1DQ0_1	L14	RB	
1	IO_L47N_LDC_M1DQ1_1	L16	RB	
1	IO_L48P_HDC_M1DQ8_1	P15	RB	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L48N_M1DQ9_1	P16	RB	
1	IO_L49P_M1DQ10_1	R15	RB	
1	IO_L49N_M1DQ11_1	R16	RB	
1	IO_L50P_M1UDQS_1	R14	RB	
1	IO_L50N_M1UDQSN_1	T15	RB	
1	IO_L51P_M1DQ12_1	T14	RB	
1	IO_L51N_M1DQ13_1	T13	RB	
1	IO_L52P_M1DQ14_1	R12	RB	
1	IO_L52N_M1DQ15_1	T12	RB	
1	IO_L53P_1	L12	RB	
1	IO_L53N_VREF_1	L13	RB	
1	IO_L74P_AWAKE_1	M13	RB	
1	IO_L74N_DOUT_BUSY_1	M14	RB	
NA	SUSPEND	P14	NA	
2	CMPCS_B_2	L11	NA	
2	DONE_2	P13	NA	
2	IO_L1P_CCLK_2	R11	BR	
2	IO_L1N_M0_CMPMISO_2	T11	BR	
2	IO_L2P_CMPCLK_2	M12	BR	
2	IO_L2N_CMPMOSI_2	M11	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	P10	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T10	BR	
2	IO_L12P_D1_MISO2_2	N12	BR	
2	IO_L12N_D2_MISO3_2	P12	BR	
2	IO_L13P_M1_2	N11	BR	
2	IO_L13N_D10_2	P11	BR	
2	IO_L14P_D11_2	N9	BR	
2	IO_L14N_D12_2	P9	BR	
2	IO_L16P_2	L10	BR	
2	IO_L16N_VREF_2	M10	BR	
2	IO_L23P_2	R9	BR	
2	IO_L23N_2	T9	BR	
2	IO_L29P_GCLK3_2	M9	BR	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L29N_GCLK2_2	N8	BR	
2	IO_L30P_GCLK1_D13_2	P8	BR	
2	IO_L30N_GCLK0_USERCCLK_2	T8	BR	
2	IO_L31P_GCLK31_D14_2	P7	BL	
2	IO_L31N_GCLK30_D15_2	M7	BL	
2	IO_L32P_GCLK29_2	R7	BL	
2	IO_L32N_GCLK28_2	T7	BL	
2	IO_L47P_2	P6	BL	
2	IO_L47N_2	T6	BL	
2	IO_L48P_D7_2	R5	BL	
2	IO_L48N_RDWR_B_VREF_2	T5	BL	
2	IO_L49P_D3_2	N5	BL	
2	IO_L49N_D4_2	P5	BL	
2	IO_L62P_D5_2	L8	BL	
2	IO_L62N_D6_2	L7	BL	
2	IO_L63P_2	P4	BL	
2	IO_L63N_2	T4	BL	
2	IO_L64P_D8_2	M6	BL	
2	IO_L64N_D9_2	N6	BL	
2	IO_L65P_INIT_B_2	R3	BL	
2	IO_L65N_CSO_B_2	T3	BL	
2	PROGRAM_B_2	T2	NA	
3	IO_L1P_3	M4	LB	
3	IO_L1N_VREF_3	M3	LB	
3	IO_L2P_3	M5	LB	
3	IO_L2N_3	N4	LB	
3	IO_L32P_M3DQ14_3	R2	LB	
3	IO_L32N_M3DQ15_3	R1	LB	
3	IO_L33P_M3DQ12_3	P2	LB	
3	IO_L33N_M3DQ13_3	P1	LB	
3	IO_L34P_M3UDQS_3	N3	LB	
3	IO_L34N_M3UDQSN_3	N1	LB	
3	IO_L35P_M3DQ10_3	M2	LB	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L35N_M3DQ11_3	M1	LB	
3	IO_L36P_M3DQ8_3	L3	LB	
3	IO_L36N_M3DQ9_3	L1	LB	
3	IO_L37P_M3DQ0_3	K2	LB	
3	IO_L37N_M3DQ1_3	K1	LB	
3	IO_L38P_M3DQ2_3	J3	LB	
3	IO_L38N_M3DQ3_3	J1	LB	
3	IO_L39P_M3LDQS_3	H2	LB	
3	IO_L39N_M3LDQSN_3	H1	LB	
3	IO_L40P_M3DQ6_3	G3	LB	
3	IO_L40N_M3DQ7_3	G1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	F2	LB	
3	IO_L41N_GCLK26_M3DQ5_3	F1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K3	LB	
3	IO_L42N_GCLK24_M3LDM_3	J4	LB	
3	IO_L43P_GCLK23_M3RASN_3	J6	LT (LB in LX25)	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	H5	LT (LB in LX25)	
3	IO_L44P_GCLK21_M3A5_3	H4	LT (LB in LX25)	
3	IO_L44N_GCLK20_M3A6_3	H3	LT (LB in LX25)	
3	IO_L45P_M3A3_3	L4	LT (LB in LX25)	
3	IO_L45N_M3ODT_3	L5	LT (LB in LX25)	
3	IO_L46P_M3CLK_3	E2	LT	
3	IO_L46N_M3CLKN_3	E1	LT	
3	IO_L47P_M3A0_3	K5	LT	
3	IO_L47N_M3A1_3	K6	LT	
3	IO_L48P_M3BA0_3	C3	LT	
3	IO_L48N_M3BA1_3	C2	LT	
3	IO_L49P_M3A7_3	D3	LT	
3	IO_L49N_M3A2_3	D1	LT	
3	IO_L50P_M3WE_3	C1	LT	
3	IO_L50N_M3BA2_3	B1	LT	
3	IO_L51P_M3A10_3	G6	LT	
3	IO_L51N_M3A4_3	G5	LT	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L52P_M3A8_3	B2	LT	
3	IO_L52N_M3A9_3	A2	LT	
3	IO_L53P_M3CKE_3	F4	LT	
3	IO_L53N_M3A12_3	F3	LT	
3	IO_L54P_M3RESET_3	E4	LT	
3	IO_L54N_M3A11_3	E3	LT	
3	IO_L55P_M3A13_3	F6	LT	
3	IO_L55N_M3A14_3	F5	LT	
3	IO_L83P_3	B3	LT	
3	IO_L83N_VREF_3	A3	LT	
NA	GND	A1	NA	
NA	GND	A16	NA	
NA	GND	B11	NA	
NA	GND	B7	NA	
NA	GND	D13	NA	
NA	GND	D4	NA	
NA	GND	E9	NA	
NA	GND	G15	NA	
NA	GND	G2	NA	
NA	GND	G8	NA	
NA	GND	H12	NA	
NA	GND	H7	NA	
NA	GND	H9	NA	
NA	GND	J5	NA	
NA	GND	J8	NA	
NA	GND	K7	NA	
NA	GND	K9	NA	
NA	GND	L15	NA	
NA	GND	L2	NA	
NA	GND	M8	NA	
NA	GND	N13	NA	
NA	GND	P3	NA	
NA	GND	R10	NA	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	R6	NA	
NA	GND	T1	NA	
NA	GND	T16	NA	
NA	VCCAUX	E5	NA	
NA	VCCAUX	F11	NA	
NA	VCCAUX	F8	NA	
NA	VCCAUX	G10	NA	
NA	VCCAUX	H6	NA	
NA	VCCAUX	J10	NA	
NA	VCCAUX	L6	NA	
NA	VCCAUX	L9	NA	
NA	VCCINT	G7	NA	
NA	VCCINT	G9	NA	
NA	VCCINT	H10	NA	
NA	VCCINT	H8	NA	
NA	VCCINT	J7	NA	
NA	VCCINT	J9	NA	
NA	VCCINT	K10	NA	
NA	VCCINT	K8	NA	
0	VCCO_0	B13	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	B9	NA	
0	VCCO_0	D10	NA	
0	VCCO_0	D7	NA	
1	VCCO_1	D15	NA	
1	VCCO_1	G13	NA	
1	VCCO_1	J15	NA	
1	VCCO_1	K13	NA	
1	VCCO_1	N15	NA	
1	VCCO_1	R13	NA	
2	VCCO_2	N10	NA	
2	VCCO_2	N7	NA	
2	VCCO_2	R4	NA	

Table 2-6: FT(G)256 Package—LX9, LX16, and LX25 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	VCCO_2	R8	NA	
3	VCCO_3	D2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	J2	NA	
3	VCCO_3	K4	NA	
3	VCCO_3	N2	NA	

CSG324 Package—LX9, LX16, LX25, and LX45

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	D4	TL	
0	IO_L1N_VREF_0	C4	TL	
0	IO_L2P_0	B2	TL	
0	IO_L2N_0	A2	TL	
0	IO_L3P_0	D6	TL	
0	IO_L3N_0	C6	TL	
0	IO_L4P_0	B3	TL	
0	IO_L4N_0	A3	TL	
0	IO_L5P_0	B4	TL	
0	IO_L5N_0	A4	TL	
0	IO_L6P_0	C5	TL	
0	IO_L6N_0	A5	TL	
0	IO_L7P_0	F7	TL	LX9, LX25, LX45
0	IO_L7N_0	E6	TL	LX9, LX25, LX45
0	IO_L8P_0	B6	TL	
0	IO_L8N_VREF_0	A6	TL	
0	IO_L9P_0	E7	TL	LX9, LX25, LX45
0	IO_L9N_0	E8	TL	LX9, LX25, LX45
0	IO_L10P_0	C7	TL	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L10N_0	A7	TL	
0	IO_L11P_0	D8	TL	
0	IO_L11N_0	C8	TL	
0	IO_L32P_0	G8	TL	LX9, LX25, LX45
0	IO_L32N_0	F8	TL	LX9, LX25, LX45
0	IO_L33P_0	B8	TL	
0	IO_L33N_0	A8	TL	
0	IO_L34P_GCLK19_0	D9	TL	
0	IO_L34N_GCLK18_0	C9	TL	
0	IO_L35P_GCLK17_0	B9	TL	
0	IO_L35N_GCLK16_0	A9	TL	
0	IO_L36P_GCLK15_0	D11	TR	
0	IO_L36N_GCLK14_0	C11	TR	
0	IO_L37P_GCLK13_0	C10	TR	
0	IO_L37N_GCLK12_0	A10	TR	
0	IO_L38P_0	G9	TR	
0	IO_L38N_VREF_0	F9	TR	
0	IO_L39P_0	B11	TR	
0	IO_L39N_0	A11	TR	
0	IO_L40P_0	G11	TR	LX9, LX45
0	IO_L40N_0	F10	TR	LX9, LX45
0	IO_L41P_0	B12	TR	
0	IO_L41N_0	A12	TR	
0	IO_L42P_0	F11	TR	LX9, LX45
0	IO_L42N_0	E11	TR	LX9, LX45
0	IO_L47P_0	D12	TR	LX9, LX45
0	IO_L47N_0	C12	TR	LX9, LX45
0	IO_L50P_0	C13	TR	LX9
0	IO_L50N_0	A13	TR	LX9
0	IO_L51P_0	F12	TR	LX9, LX45
0	IO_L51N_0	E12	TR	LX9, LX45
0	IO_L62P_0	B14	TR	
0	IO_L62N_VREF_0	A14	TR	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L63P_SCP7_0	F13	TR	
0	IO_L63N_SCP6_0	E13	TR	
0	IO_L64P_SCP5_0	C15	TR	
0	IO_L64N_SCP4_0	A15	TR	
0	IO_L65P_SCP3_0	D14	TR	
0	IO_L65N_SCP2_0	C14	TR	
0	IO_L66P_SCP1_0	B16	TR	
0	IO_L66N_SCP0_0	A16	TR	
NA	TCK	A17	NA	
NA	TDI	D15	NA	
NA	TMS	B18	NA	
NA	TDO	D16	NA	
1	IO_L1P_A25_1	F15	RT	
1	IO_L1N_A24_VREF_1	F16	RT	
1	IO_L29P_A23_M1A13_1	C17	RT	
1	IO_L29N_A22_M1A14_1	C18	RT	
1	IO_L30P_A21_M1RESET_1	F14	RT	
1	IO_L30N_A20_M1A11_1	G14	RT	
1	IO_L31P_A19_M1CKE_1	D17	RT	
1	IO_L31N_A18_M1A12_1	D18	RT	
1	IO_L32P_A17_M1A8_1	H12	RT	
1	IO_L32N_A16_M1A9_1	G13	RT	
1	IO_L33P_A15_M1A10_1	E16	RT	
1	IO_L33N_A14_M1A4_1	E18	RT	
1	IO_L34P_A13_M1WE_1	K12	RT	
1	IO_L34N_A12_M1BA2_1	K13	RT	
1	IO_L35P_A11_M1A7_1	F17	RT	
1	IO_L35N_A10_M1A2_1	F18	RT	
1	IO_L36P_A9_M1BA0_1	H13	RT	
1	IO_L36N_A8_M1BA1_1	H14	RT	
1	IO_L37P_A7_M1A0_1	H15	RT	
1	IO_L37N_A6_M1A1_1	H16	RT	
1	IO_L38P_A5_M1CLK_1	G16	RT	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L38N_A4_M1CLKN_1	G18	RT	
1	IO_L39P_M1A3_1	J13	RT (RB in LX25)	
1	IO_L39N_M1ODT_1	K14	RT (RB in LX25)	
1	IO_L40P_GCLK11_M1A5_1	L12	RT (RB in LX25)	
1	IO_L40N_GCLK10_M1A6_1	L13	RT (RB in LX25)	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K15	RT (RB in LX25)	
1	IO_L41N_GCLK8_M1CASN_1	K16	RT (RB in LX25)	
1	IO_L42P_GCLK7_M1UDM_1	L15	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L16	RB	
1	IO_L43P_GCLK5_M1DQ4_1	H17	RB	
1	IO_L43N_GCLK4_M1DQ5_1	H18	RB	
1	IO_L44P_A3_M1DQ6_1	J16	RB	
1	IO_L44N_A2_M1DQ7_1	J18	RB	
1	IO_L45P_A1_M1LDQS_1	K17	RB	
1	IO_L45N_A0_M1LDQSN_1	K18	RB	
1	IO_L46P_FCS_B_M1DQ2_1	L17	RB	
1	IO_L46N_FOE_B_M1DQ3_1	L18	RB	
1	IO_L47P_FWE_B_M1DQ0_1	M16	RB	
1	IO_L47N_LDC_M1DQ1_1	M18	RB	
1	IO_L48P_HDC_M1DQ8_1	N17	RB	
1	IO_L48N_M1DQ9_1	N18	RB	
1	IO_L49P_M1DQ10_1	P17	RB	
1	IO_L49N_M1DQ11_1	P18	RB	
1	IO_L50P_M1UDQS_1	N15	RB	
1	IO_L50N_M1UDQSN_1	N16	RB	
1	IO_L51P_M1DQ12_1	T17	RB	
1	IO_L51N_M1DQ13_1	T18	RB	
1	IO_L52P_M1DQ14_1	U17	RB	
1	IO_L52N_M1DQ15_1	U18	RB	
1	IO_L53P_1	M14	RB	
1	IO_L53N_VREF_1	N14	RB	
1	IO_L61P_1	L14	RB	
1	IO_L61N_1	M13	RB	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L74P_AWAKE_1	P15	RB	
1	IO_L74N_DOUT_BUSY_1	P16	RB	
NA	SUSPEND	R16	NA	
2	CMPCS_B_2	P13	NA	
2	DONE_2	V17	NA	
2	IO_L1P_CCLK_2	R15	BR	
2	IO_L1N_M0_CMPMISO_2	T15	BR	
2	IO_L2P_CMPCLK_2	U16	BR	
2	IO_L2N_CMPMOSI_2	V16	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	R13	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T13	BR	
2	IO_L5P_2	U15	BR	LX9
2	IO_L5N_2	V15	BR	LX9
2	IO_L12P_D1_MISO2_2	T14	BR	
2	IO_L12N_D2_MISO3_2	V14	BR	
2	IO_L13P_M1_2	N12	BR	
2	IO_L13N_D10_2	P12	BR	
2	IO_L14P_D11_2	U13	BR	
2	IO_L14N_D12_2	V13	BR	
2	IO_L15P_2	M11	BR	LX9
2	IO_L15N_2	N11	BR	LX9
2	IO_L16P_2	R11	BR	
2	IO_L16N_VREF_2	T11	BR	
2	IO_L19P_2	T12	BR	LX9
2	IO_L19N_2	V12	BR	LX9
2	IO_L20P_2	N10	BR	LX9
2	IO_L20N_2	P11	BR	LX9
2	IO_L22P_2	M10	BR	LX9
2	IO_L22N_2	N9	BR	LX9
2	IO_L23P_2	U11	BR	
2	IO_L23N_2	V11	BR	
2	IO_L29P_GCLK3_2	R10	BR	
2	IO_L29N_GCLK2_2	T10	BR	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L30P_GCLK1_D13_2	U10	BR	
2	IO_L30N_GCLK0_USERCCLK_2	V10	BR	
2	IO_L31P_GCLK31_D14_2	R8	BL	
2	IO_L31N_GCLK30_D15_2	T8	BL	
2	IO_L32P_GCLK29_2	T9	BL	
2	IO_L32N_GCLK28_2	V9	BL	
2	IO_L40P_2	M8	BL	LX9
2	IO_L40N_2	N8	BL	LX9
2	IO_L41P_2	U8	BL	
2	IO_L41N_VREF_2	V8	BL	
2	IO_L43P_2	U7	BL	
2	IO_L43N_2	V7	BL	
2	IO_L44P_2	N7	BL	LX9
2	IO_L44N_2	P8	BL	LX9
2	IO_L45P_2	T6	BL	
2	IO_L45N_2	V6	BL	
2	IO_L46P_2	R7	BL	
2	IO_L46N_2	T7	BL	
2	IO_L47P_2	N6	BL	LX9
2	IO_L47N_2	P7	BL	LX9
2	IO_L48P_D7_2	R5	BL	
2	IO_L48N_RDWR_B_VREF_2	T5	BL	
2	IO_L49P_D3_2	U5	BL	
2	IO_L49N_D4_2	V5	BL	
2	IO_L62P_D5_2	R3	BL	
2	IO_L62N_D6_2	T3	BL	
2	IO_L63P_2	T4	BL	
2	IO_L63N_2	V4	BL	
2	IO_L64P_D8_2	N5	BL	
2	IO_L64N_D9_2	P6	BL	
2	IO_L65P_INIT_B_2	U3	BL	
2	IO_L65N_CSO_B_2	V3	BL	
2	PROGRAM_B_2	V2	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L1P_3	N4	LB	
3	IO_L1N_VREF_3	N3	LB	
3	IO_L2P_3	P4	LB	
3	IO_L2N_3	P3	LB	
3	IO_L31P_3	L6	LB	
3	IO_L31N_VREF_3	M5	LB	
3	IO_L32P_M3DQ14_3	U2	LB	
3	IO_L32N_M3DQ15_3	U1	LB	
3	IO_L33P_M3DQ12_3	T2	LB	
3	IO_L33N_M3DQ13_3	T1	LB	
3	IO_L34P_M3UDQS_3	P2	LB	
3	IO_L34N_M3UDQSN_3	P1	LB	
3	IO_L35P_M3DQ10_3	N2	LB	
3	IO_L35N_M3DQ11_3	N1	LB	
3	IO_L36P_M3DQ8_3	M3	LB	
3	IO_L36N_M3DQ9_3	M1	LB	
3	IO_L37P_M3DQ0_3	L2	LB	
3	IO_L37N_M3DQ1_3	L1	LB	
3	IO_L38P_M3DQ2_3	K2	LB	
3	IO_L38N_M3DQ3_3	K1	LB	
3	IO_L39P_M3LDQS_3	L4	LB	
3	IO_L39N_M3LDQSN_3	L3	LB	
3	IO_L40P_M3DQ6_3	J3	LB	
3	IO_L40N_M3DQ7_3	J1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	H2	LB	
3	IO_L41N_GCLK26_M3DQ5_3	H1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	LB	
3	IO_L42N_GCLK24_M3LDM_3	K3	LB	
3	IO_L43P_GCLK23_M3RASN_3	L5	LT (LB in LX25)	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	LT (LB in LX25)	
3	IO_L44P_GCLK21_M3A5_3	H4	LT (LB in LX25)	
3	IO_L44N_GCLK20_M3A6_3	H3	LT (LB in LX25)	
3	IO_L45P_M3A3_3	L7	LT (LB in LX25)	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L45N_M3ODT_3	K6	LT (LB in LX25)	
3	IO_L46P_M3CLK_3	G3	LT	
3	IO_L46N_M3CLKN_3	G1	LT	
3	IO_L47P_M3A0_3	J7	LT	
3	IO_L47N_M3A1_3	J6	LT	
3	IO_L48P_M3BA0_3	F2	LT	
3	IO_L48N_M3BA1_3	F1	LT	
3	IO_L49P_M3A7_3	H6	LT	
3	IO_L49N_M3A2_3	H5	LT	
3	IO_L50P_M3WE_3	E3	LT	
3	IO_L50N_M3BA2_3	E1	LT	
3	IO_L51P_M3A10_3	F4	LT	
3	IO_L51N_M3A4_3	F3	LT	
3	IO_L52P_M3A8_3	D2	LT	
3	IO_L52N_M3A9_3	D1	LT	
3	IO_L53P_M3CKE_3	H7	LT	
3	IO_L53N_M3A12_3	G6	LT	
3	IO_L54P_M3RESET_3	E4	LT	
3	IO_L54N_M3A11_3	D3	LT	
3	IO_L55P_M3A13_3	F6	LT	
3	IO_L55N_M3A14_3	F5	LT	
3	IO_L83P_3	C2	LT	
3	IO_L83N_VREF_3	C1	LT	
NA	GND	A1	NA	
NA	GND	A18	NA	
NA	GND	B13	NA	
NA	GND	B7	NA	
NA	GND	C16	NA	
NA	GND	C3	NA	
NA	GND	D10	NA	
NA	GND	D5	NA	
NA	GND	E15	NA	
NA	GND	G12	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	G17	NA	
NA	GND	G2	NA	
NA	GND	G5	NA	
NA	GND	H10	NA	
NA	GND	H8	NA	
NA	GND	J11	NA	
NA	GND	J15	NA	
NA	GND	J4	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K8	NA	
NA	GND	L11	NA	
NA	GND	L9	NA	
NA	GND	M17	NA	
NA	GND	M2	NA	
NA	GND	M6	NA	
NA	GND	N13	NA	
NA	GND	R1	NA	
NA	GND	R14	NA	
NA	GND	R18	NA	
NA	GND	R4	NA	
NA	GND	R9	NA	
NA	GND	T16	NA	
NA	GND	U12	NA	
NA	GND	U6	NA	
NA	GND	V1	NA	
NA	GND	V18	NA	
NA	VCCAUX	B1	NA	
NA	VCCAUX	B17	NA	
NA	VCCAUX	E14	NA	
NA	VCCAUX	E5	NA	
NA	VCCAUX	E9	NA	
NA	VCCAUX	G10	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	J12	NA	
NA	VCCAUX	K7	NA	
NA	VCCAUX	M9	NA	
NA	VCCAUX	P10	NA	
NA	VCCAUX	P14	NA	
NA	VCCAUX	P5	NA	
NA	VCCINT	G7	NA	
NA	VCCINT	H11	NA	
NA	VCCINT	H9	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L8	NA	
NA	VCCINT	M12	NA	
NA	VCCINT	M7	NA	
0	VCCO_0	B10	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	B5	NA	
0	VCCO_0	D13	NA	
0	VCCO_0	D7	NA	
0	VCCO_0	E10	NA	
1	VCCO_1	E17	NA	
1	VCCO_1	G15	NA	
1	VCCO_1	J14	NA	
1	VCCO_1	J17	NA	
1	VCCO_1	M15	NA	
1	VCCO_1	R17	NA	
2	VCCO_2	P9	NA	
2	VCCO_2	R12	NA	
2	VCCO_2	R6	NA	
2	VCCO_2	U14	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	VCCO_2	U4	NA	
2	VCCO_2	U9	NA	
3	VCCO_3	E2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	J2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	M4	NA	
3	VCCO_3	R2	NA	

CSG324 Package—LX25T and LX45T

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-8: CSG324 Package—LX25T and LX45T

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B2	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B3	TL	
0	IO_L2N_0	A3	TL	
0	IO_L34P_GCLK19_0	E6	TL	
0	IO_L34N_GCLK18_0	F7	TL	
0	IO_L35P_GCLK17_0	G8	TL	
0	IO_L35N_GCLK16_0	E8	TL	
0	IO_L36P_GCLK15_0	G9	TR	
0	IO_L36N_GCLK14_0	G11	TR	
0	IO_L37P_GCLK13_0	F12	TR	
0	IO_L37N_GCLK12_0	E12	TR	
0	IO_L64P_SCP5_0	C15	TR	
0	IO_L64N_SCP4_0	A15	TR	
0	IO_L65P_SCP3_0	B16	TR	
0	IO_L65N_SCP2_0	A16	TR	
0	IO_L66P_SCP1_0	E14	TR	
0	IO_L66N_SCP0_0	D15	TR	
NA	TCK	A17	NA	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	TDI	F13	NA	
NA	TMS	B18	NA	
NA	TDO	D16	NA	
1	IO_L1P_A25_1	F15	RT	
1	IO_L1N_A24_VREF_1	F16	RT	
1	IO_L29P_A23_M1A13_1	C17	RT	
1	IO_L29N_A22_M1A14_1	C18	RT	
1	IO_L30P_A21_M1RESET_1	F14	RT	
1	IO_L30N_A20_M1A11_1	G14	RT	
1	IO_L31P_A19_M1CKE_1	D17	RT	
1	IO_L31N_A18_M1A12_1	D18	RT	
1	IO_L32P_A17_M1A8_1	H12	RT	
1	IO_L32N_A16_M1A9_1	G13	RT	
1	IO_L33P_A15_M1A10_1	E16	RT	
1	IO_L33N_A14_M1A4_1	E18	RT	
1	IO_L34P_A13_M1WE_1	K12	RT	
1	IO_L34N_A12_M1BA2_1	K13	RT	
1	IO_L35P_A11_M1A7_1	F17	RT	
1	IO_L35N_A10_M1A2_1	F18	RT	
1	IO_L36P_A9_M1BA0_1	H13	RT	
1	IO_L36N_A8_M1BA1_1	H14	RT	
1	IO_L37P_A7_M1A0_1	H15	RT	
1	IO_L37N_A6_M1A1_1	H16	RT	
1	IO_L38P_A5_M1CLK_1	G16	RT	
1	IO_L38N_A4_M1CLKN_1	G18	RT	
1	IO_L39P_M1A3_1	J13	RT (RB in LX25T)	
1	IO_L39N_M1ODT_1	K14	RT (RB in LX25T)	
1	IO_L40P_GCLK11_M1A5_1	L12	RT (RB in LX25T)	
1	IO_L40N_GCLK10_M1A6_1	L13	RT (RB in LX25T)	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K15	RT (RB in LX25T)	
1	IO_L41N_GCLK8_M1CASN_1	K16	RT (RB in LX25T)	
1	IO_L42P_GCLK7_M1UDM_1	L15	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L16	RB	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L43P_GCLK5_M1DQ4_1	H17	RB	
1	IO_L43N_GCLK4_M1DQ5_1	H18	RB	
1	IO_L44P_A3_M1DQ6_1	J16	RB	
1	IO_L44N_A2_M1DQ7_1	J18	RB	
1	IO_L45P_A1_M1LDQS_1	K17	RB	
1	IO_L45N_A0_M1LDQSN_1	K18	RB	
1	IO_L46P_FCS_B_M1DQ2_1	L17	RB	
1	IO_L46N_FOE_B_M1DQ3_1	L18	RB	
1	IO_L47P_FWE_B_M1DQ0_1	M16	RB	
1	IO_L47N_LDC_M1DQ1_1	M18	RB	
1	IO_L48P_HDC_M1DQ8_1	N17	RB	
1	IO_L48N_M1DQ9_1	N18	RB	
1	IO_L49P_M1DQ10_1	P17	RB	
1	IO_L49N_M1DQ11_1	P18	RB	
1	IO_L50P_M1UDQS_1	N15	RB	
1	IO_L50N_M1UDQSN_1	N16	RB	
1	IO_L51P_M1DQ12_1	T17	RB	
1	IO_L51N_M1DQ13_1	T18	RB	
1	IO_L52P_M1DQ14_1	U17	RB	
1	IO_L52N_M1DQ15_1	U18	RB	
1	IO_L53P_1	M14	RB	
1	IO_L53N_VREF_1	N14	RB	
1	IO_L61P_1	L14	RB	
1	IO_L61N_1	M13	RB	
1	IO_L74P_AWAKE_1	P15	RB	
1	IO_L74N_DOUT_BUSY_1	P16	RB	
NA	SUSPEND	R16	NA	
2	CMPCS_B_2	P13	NA	
2	DONE_2	V17	NA	
2	IO_L1P_CCLK_2	R15	BR	
2	IO_L1N_M0_CMPMISO_2	T15	BR	
2	IO_L2P_CMPCLK_2	U16	BR	
2	IO_L2N_CMPMOSI_2	V16	BR	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L3P_D0_DIN_MISO_MISO1_2	R13	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T13	BR	
2	IO_L5P_2	U15	BR	
2	IO_L5N_2	V15	BR	
2	IO_L12P_D1_MISO2_2	T14	BR	
2	IO_L12N_D2_MISO3_2	V14	BR	
2	IO_L13P_M1_2	N12	BR	
2	IO_L13N_D10_2	P12	BR	
2	IO_L14P_D11_2	U13	BR	
2	IO_L14N_D12_2	V13	BR	
2	IO_L15P_2	M11	BR	
2	IO_L15N_2	N11	BR	
2	IO_L16P_2	R11	BR	
2	IO_L16N_VREF_2	T11	BR	
2	IO_L19P_2	T12	BR	
2	IO_L19N_2	V12	BR	
2	IO_L20P_2	N10	BR	
2	IO_L20N_2	P11	BR	
2	IO_L22P_2	M10	BR	
2	IO_L22N_2	N9	BR	
2	IO_L23P_2	U11	BR	
2	IO_L23N_2	V11	BR	
2	IO_L29P_GCLK3_2	R10	BR	
2	IO_L29N_GCLK2_2	T10	BR	
2	IO_L30P_GCLK1_D13_2	U10	BR	
2	IO_L30N_GCLK0_USERCCLK_2	V10	BR	
2	IO_L31P_GCLK31_D14_2	R8	BL	
2	IO_L31N_GCLK30_D15_2	T8	BL	
2	IO_L32P_GCLK29_2	T9	BL	
2	IO_L32N_GCLK28_2	V9	BL	
2	IO_L40P_2	M8	BL	
2	IO_L40N_2	N8	BL	
2	IO_L41P_2	U8	BL	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L41N_VREF_2	V8	BL	
2	IO_L43P_2	U7	BL	
2	IO_L43N_2	V7	BL	
2	IO_L44P_2	N7	BL	
2	IO_L44N_2	P8	BL	
2	IO_L45P_2	T6	BL	
2	IO_L45N_2	V6	BL	
2	IO_L46P_2	R7	BL	
2	IO_L46N_2	T7	BL	
2	IO_L47P_2	N6	BL	
2	IO_L47N_2	P7	BL	
2	IO_L48P_D7_2	R5	BL	
2	IO_L48N_RDWR_B_VREF_2	T5	BL	
2	IO_L49P_D3_2	U5	BL	
2	IO_L49N_D4_2	V5	BL	
2	IO_L62P_D5_2	R3	BL	
2	IO_L62N_D6_2	T3	BL	
2	IO_L63P_2	T4	BL	
2	IO_L63N_2	V4	BL	
2	IO_L64P_D8_2	N5	BL	
2	IO_L64N_D9_2	P6	BL	
2	IO_L65P_INIT_B_2	U3	BL	
2	IO_L65N_CSO_B_2	V3	BL	
2	PROGRAM_B_2	V2	NA	
3	IO_L1P_3	N4	LB	
3	IO_L1N_VREF_3	N3	LB	
3	IO_L2P_3	P4	LB	
3	IO_L2N_3	P3	LB	
3	IO_L31P_3	L6	LB	
3	IO_L31N_VREF_3	M5	LB	
3	IO_L32P_M3DQ14_3	U2	LB	
3	IO_L32N_M3DQ15_3	U1	LB	
3	IO_L33P_M3DQ12_3	T2	LB	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L33N_M3DQ13_3	T1	LB	
3	IO_L34P_M3UDQS_3	P2	LB	
3	IO_L34N_M3UDQSN_3	P1	LB	
3	IO_L35P_M3DQ10_3	N2	LB	
3	IO_L35N_M3DQ11_3	N1	LB	
3	IO_L36P_M3DQ8_3	M3	LB	
3	IO_L36N_M3DQ9_3	M1	LB	
3	IO_L37P_M3DQ0_3	L2	LB	
3	IO_L37N_M3DQ1_3	L1	LB	
3	IO_L38P_M3DQ2_3	K2	LB	
3	IO_L38N_M3DQ3_3	K1	LB	
3	IO_L39P_M3LDQS_3	L4	LB	
3	IO_L39N_M3LDQSN_3	L3	LB	
3	IO_L40P_M3DQ6_3	J3	LB	
3	IO_L40N_M3DQ7_3	J1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	H2	LB	
3	IO_L41N_GCLK26_M3DQ5_3	H1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	LB	
3	IO_L42N_GCLK24_M3LDM_3	K3	LB	
3	IO_L43P_GCLK23_M3RASN_3	L5	LT (LB in LX25T)	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	LT (LB in LX25T)	
3	IO_L44P_GCLK21_M3A5_3	H4	LT (LB in LX25T)	
3	IO_L44N_GCLK20_M3A6_3	H3	LT (LB in LX25T)	
3	IO_L45P_M3A3_3	L7	LT (LB in LX25T)	
3	IO_L45N_M3ODT_3	K6	LT (LB in LX25T)	
3	IO_L46P_M3CLK_3	G3	LT	
3	IO_L46N_M3CLKN_3	G1	LT	
3	IO_L47P_M3A0_3	J7	LT	
3	IO_L47N_M3A1_3	J6	LT	
3	IO_L48P_M3BA0_3	F2	LT	
3	IO_L48N_M3BA1_3	F1	LT	
3	IO_L49P_M3A7_3	H6	LT	
3	IO_L49N_M3A2_3	H5	LT	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L50P_M3WE_3	E3	LT	
3	IO_L50N_M3BA2_3	E1	LT	
3	IO_L51P_M3A10_3	F4	LT	
3	IO_L51N_M3A4_3	F3	LT	
3	IO_L52P_M3A8_3	D2	LT	
3	IO_L52N_M3A9_3	D1	LT	
3	IO_L53P_M3CKE_3	H7	LT	
3	IO_L53N_M3A12_3	G6	LT	
3	IO_L54P_M3RESET_3	E4	LT	
3	IO_L54N_M3A11_3	D3	LT	
3	IO_L55P_M3A13_3	F6	LT	
3	IO_L55N_M3A14_3	F5	LT	
3	IO_L83P_3	C2	LT	
3	IO_L83N_VREF_3	C1	LT	
101	MGTTXN0_101	A4	NA	
101	MGTTXP0_101	B4	NA	
101	MGTAVCCPLL0_101	B7	NA	
101	MGTREFCLK0N_101	A8	NA	
101	MGTREFCLK0P_101	B8	NA	
101	MGTRXN0_101	C5	NA	
101	MGTRXP0_101	D5	NA	
101	MGTRREF_101	E7	NA	
101	MGTRXN1_101	C7	NA	
101	MGTAVTTRCAL_101	E5	NA	
101	MGTRXP1_101	D7	NA	
101	MGTAVCCPLL1_101	D10	NA	
101	MGTREFCLK1N_101	C9	NA	
101	MGTREFCLK1P_101	D9	NA	
101	MGTTXN1_101	A6	NA	
101	MGTTXP1_101	B6	NA	
123	MGTTXN0_123	A12	NA	LX25T
123	MGTTXP0_123	B12	NA	LX25T
123	MGTAVCCPLL0_123	B11	NA	LX25T

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
123	MGTREFCLK0N_123	A10	NA	LX25T
123	MGTREFCLK0P_123	B10	NA	LX25T
123	MGTRXN0_123	C11	NA	LX25T
123	MGTRXP0_123	D11	NA	LX25T
123	MGTRXN1_123	C13	NA	LX25T
123	MGTRXP1_123	D13	NA	LX25T
123	MGTAVCCPLL1_123	E11	NA	LX25T
123	MGTREFCLK1N_123	E10	NA	LX25T
123	MGTREFCLK1P_123	F10	NA	LX25T
123	MGTTXN1_123	A14	NA	LX25T
123	MGTTXP1_123	B14	NA	LX25T
NA	GND	A1	NA	
NA	GND	A11	NA	
NA	GND	A18	NA	
NA	GND	A7	NA	
NA	GND	A9	NA	
NA	GND	B13	NA	
NA	GND	B5	NA	
NA	GND	B9	NA	
NA	GND	C10	NA	
NA	GND	C12	NA	
NA	GND	C14	NA	
NA	GND	C16	NA	
NA	GND	C4	NA	
NA	GND	C6	NA	
NA	GND	D8	NA	
NA	GND	E13	NA	
NA	GND	E15	NA	
NA	GND	F11	NA	
NA	GND	F9	NA	
NA	GND	G17	NA	
NA	GND	G2	NA	
NA	GND	G5	NA	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	H10	NA	
NA	GND	H8	NA	
NA	GND	J11	NA	
NA	GND	J15	NA	
NA	GND	J4	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K8	NA	
NA	GND	L11	NA	
NA	GND	L9	NA	
NA	GND	M17	NA	
NA	GND	M2	NA	
NA	GND	M6	NA	
NA	GND	N13	NA	
NA	GND	R1	NA	
NA	GND	R14	NA	
NA	GND	R18	NA	
NA	GND	R4	NA	
NA	GND	R9	NA	
NA	GND	T16	NA	
NA	GND	U12	NA	
NA	GND	U6	NA	
NA	GND	V1	NA	
NA	GND	V18	NA	
NA	VCCAUX	B1	NA	
NA	VCCAUX	B17	NA	
NA	VCCAUX	D14	NA	
NA	VCCAUX	D4	NA	
NA	VCCAUX	G10	NA	
NA	VCCAUX	J12	NA	
NA	VCCAUX	K7	NA	
NA	VCCAUX	M9	NA	
NA	VCCAUX	P10	NA	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	P14	NA	
NA	VCCAUX	P5	NA	
NA	VCCINT	G7	NA	
NA	VCCINT	H11	NA	
NA	VCCINT	H9	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L8	NA	
NA	VCCINT	M12	NA	
NA	VCCINT	M7	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	C3	NA	
0	VCCO_0	F8	NA	
0	VCCO_0	G12	NA	
1	VCCO_1	E17	NA	
1	VCCO_1	G15	NA	
1	VCCO_1	J14	NA	
1	VCCO_1	J17	NA	
1	VCCO_1	M15	NA	
1	VCCO_1	R17	NA	
2	VCCO_2	P9	NA	
2	VCCO_2	R12	NA	
2	VCCO_2	R6	NA	
2	VCCO_2	U14	NA	
2	VCCO_2	U4	NA	
2	VCCO_2	U9	NA	
3	VCCO_3	E2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	J2	NA	
3	VCCO_3	J5	NA	

Table 2-8: CSG324 Package—LX25T and LX45T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	VCCO_3	M4	NA	
3	VCCO_3	R2	NA	
101	MGTAVTTTX_101	A5	NA	
123	MGTAVTTTX_123	A13	NA	LX25T
101	MGTAVTTRX_101	D6	NA	
123	MGTAVTTRX_123	D12	NA	LX25T
101	MGTAVCC_101	C8	NA	
123	MGTAVCC_123	E9	NA	LX25T

FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	TL	
0	IO_L1N_VREF_0	A4	TL	
0	IO_L2P_0	C5	TL	
0	IO_L2N_0	A5	TL	
0	IO_L3P_0	D6	TL	
0	IO_L3N_0	C6	TL	
0	IO_L4P_0	B6	TL	
0	IO_L4N_0	A6	TL	
0	IO_L5P_0	C7	TL	
0	IO_L5N_0	A7	TL	
0	IO_L6P_0	B8	TL	
0	IO_L6N_0	A8	TL	
0	IO_L7P_0	D9	TL	
0	IO_L7N_0	C8	TL	
0	IO_L8P_0	C9	TL	
0	IO_L8N_VREF_0	A9	TL	
0	IO_L14P_0	E8	TL	LX25, LX45, LX75
0	IO_L14N_0	F8	TL	LX25, LX45, LX75
0	IO_L15P_0	G8	TL	LX25, LX45, LX75

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L15N_0	F9	TL	LX25, LX45, LX75
0	IO_L16P_0	G9	TL	LX25, LX45, LX75
0	IO_L16N_0	H10	TL	LX25, LX45, LX75
0	IO_L17P_0	E10	TL	LX25, LX45, LX75
0	IO_L17N_0	F10	TL	LX25, LX45, LX75
0	IO_L18P_0	G11	TL	LX25, LX45, LX75
0	IO_L18N_0	H11	TL	LX25, LX45, LX75
0	IO_L32P_0	D7	TL	
0	IO_L32N_0	D8	TL	
0	IO_L33P_0	D10	TL	
0	IO_L33N_0	C10	TL	
0	IO_L34P_GCLK19_0	B10	TL	
0	IO_L34N_GCLK18_0	A10	TL	
0	IO_L35P_GCLK17_0	C11	TL	
0	IO_L35N_GCLK16_0	A11	TL	
0	IO_L36P_GCLK15_0	D11	TR	
0	IO_L36N_GCLK14_0	C12	TR	
0	IO_L37P_GCLK13_0	B12	TR	
0	IO_L37N_GCLK12_0	A12	TR	
0	IO_L38P_0	C13	TR	
0	IO_L38N_VREF_0	A13	TR	
0	IO_L43P_0	E12	TR (TL in LX75)	LX45
0	IO_L43N_0	D12	TR (TL in LX75)	LX45
0	IO_L44P_0	H12	TR	LX45, LX75
0	IO_L44N_0	F12	TR	LX45, LX75
0	IO_L45P_0	F13	TR (TL in LX75)	LX45
0	IO_L45N_0	D13	TR (TL in LX75)	LX45
0	IO_L46P_0	H13	TR	LX45
0	IO_L46N_0	G13	TR	LX45
0	IO_L47P_0	E14	TR	LX45
0	IO_L47N_0	F15	TR	LX45
0	IO_L48P_0	F14	TR	LX45
0	IO_L48N_0	H14	TR	LX45

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L49P_0	D14	TR	
0	IO_L49N_0	C14	TR	
0	IO_L50P_0	B14	TR	
0	IO_L50N_0	A14	TR	
0	IO_L51P_0	C15	TR	
0	IO_L51N_0	A15	TR	
0	IO_L62P_0	D15	TR	
0	IO_L62N_VREF_0	C16	TR	
0	IO_L63P_SCP7_0	B16	TR	
0	IO_L63N_SCP6_0	A16	TR	
0	IO_L64P_SCP5_0	C17	TR	
0	IO_L64N_SCP4_0	A17	TR	
0	IO_L65P_SCP3_0	B18	TR	
0	IO_L65N_SCP2_0	A18	TR	
0	IO_L66P_SCP1_0	E16	TR	
0	IO_L66N_SCP0_0	D17	TR	
NA	TCK	G15	NA	
NA	TDI	E18	NA	
NA	TMS	C18	NA	
NA	TDO	A19	NA	
1	IO_L1P_A25_1	C19	RT	
1	IO_L1N_A24_VREF_1	B20	RT	
1	IO_L9P_1	G16	RT	LX25
1	IO_L9N_1	G17	RT	LX25
1	IO_L10P_1	F16	RT	LX25
1	IO_L10N_1	F17	RT	LX25
1	IO_L19P_1	B21	RT	
1	IO_L19N_1	B22	RT	
1	IO_L20P_1	A20	RT	
1	IO_L20N_1	A21	RT	
1	IO_L21P_1	K16	RT	LX25
1	IO_L21N_1	J16	RT	LX25
1	IO_L28P_1	H16	RT	LX25

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L28N_VREF_1	H17	RT	LX25
1	IO_L29P_A23_M1A13_1	D19	RT	
1	IO_L29N_A22_M1A14_1	D20	RT	
1	IO_L30P_A21_M1RESET_1	F18	RT	
1	IO_L30N_A20_M1A11_1	F19	RT	
1	IO_L31P_A19_M1CKE_1	D21	RT	
1	IO_L31N_A18_M1A12_1	D22	RT	
1	IO_L32P_A17_M1A8_1	C20	RT	
1	IO_L32N_A16_M1A9_1	C22	RT	
1	IO_L33P_A15_M1A10_1	G19	RT	
1	IO_L33N_A14_M1A4_1	F20	RT	
1	IO_L34P_A13_M1WE_1	H19	RT	
1	IO_L34N_A12_M1BA2_1	H18	RT	
1	IO_L35P_A11_M1A7_1	E20	RT	
1	IO_L35N_A10_M1A2_1	E22	RT	
1	IO_L36P_A9_M1BA0_1	J17	RT	
1	IO_L36N_A8_M1BA1_1	K17	RT	
1	IO_L37P_A7_M1A0_1	F21	RT	
1	IO_L37N_A6_M1A1_1	F22	RT	
1	IO_L38P_A5_M1CLK_1	H20	RT	
1	IO_L38N_A4_M1CLKN_1	J19	RT	
1	IO_L39P_M1A3_1	G20	RT (RB in LX25)	
1	IO_L39N_M1ODT_1	G22	RT (RB in LX25)	
1	IO_L40P_GCLK11_M1A5_1	K20	RT (RB in LX25)	
1	IO_L40N_GCLK10_M1A6_1	K19	RT (RB in LX25)	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	H21	RT (RB in LX25)	
1	IO_L41N_GCLK8_M1CASN_1	H22	RT (RB in LX25)	
1	IO_L42P_GCLK7_M1UDM_1	M20	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L19	RB	
1	IO_L43P_GCLK5_M1DQ4_1	J20	RB	
1	IO_L43N_GCLK4_M1DQ5_1	J22	RB	
1	IO_L44P_A3_M1DQ6_1	K21	RB	
1	IO_L44N_A2_M1DQ7_1	K22	RB	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L45P_A1_M1LDQS_1	L20	RB	
1	IO_L45N_A0_M1LDQSN_1	L22	RB	
1	IO_L46P_FCS_B_M1DQ2_1	M21	RB	
1	IO_L46N_FOE_B_M1DQ3_1	M22	RB	
1	IO_L47P_FWE_B_M1DQ0_1	N20	RB	
1	IO_L47N_LDC_M1DQ1_1	N22	RB	
1	IO_L48P_HDC_M1DQ8_1	P21	RB	
1	IO_L48N_M1DQ9_1	P22	RB	
1	IO_L49P_M1DQ10_1	R20	RB	
1	IO_L49N_M1DQ11_1	R22	RB	
1	IO_L50P_M1UDQS_1	T21	RB	
1	IO_L50N_M1UDQSN_1	T22	RB	
1	IO_L51P_M1DQ12_1	U20	RB	
1	IO_L51N_M1DQ13_1	U22	RB	
1	IO_L52P_M1DQ14_1	V21	RB	
1	IO_L52N_M1DQ15_1	V22	RB	
1	IO_L53P_1	M19	RB	
1	IO_L53N_VREF_1	N19	RB	
1	IO_L58P_1	M16	RB	LX25
1	IO_L58N_1	L15	RB	LX25
1	IO_L59P_1	P19	RB	
1	IO_L59N_1	P20	RB	
1	IO_L60P_1	W20	RB	
1	IO_L60N_1	W22	RB	
1	IO_L61P_1	L17	RB	
1	IO_L61N_1	K18	RB	
1	IO_L70P_1	U19	RB	LX25
1	IO_L70N_1	V20	RB	LX25
1	IO_L71P_1	M17	RB	LX25
1	IO_L71N_1	M18	RB	LX25
1	IO_L72P_1	P17	RB	LX25
1	IO_L72N_1	N16	RB	LX25
1	IO_L73P_1	P18	RB	LX25

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L73N_1	R19	RB	LX25
1	IO_L74P_AWAKE_1	T19	RB	
1	IO_L74N_DOUT_BUSY_1	T20	RB	
NA	VFS	P16	NA	LX25, LX45
NA	RFUSE	P15	NA	LX25, LX45
NA	VBATT	R17	NA	LX25, LX45
NA	SUSPEND	N15	NA	
2	CMPCS_B_2	Y20	NA	
2	DONE_2	Y22	NA	
2	IO_L1P_CCLK_2	Y21	BR	
2	IO_L1N_M0_CMPMISO_2	AA22	BR	
2	IO_L2P_CMPCLK_2	AA21	BR	
2	IO_L2N_CMPMOSI_2	AB21	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AA20	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB20	BR	
2	IO_L4P_2	T18	BR	LX25
2	IO_L4N_VREF_2	T17	BR	LX25
2	IO_L5P_2	Y19	BR	
2	IO_L5N_2	AB19	BR	
2	IO_L6P_2	W18	BR	LX75
2	IO_L6N_2	Y18	BR	LX75
2	IO_L7P_2	T16	BR	LX25, LX75
2	IO_L7N_2	T15	BR	LX25, LX75
2	IO_L8P_2	U17	BR	LX25, LX75
2	IO_L8N_2	U16	BR	LX25, LX75
2	IO_L9P_2	V19	BR	LX25, LX75
2	IO_L9N_2	V18	BR	LX25, LX75
2	IO_L10P_2	R16	BR	LX25, LX75
2	IO_L10N_2	R15	BR	LX25, LX75
2	IO_L11P_2	V17	BR	LX25, LX75
2	IO_L11N_2	W17	BR	LX25, LX75
2	IO_L12P_D1_MISO2_2	U14	BR	
2	IO_L12N_D2_MISO3_2	U13	BR	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L13P_M1_2	U15	BR	
2	IO_L13N_D10_2	V15	BR	
2	IO_L14P_D11_2	AA18	BR	
2	IO_L14N_D12_2	AB18	BR	
2	IO_L15P_2	Y17	BR	
2	IO_L15N_2	AB17	BR	
2	IO_L16P_2	AA14	BR	
2	IO_L16N_VREF_2	AB14	BR	
2	IO_L17P_2	Y16	BR	LX75, LX100
2	IO_L17N_2	W15	BR	LX75, LX100
2	IO_L18P_2	V13	BR	LX75
2	IO_L18N_2	W13	BR	LX75
2	IO_L19P_2	AA16	BR	
2	IO_L19N_2	AB16	BR	
2	IO_L20P_2	W14	BR	LX75
2	IO_L20N_2	Y14	BR	LX75
2	IO_L21P_2	Y15	BR	
2	IO_L21N_2	AB15	BR	
2	IO_L22P_2	T12	BR	LX25, LX75, LX100
2	IO_L22N_2	U12	BR	LX25, LX75, LX100
2	IO_L23P_2	T14	BR	LX25, LX75
2	IO_L23N_2	R13	BR	LX25, LX75
2	IO_L29P_GCLK3_2	W12	BR	
2	IO_L29N_GCLK2_2	Y12	BR	
2	IO_L30P_GCLK1_D13_2	Y13	BR	
2	IO_L30N_GCLK0_USERCCLK_2	AB13	BR	
2	IO_L31P_GCLK31_D14_2	AA12	BL	
2	IO_L31N_GCLK30_D15_2	AB12	BL	
2	IO_L32P_GCLK29_2	Y11	BL	
2	IO_L32N_GCLK28_2	AB11	BL	
2	IO_L40P_2	R11	BL	LX75
2	IO_L40N_2	T11	BL	LX75
2	IO_L41P_2	AA10	BL	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L41N_VREF_2	AB10	BL	
2	IO_L42P_2	V11	BL	
2	IO_L42N_2	W11	BL	
2	IO_L43P_2	Y9	BL	
2	IO_L43N_2	AB9	BL	
2	IO_L44P_2	W10	BL	LX75
2	IO_L44N_2	Y10	BL	LX75
2	IO_L45P_2	AA8	BL	
2	IO_L45N_2	AB8	BL	
2	IO_L46P_2	W8	BL	LX75
2	IO_L46N_2	V7	BL	LX75
2	IO_L47P_2	W9	BL	LX75
2	IO_L47N_2	Y8	BL	LX75
2	IO_L48P_D7_2	Y7	BL	
2	IO_L48N_RDWR_B_VREF_2	AB7	BL	
2	IO_L49P_D3_2	AA6	BL	
2	IO_L49N_D4_2	AB6	BL	
2	IO_L50P_2	U9	BL	LX75
2	IO_L50N_2	V9	BL	LX75
2	IO_L51P_2	T8	BL	LX25, LX75, LX100
2	IO_L51N_2	U8	BL	LX25, LX75, LX100
2	IO_L52P_2	T10	BL	LX25, LX75, LX100
2	IO_L52N_2	U10	BL	LX25, LX75, LX100
2	IO_L53P_2	W6	BL	LX75, LX100
2	IO_L53N_2	Y6	BL	LX75, LX100
2	IO_L54P_2	Y5	BL	LX75, LX100
2	IO_L54N_2	AB5	BL	LX75, LX100
2	IO_L57P_2	AA4	BL	
2	IO_L57N_2	AB4	BL	
2	IO_L58P_2	Y3	BL	
2	IO_L58N_2	AB3	BL	
2	IO_L59P_2	R9	BL	LX75
2	IO_L59N_2	R8	BL	LX75

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L60P_2	T7	BL	LX75
2	IO_L60N_2	R7	BL	LX75
2	IO_L62P_D5_2	W4	BL	
2	IO_L62N_D6_2	Y4	BL	
2	IO_L63P_2	U6	BL	LX75
2	IO_L63N_2	V5	BL	LX75
2	IO_L64P_D8_2	AA2	BL	
2	IO_L64N_D9_2	AB2	BL	
2	IO_L65P_INIT_B_2	T6	BL	
2	IO_L65N_CSO_B_2	T5	BL	
2	PROGRAM_B_2	AA1	NA	
3	IO_L1P_3	Y2	LB	
3	IO_L1N_VREF_3	Y1	LB	
3	IO_L2P_3	W3	LB	
3	IO_L2N_3	W1	LB	
3	IO_L7P_3	P8	LB	LX25
3	IO_L7N_3	P7	LB	LX25
3	IO_L8P_3	P6	LB	LX25
3	IO_L8N_3	P5	LB	LX25
3	IO_L9P_3	T4	LB	
3	IO_L9N_3	T3	LB	
3	IO_L10P_3	U4	LB	
3	IO_L10N_3	V3	LB	
3	IO_L11P_3	N6	LB	LX25
3	IO_L11N_3	N7	LB	LX25
3	IO_L23P_3	M7	LB	LX25
3	IO_L23N_3	M8	LB	LX25
3	IO_L24P_3	R4	LB	LX25
3	IO_L24N_3	P4	LB	LX25
3	IO_L25P_3	M6	LB	LX25
3	IO_L25N_3	L6	LB	LX25
3	IO_L26P_3	P3	LB	LX25
3	IO_L26N_3	N4	LB	LX25

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L31P_3	M5	LB	
3	IO_L31N_VREF_3	M4	LB	
3	IO_L32P_M3DQ14_3	V2	LB	
3	IO_L32N_M3DQ15_3	V1	LB	
3	IO_L33P_M3DQ12_3	U3	LB	
3	IO_L33N_M3DQ13_3	U1	LB	
3	IO_L34P_M3UDQS_3	T2	LB	
3	IO_L34N_M3UDQSN_3	T1	LB	
3	IO_L35P_M3DQ10_3	R3	LB	
3	IO_L35N_M3DQ11_3	R1	LB	
3	IO_L36P_M3DQ8_3	P2	LB	
3	IO_L36N_M3DQ9_3	P1	LB	
3	IO_L37P_M3DQ0_3	N3	LB	
3	IO_L37N_M3DQ1_3	N1	LB	
3	IO_L38P_M3DQ2_3	M2	LB	
3	IO_L38N_M3DQ3_3	M1	LB	
3	IO_L39P_M3LDQS_3	L3	LB	
3	IO_L39N_M3LDQSN_3	L1	LB	
3	IO_L40P_M3DQ6_3	K2	LB	
3	IO_L40N_M3DQ7_3	K1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	J3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	M3	LB	
3	IO_L42N_GCLK24_M3LDM_3	L4	LB	
3	IO_L43P_GCLK23_M3RASN_3	K5	LT (LB in LX25)	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K4	LT (LB in LX25)	
3	IO_L44P_GCLK21_M3A5_3	K3	LT (LB in LX25)	
3	IO_L44N_GCLK20_M3A6_3	J4	LT (LB in LX25)	
3	IO_L45P_M3A3_3	K6	LT (LB in LX25)	
3	IO_L45N_M3ODT_3	J6	LT (LB in LX25)	
3	IO_L46P_M3CLK_3	H4	LT	
3	IO_L46N_M3CLKN_3	H3	LT	
3	IO_L47P_M3A0_3	H2	LT	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L47N_M3A1_3	H1	LT	
3	IO_L48P_M3BA0_3	G3	LT	
3	IO_L48N_M3BA1_3	G1	LT	
3	IO_L49P_M3A7_3	H6	LT	
3	IO_L49N_M3A2_3	H5	LT	
3	IO_L50P_M3WE_3	F2	LT	
3	IO_L50N_M3BA2_3	F1	LT	
3	IO_L51P_M3A10_3	G4	LT	
3	IO_L51N_M3A4_3	F3	LT	
3	IO_L52P_M3A8_3	E3	LT	
3	IO_L52N_M3A9_3	E1	LT	
3	IO_L53P_M3CKE_3	D2	LT	
3	IO_L53N_M3A12_3	D1	LT	
3	IO_L54P_M3RESET_3	C3	LT	
3	IO_L54N_M3A11_3	C1	LT	
3	IO_L55P_M3A13_3	G6	LT	
3	IO_L55N_M3A14_3	F5	LT	
3	IO_L57P_3	K7	LT	LX25
3	IO_L57N_VREF_3	K8	LT	LX25
3	IO_L58P_3	D5	LT	LX25
3	IO_L58N_3	E4	LT	LX25
3	IO_L59P_3	J7	LT	
3	IO_L59N_3	H8	LT	
3	IO_L60P_3	B2	LT	
3	IO_L60N_3	B1	LT	
3	IO_L80P_3	G7	LT	LX25
3	IO_L80N_3	F7	LT	LX25
3	IO_L81P_3	D3	LT	LX25
3	IO_L81N_3	C4	LT	LX25
3	IO_L82P_3	E5	LT	LX25
3	IO_L82N_3	E6	LT	LX25
3	IO_L83P_3	A2	LT	
3	IO_L83N_VREF_3	B3	LT	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	A1	NA	
NA	GND	A22	NA	
NA	GND	AA13	NA	
NA	GND	AA17	NA	
NA	GND	AA5	NA	
NA	GND	AA9	NA	
NA	GND	AB1	NA	
NA	GND	AB22	NA	
NA	GND	B13	NA	
NA	GND	B17	NA	
NA	GND	B5	NA	
NA	GND	B9	NA	
NA	GND	D18	NA	
NA	GND	D4	NA	
NA	GND	E11	NA	
NA	GND	E15	NA	
NA	GND	E2	NA	
NA	GND	E21	NA	
NA	GND	E7	NA	
NA	GND	G18	NA	
NA	GND	G5	NA	
NA	GND	H7	NA	
NA	GND	J11	NA	
NA	GND	J13	NA	
NA	GND	J15	NA	
NA	GND	J2	NA	
NA	GND	J21	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K12	NA	
NA	GND	K14	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	L18	NA	
NA	GND	L5	NA	
NA	GND	L9	NA	
NA	GND	M10	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	
NA	GND	N11	NA	
NA	GND	N13	NA	
NA	GND	N17	NA	
NA	GND	N2	NA	
NA	GND	N21	NA	
NA	GND	N9	NA	
NA	GND	P10	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	
NA	GND	R18	NA	
NA	GND	R5	NA	
NA	GND	U2	NA	
NA	GND	U21	NA	
NA	GND	U7	NA	
NA	GND	V10	NA	
NA	GND	V14	NA	
NA	GND	V4	NA	
NA	GND	W16	NA	
NA	GND	W19	NA	
NA	GND	W7	NA	
NA	VCCAUX	D16	NA	
NA	VCCAUX	F11	NA	
NA	VCCAUX	G12	NA	
NA	VCCAUX	H15	NA	
NA	VCCAUX	H9	NA	
NA	VCCAUX	K15	NA	
NA	VCCAUX	L8	NA	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	M15	NA	
NA	VCCAUX	N8	NA	
NA	VCCAUX	R10	NA	
NA	VCCAUX	R12	NA	
NA	VCCAUX	R6	NA	
NA	VCCAUX	U11	NA	
NA	VCCAUX	V6	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J12	NA	
NA	VCCINT	J14	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K13	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M9	NA	
NA	VCCINT	N10	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	P9	NA	
NA	VCCINT	R14	NA	
0	VCCO_0	B11	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	B19	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	B7	NA	
0	VCCO_0	E13	NA	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	VCCO_0	E17	NA	
0	VCCO_0	E9	NA	
0	VCCO_0	G10	NA	
0	VCCO_0	G14	NA	
1	VCCO_1	C21	NA	
1	VCCO_1	E19	NA	
1	VCCO_1	G21	NA	
1	VCCO_1	J18	NA	
1	VCCO_1	L16	NA	
1	VCCO_1	L21	NA	
1	VCCO_1	N18	NA	
1	VCCO_1	R21	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	W21	NA	
2	VCCO_2	AA11	NA	
2	VCCO_2	AA15	NA	
2	VCCO_2	AA19	NA	
2	VCCO_2	AA3	NA	
2	VCCO_2	AA7	NA	
2	VCCO_2	T13	NA	
2	VCCO_2	T9	NA	
2	VCCO_2	V12	NA	
2	VCCO_2	V16	NA	
2	VCCO_2	V8	NA	
2	VCCO_2	W5	NA	
3	VCCO_3	C2	NA	
3	VCCO_3	F4	NA	
3	VCCO_3	F6	NA	
3	VCCO_3	G2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	L2	NA	
3	VCCO_3	L7	NA	
3	VCCO_3	N5	NA	

Table 2-9: FG(G)484 Package—LX25, LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	VCCO_3	R2	NA	
3	VCCO_3	U5	NA	
3	VCCO_3	W2	NA	

FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	C3	TL	
0	IO_L1N_VREF_0	D3	TL	
0	IO_L2P_0	D4	TL	
0	IO_L2N_0	D5	TL	
0	IO_L3P_0	B2	TL	
0	IO_L3N_0	A2	TL	
0	IO_L4P_0	E5	TL	
0	IO_L4N_0	E6	TL	
0	IO_L5P_0	B3	TL	
0	IO_L5N_0	A3	TL	
0	IO_L6P_0	C4	TL	
0	IO_L6N_0	A4	TL	
0	IO_L7P_0	F7	TL	
0	IO_L7N_0	F8	TL	
0	IO_L8P_0	C5	TL	
0	IO_L8N_VREF_0	A5	TL	
101	MGTTXN0_101	A6	NA	
101	MGTTXP0_101	B6	NA	
101	MGTAVCCPLL0_101	B9	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
101	MGTREFCLK0N_101	B10	NA	
101	MGTREFCLK0P_101	A10	NA	
101	MGTRXN0_101	C7	NA	
101	MGTRXP0_101	D7	NA	
101	MGTREF_101	E9	NA	
101	MGTRXN1_101	C9	NA	
101	MGTAVTTRCAL_101	E8	NA	
101	MGTRXP1_101	D9	NA	
101	MGTAVCCPLL1_101	D12	NA	
101	MGTREFCLK1N_101	D11	NA	
101	MGTREFCLK1P_101	C11	NA	
101	MGTTXN1_101	A8	NA	
101	MGTTXP1_101	B8	NA	
0	IO_L32P_0	G8	TL	
0	IO_L32N_0	F9	TL	
0	IO_L33P_0	H10	TL	
0	IO_L33N_0	H11	TL	
0	IO_L34P_GCLK19_0	G9	TL	
0	IO_L34N_GCLK18_0	F10	TL	
0	IO_L35P_GCLK17_0	H12	TL	
0	IO_L35N_GCLK16_0	G11	TL	
0	IO_L36P_GCLK15_0	F14	TR	
0	IO_L36N_GCLK14_0	F15	TR	
0	IO_L37P_GCLK13_0	E16	TR	
0	IO_L37N_GCLK12_0	F16	TR	
0	IO_L38P_0	H13	TR	
0	IO_L38N_VREF_0	G13	TR	
123	MGTTXN0_123	A14	NA	LX25T
123	MGTTXP0_123	B14	NA	LX25T
123	MGTAVCCPLL0_123	B13	NA	LX25T
123	MGTREFCLK0N_123	B12	NA	LX25T
123	MGTREFCLK0P_123	A12	NA	LX25T
123	MGTRXN0_123	C13	NA	LX25T

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
123	MGTRXP0_123	D13	NA	LX25T
123	MGTRXN1_123	C15	NA	LX25T
123	MGTRXP1_123	D15	NA	LX25T
123	MGTAVCCPLL1_123	E13	NA	LX25T
123	MGTREFCLK1N_123	F12	NA	LX25T
123	MGTREFCLK1P_123	E12	NA	LX25T
123	MGTTXN1_123	A16	NA	LX25T
123	MGTTXP1_123	B16	NA	LX25T
0	IO_L49P_0	H14	TR	
0	IO_L49N_0	G15	TR	
0	IO_L50P_0	C17	TR	
0	IO_L50N_0	A17	TR	
0	IO_L51P_0	G16	TR	
0	IO_L51N_0	F17	TR	
0	IO_L62P_0	D18	TR	
0	IO_L62N_VREF_0	D19	TR	
0	IO_L63P_SCP7_0	B18	TR	
0	IO_L63N_SCP6_0	A18	TR	
0	IO_L64P_SCP5_0	C19	TR	
0	IO_L64N_SCP4_0	A19	TR	
0	IO_L65P_SCP3_0	B20	TR	
0	IO_L65N_SCP2_0	A20	TR	
0	IO_L66P_SCP1_0	D17	TR	
0	IO_L66N_SCP0_0	C18	TR	
NA	TCK	A21	NA	
NA	TDI	E18	NA	
NA	TMS	D20	NA	
NA	TDO	G17	NA	
1	IO_L1P_A25_1	F18	RT	
1	IO_L1N_A24_VREF_1	F19	RT	
1	IO_L9P_1	H16	RT	LX25T
1	IO_L9N_1	H17	RT	LX25T
1	IO_L10P_1	B21	RT	LX25T

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L10N_1	B22	RT	LX25T
1	IO_L19P_1	J16	RT	
1	IO_L19N_1	J17	RT	
1	IO_L20P_1	C20	RT	
1	IO_L20N_1	C22	RT	
1	IO_L21P_1	L15	RT	LX25T
1	IO_L21N_1	K16	RT	LX25T
1	IO_L28P_1	D21	RT	LX25T
1	IO_L28N_VREF_1	D22	RT	LX25T
1	IO_L29P_A23_M1A13_1	G19	RT	
1	IO_L29N_A22_M1A14_1	F20	RT	
1	IO_L30P_A21_M1RESET_1	H18	RT	
1	IO_L30N_A20_M1A11_1	H19	RT	
1	IO_L31P_A19_M1CKE_1	F21	RT	
1	IO_L31N_A18_M1A12_1	F22	RT	
1	IO_L32P_A17_M1A8_1	E20	RT	
1	IO_L32N_A16_M1A9_1	E22	RT	
1	IO_L33P_A15_M1A10_1	J19	RT	
1	IO_L33N_A14_M1A4_1	H20	RT	
1	IO_L34P_A13_M1WE_1	K19	RT	
1	IO_L34N_A12_M1BA2_1	K18	RT	
1	IO_L35P_A11_M1A7_1	G20	RT	
1	IO_L35N_A10_M1A2_1	G22	RT	
1	IO_L36P_A9_M1BA0_1	K17	RT	
1	IO_L36N_A8_M1BA1_1	L17	RT	
1	IO_L37P_A7_M1A0_1	H21	RT	
1	IO_L37N_A6_M1A1_1	H22	RT	
1	IO_L38P_A5_M1CLK_1	K20	RT	
1	IO_L38N_A4_M1CLKN_1	L19	RT	
1	IO_L39P_M1A3_1	J20	RT (RB in LX25T)	
1	IO_L39N_M1ODT_1	J22	RT (RB in LX25T)	
1	IO_L40P_GCLK11_M1A5_1	M20	RT (RB in LX25T)	
1	IO_L40N_GCLK10_M1A6_1	M19	RT (RB in LX25T)	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K21	RT (RB in LX25T)	
1	IO_L41N_GCLK8_M1CASN_1	K22	RT (RB in LX25T)	
1	IO_L42P_GCLK7_M1UDM_1	P20	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	N19	RB	
1	IO_L43P_GCLK5_M1DQ4_1	L20	RB	
1	IO_L43N_GCLK4_M1DQ5_1	L22	RB	
1	IO_L44P_A3_M1DQ6_1	M21	RB	
1	IO_L44N_A2_M1DQ7_1	M22	RB	
1	IO_L45P_A1_M1LDQS_1	N20	RB	
1	IO_L45N_A0_M1LDQSN_1	N22	RB	
1	IO_L46P_FCS_B_M1DQ2_1	P21	RB	
1	IO_L46N_FOE_B_M1DQ3_1	P22	RB	
1	IO_L47P_FWE_B_M1DQ0_1	R20	RB	
1	IO_L47N_LDC_M1DQ1_1	R22	RB	
1	IO_L48P_HDC_M1DQ8_1	T21	RB	
1	IO_L48N_M1DQ9_1	T22	RB	
1	IO_L49P_M1DQ10_1	U20	RB	
1	IO_L49N_M1DQ11_1	U22	RB	
1	IO_L50P_M1UDQS_1	V21	RB	
1	IO_L50N_M1UDQSN_1	V22	RB	
1	IO_L51P_M1DQ12_1	W20	RB	
1	IO_L51N_M1DQ13_1	W22	RB	
1	IO_L52P_M1DQ14_1	Y21	RB	
1	IO_L52N_M1DQ15_1	Y22	RB	
1	IO_L53P_1	P19	RB	
1	IO_L53N_VREF_1	R19	RB	
1	IO_L58P_1	M16	RB	LX25T
1	IO_L58N_1	N15	RB	LX25T
1	IO_L59P_1	U19	RB	
1	IO_L59N_1	T20	RB	
1	IO_L60P_1	N16	RB	
1	IO_L60N_1	P16	RB	
1	IO_L61P_1	M17	RB	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L61N_1	M18	RB	
1	IO_L70P_1	R15	RB	LX25T
1	IO_L70N_1	R16	RB	LX25T
1	IO_L71P_1	P17	RB	LX25T
1	IO_L71N_1	P18	RB	LX25T
1	IO_L72P_1	R17	RB	LX25T
1	IO_L72N_1	T17	RB	LX25T
1	IO_L73P_1	T19	RB	LX25T
1	IO_L73N_1	T18	RB	LX25T
1	IO_L74P_AWAKE_1	V19	RB	
1	IO_L74N_DOUT_BUSY_1	V20	RB	
NA	VFS	U17	NA	LX25T, LX45T
NA	RFUSE	P15	NA	LX25T, LX45T
NA	VBATT	T16	NA	LX25T, LX45T
NA	SUSPEND	AA22	NA	
2	CMPCS_B_2	V18	NA	
2	DONE_2	AB21	NA	
2	IO_L1P_CCLK_2	Y20	BR	
2	IO_L1N_M0_CMPMISO_2	AA21	BR	
2	IO_L2P_CMPCLK_2	V17	BR	
2	IO_L2N_CMPMOSI_2	W18	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AA20	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB20	BR	
2	IO_L4P_2	U16	BR	LX25T
2	IO_L4N_VREF_2	V15	BR	LX25T
2	IO_L5P_2	W17	BR	LX75T
2	IO_L5N_2	Y18	BR	LX75T
2	IO_L6P_2	AA14	BR	
2	IO_L6N_2	AB14	BR	
2	IO_L12P_D1_MISO2_2	R13	BR	
2	IO_L12N_D2_MISO3_2	T14	BR	
2	IO_L13P_M1_2	Y19	BR	
2	IO_L13N_D10_2	AB19	BR	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L14P_D11_2	AA18	BR	
2	IO_L14N_D12_2	AB18	BR	
2	IO_L15P_2	Y17	BR	
2	IO_L15N_2	AB17	BR	
2	IO_L16P_2	U14	BR	
2	IO_L16N_VREF_2	U13	BR	
2	IO_L17P_2	Y16	BR	LX75T
2	IO_L17N_2	W15	BR	LX75T
2	IO_L18P_2	V13	BR	LX75T
2	IO_L18N_2	W13	BR	LX75T
2	IO_L19P_2	AA16	BR	
2	IO_L19N_2	AB16	BR	
2	IO_L20P_2	W14	BR	LX75T
2	IO_L20N_2	Y14	BR	LX75T
2	IO_L21P_2	Y15	BR	
2	IO_L21N_2	AB15	BR	
2	IO_L22P_2	R11	BR	LX25T, LX75T
2	IO_L22N_2	T11	BR	LX25T, LX75T
2	IO_L23P_2	T15	BR	LX25T, LX75T
2	IO_L23N_2	U15	BR	LX25T, LX75T
2	IO_L29P_GCLK3_2	T12	BR	
2	IO_L29N_GCLK2_2	U12	BR	
2	IO_L30P_GCLK1_D13_2	Y13	BR	
2	IO_L30N_GCLK0_USERCLK_2	AB13	BR	
2	IO_L31P_GCLK31_D14_2	AA12	BL	
2	IO_L31N_GCLK30_D15_2	AB12	BL	
2	IO_L32P_GCLK29_2	Y11	BL	
2	IO_L32N_GCLK28_2	AB11	BL	
2	IO_L40P_2	W12	BL	
2	IO_L40N_2	Y12	BL	
2	IO_L41P_2	AA10	BL	
2	IO_L41N_VREF_2	AB10	BL	
2	IO_L42P_2	V11	BL	LX75T

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L42N_2	W11	BL	LX75T
2	IO_L43P_2	Y9	BL	
2	IO_L43N_2	AB9	BL	
2	IO_L44P_2	W10	BL	LX75T
2	IO_L44N_2	Y10	BL	LX75T
2	IO_L45P_2	AA8	BL	
2	IO_L45N_2	AB8	BL	
2	IO_L46P_2	T10	BL	LX75T
2	IO_L46N_2	U10	BL	LX75T
2	IO_L47P_2	Y7	BL	
2	IO_L47N_2	AB7	BL	
2	IO_L48P_D7_2	W9	BL	
2	IO_L48N_RDWR_B_VREF_2	Y8	BL	
2	IO_L49P_D3_2	AA6	BL	
2	IO_L49N_D4_2	AB6	BL	
2	IO_L50P_2	U9	BL	LX75T
2	IO_L50N_2	V9	BL	LX75T
2	IO_L57P_2	T8	BL	LX75T
2	IO_L57N_2	U8	BL	LX75T
2	IO_L58P_2	V7	BL	LX75T
2	IO_L58N_2	W8	BL	LX75T
2	IO_L59P_2	R9	BL	LX75T
2	IO_L59N_2	R8	BL	LX75T
2	IO_L60P_2	W6	BL	LX75T
2	IO_L60N_2	Y6	BL	LX75T
2	IO_L62P_D5_2	Y5	BL	
2	IO_L62N_D6_2	AB5	BL	
2	IO_L63P_2	AA4	BL	
2	IO_L63N_2	AB4	BL	
2	IO_L64P_D8_2	T7	BL	
2	IO_L64N_D9_2	U6	BL	
2	IO_L65P_INIT_B_2	Y4	BL	
2	IO_L65N_CSO_B_2	AA3	BL	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	PROGRAM_B_2	AB2	NA	
3	IO_L1P_3	R7	LB	
3	IO_L1N_VREF_3	P8	LB	
3	IO_L2P_3	W4	LB	
3	IO_L2N_3	Y3	LB	
3	IO_L7P_3	T6	LB	LX25T
3	IO_L7N_3	T5	LB	LX25T
3	IO_L8P_3	V5	LB	LX25T
3	IO_L8N_3	V3	LB	LX25T
3	IO_L9P_3	P5	LB	
3	IO_L9N_3	P4	LB	
3	IO_L10P_3	AA2	LB	
3	IO_L10N_3	AA1	LB	
3	IO_L23P_3	N6	LB	LX25T
3	IO_L23N_3	N7	LB	LX25T
3	IO_L24P_3	U4	LB	LX25T
3	IO_L24N_3	T4	LB	LX25T
3	IO_L25P_3	P6	LB	LX25T
3	IO_L25N_3	P7	LB	LX25T
3	IO_L26P_3	T3	LB	LX25T
3	IO_L26N_3	R4	LB	LX25T
3	IO_L31P_3	M7	LB	
3	IO_L31N_VREF_3	M8	LB	
3	IO_L32P_M3DQ14_3	Y2	LB	
3	IO_L32N_M3DQ15_3	Y1	LB	
3	IO_L33P_M3DQ12_3	W3	LB	
3	IO_L33N_M3DQ13_3	W1	LB	
3	IO_L34P_M3UDQS_3	V2	LB	
3	IO_L34N_M3UDQSN_3	V1	LB	
3	IO_L35P_M3DQ10_3	U3	LB	
3	IO_L35N_M3DQ11_3	U1	LB	
3	IO_L36P_M3DQ8_3	T2	LB	
3	IO_L36N_M3DQ9_3	T1	LB	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L37P_M3DQ0_3	R3	LB	
3	IO_L37N_M3DQ1_3	R1	LB	
3	IO_L38P_M3DQ2_3	P2	LB	
3	IO_L38N_M3DQ3_3	P1	LB	
3	IO_L39P_M3LDQS_3	N3	LB	
3	IO_L39N_M3LDQSN_3	N1	LB	
3	IO_L40P_M3DQ6_3	M2	LB	
3	IO_L40N_M3DQ7_3	M1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	L3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	L1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	P3	LB	
3	IO_L42N_GCLK24_M3LDM_3	N4	LB	
3	IO_L43P_GCLK23_M3RASN_3	M5	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	M4	LT	
3	IO_L44P_GCLK21_M3A5_3	M3	LT	
3	IO_L44N_GCLK20_M3A6_3	L4	LT	
3	IO_L45P_M3A3_3	M6	LT	
3	IO_L45N_M3ODT_3	L6	LT	
3	IO_L46P_M3CLK_3	K4	LT	
3	IO_L46N_M3CLKN_3	K3	LT	
3	IO_L47P_M3A0_3	K2	LT	
3	IO_L47N_M3A1_3	K1	LT	
3	IO_L48P_M3BA0_3	J3	LT	
3	IO_L48N_M3BA1_3	J1	LT	
3	IO_L49P_M3A7_3	K6	LT	
3	IO_L49N_M3A2_3	K5	LT	
3	IO_L50P_M3WE_3	H2	LT	
3	IO_L50N_M3BA2_3	H1	LT	
3	IO_L51P_M3A10_3	J4	LT	
3	IO_L51N_M3A4_3	H3	LT	
3	IO_L52P_M3A8_3	G3	LT	
3	IO_L52N_M3A9_3	G1	LT	
3	IO_L53P_M3CKE_3	F2	LT	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L53N_M3A12_3	F1	LT	
3	IO_L54P_M3RESET_3	E3	LT	
3	IO_L54N_M3A11_3	E1	LT	
3	IO_L55P_M3A13_3	J6	LT	
3	IO_L55N_M3A14_3	H5	LT	
3	IO_L57P_3	K7	LT	LX25T
3	IO_L57N_VREF_3	K8	LT	LX25T
3	IO_L58P_3	H4	LT	LX25T
3	IO_L58N_3	G4	LT	LX25T
3	IO_L59P_3	D2	LT	
3	IO_L59N_3	D1	LT	
3	IO_L60P_3	F3	LT	
3	IO_L60N_3	E4	LT	
3	IO_L80P_3	H6	LT	LX25T
3	IO_L80N_3	G7	LT	LX25T
3	IO_L81P_3	J7	LT	LX25T
3	IO_L81N_3	H8	LT	LX25T
3	IO_L82P_3	F5	LT	LX25T
3	IO_L82N_3	G6	LT	LX25T
3	IO_L83P_3	C1	LT	
3	IO_L83N_VREF_3	B1	LT	
NA	GND	A1	NA	
NA	GND	A11	NA	
NA	GND	A13	NA	
NA	GND	A22	NA	
NA	GND	A9	NA	
NA	GND	AA13	NA	
NA	GND	AA17	NA	
NA	GND	AA5	NA	
NA	GND	AA9	NA	
NA	GND	AB1	NA	
NA	GND	AB22	NA	
NA	GND	B11	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	B15	NA	
NA	GND	B17	NA	
NA	GND	B5	NA	
NA	GND	B7	NA	
NA	GND	C12	NA	
NA	GND	C14	NA	
NA	GND	C16	NA	
NA	GND	C6	NA	
NA	GND	C8	NA	
NA	GND	D10	NA	
NA	GND	D16	NA	
NA	GND	D6	NA	
NA	GND	E11	NA	
NA	GND	E14	NA	
NA	GND	E15	NA	
NA	GND	E2	NA	
NA	GND	E21	NA	
NA	GND	E7	NA	
NA	GND	F13	NA	
NA	GND	G18	NA	
NA	GND	G5	NA	
NA	GND	H7	NA	
NA	GND	J11	NA	
NA	GND	J13	NA	
NA	GND	J15	NA	
NA	GND	J2	NA	
NA	GND	J21	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K12	NA	
NA	GND	K14	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	L18	NA	
NA	GND	L5	NA	
NA	GND	L9	NA	
NA	GND	M10	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	
NA	GND	N11	NA	
NA	GND	N13	NA	
NA	GND	N17	NA	
NA	GND	N2	NA	
NA	GND	N21	NA	
NA	GND	N9	NA	
NA	GND	P10	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	
NA	GND	R18	NA	
NA	GND	R5	NA	
NA	GND	U2	NA	
NA	GND	U21	NA	
NA	GND	U7	NA	
NA	GND	V10	NA	
NA	GND	V14	NA	
NA	GND	V4	NA	
NA	GND	W16	NA	
NA	GND	W19	NA	
NA	GND	W7	NA	
101	MGTAVCC_101	C10	NA	
123	MGTAVCC_123	E10	NA	LX25T
101	MGTAVTTRX_101	D8	NA	
123	MGTAVTTRX_123	D14	NA	LX25T
101	MGTAVTTTX_101	A7	NA	
123	MGTAVTTTX_123	A15	NA	LX25T
NA	VCCAUX	F11	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	G12	NA	
NA	VCCAUX	H15	NA	
NA	VCCAUX	H9	NA	
NA	VCCAUX	K15	NA	
NA	VCCAUX	L8	NA	
NA	VCCAUX	M15	NA	
NA	VCCAUX	N8	NA	
NA	VCCAUX	R10	NA	
NA	VCCAUX	R12	NA	
NA	VCCAUX	R6	NA	
NA	VCCAUX	U11	NA	
NA	VCCAUX	V6	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J12	NA	
NA	VCCINT	J14	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K13	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M9	NA	
NA	VCCINT	N10	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	P9	NA	
NA	VCCINT	R14	NA	
0	VCCO_0	B19	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	VCCO_0	B4	NA	
0	VCCO_0	E17	NA	
0	VCCO_0	F6	NA	
0	VCCO_0	G10	NA	
0	VCCO_0	G14	NA	
1	VCCO_1	C21	NA	
1	VCCO_1	E19	NA	
1	VCCO_1	G21	NA	
1	VCCO_1	J18	NA	
1	VCCO_1	L16	NA	
1	VCCO_1	L21	NA	
1	VCCO_1	N18	NA	
1	VCCO_1	R21	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	W21	NA	
2	VCCO_2	AA11	NA	
2	VCCO_2	AA15	NA	
2	VCCO_2	AA19	NA	
2	VCCO_2	AA7	NA	
2	VCCO_2	AB3	NA	
2	VCCO_2	T13	NA	
2	VCCO_2	T9	NA	
2	VCCO_2	V12	NA	
2	VCCO_2	V16	NA	
2	VCCO_2	V8	NA	
2	VCCO_2	W5	NA	
3	VCCO_3	C2	NA	
3	VCCO_3	F4	NA	
3	VCCO_3	G2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	L2	NA	
3	VCCO_3	L7	NA	
3	VCCO_3	N5	NA	

Table 2-10: FG(G)484 Package—LX25T, LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	VCCO_3	R2	NA	
3	VCCO_3	U5	NA	
3	VCCO_3	W2	NA	

CS(G)484 Package—LX45, LX75, LX100, and LX150

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B3	TL	
0	IO_L1N_VREF_0	A4	TL	
0	IO_L2P_0	C5	TL	
0	IO_L2N_0	A5	TL	
0	IO_L3P_0	D6	TL	
0	IO_L3N_0	C6	TL	
0	IO_L4P_0	B6	TL	
0	IO_L4N_0	A6	TL	
0	IO_L5P_0	C7	TL	
0	IO_L5N_0	A7	TL	
0	IO_L6P_0	B8	TL	
0	IO_L6N_0	A8	TL	
0	IO_L7P_0	D7	TL	
0	IO_L7N_0	C8	TL	
0	IO_L8P_0	C9	TL	
0	IO_L8N_VREF_0	A9	TL	
0	IO_L15P_0	F9	TL	LX45
0	IO_L15N_0	E8	TL	LX45
0	IO_L16P_0	H10	TL	LX45

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L16N_0	G9	TL	LX45
0	IO_L32P_0	D9	TL	
0	IO_L32N_0	D8	TL	
0	IO_L33P_0	D10	TL	
0	IO_L33N_0	C10	TL	
0	IO_L34P_GCLK19_0	B10	TL	
0	IO_L34N_GCLK18_0	A10	TL	
0	IO_L35P_GCLK17_0	C11	TL	
0	IO_L35N_GCLK16_0	A11	TL	
0	IO_L36P_GCLK15_0	B12	TR	
0	IO_L36N_GCLK14_0	A12	TR	
0	IO_L37P_GCLK13_0	D11	TR	
0	IO_L37N_GCLK12_0	C12	TR	
0	IO_L38P_0	F10	TR	
0	IO_L38N_VREF_0	E10	TR	
0	IO_L46P_0	D15	TR	
0	IO_L46N_0	C14	TR	
0	IO_L47P_0	D13	TR	LX45
0	IO_L47N_0	D12	TR	LX45
0	IO_L48P_0	C13	TR	
0	IO_L48N_0	A13	TR	
0	IO_L49P_0	F12	TR	LX45
0	IO_L49N_0	E12	TR	LX45
0	IO_L50P_0	B14	TR	
0	IO_L50N_0	A14	TR	
0	IO_L51P_0	H11	TR	LX45
0	IO_L51N_0	G11	TR	LX45
0	IO_L62P_0	C15	TR	
0	IO_L62N_VREF_0	A15	TR	
0	IO_L63P_SCP7_0	B16	TR	
0	IO_L63N_SCP6_0	A16	TR	
0	IO_L64P_SCP5_0	C17	TR	
0	IO_L64N_SCP4_0	A17	TR	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L65P_SCP3_0	D17	TR	
0	IO_L65N_SCP2_0	C16	TR	
0	IO_L66P_SCP1_0	B18	TR	
0	IO_L66N_SCP0_0	A18	TR	
NA	TCK	D14	NA	
NA	TDI	E18	NA	
NA	TMS	E16	NA	
NA	TDO	E14	NA	
1	IO_L1P_A25_1	F15	RT	
1	IO_L1N_A24_VREF_1	F16	RT	
1	IO_L9P_1	F13	RT	
1	IO_L9N_1	F14	RT	
1	IO_L10P_1	G15	RT	
1	IO_L10N_1	G16	RT	
1	IO_L11P_1	D19	RT	
1	IO_L11N_1	D20	RT	
1	IO_L12P_1	C18	RT	
1	IO_L12N_1	C19	RT	
1	IO_L13P_1	G17	RT	
1	IO_L13N_1	G19	RT	
1	IO_L14P_1	B20	RT	
1	IO_L14N_1	A21	RT	
1	IO_L15P_1	F17	RT	
1	IO_L15N_1	F18	RT	
1	IO_L16P_1	A19	RT	
1	IO_L16N_1	A20	RT	
1	IO_L17P_1	H17	RT	
1	IO_L17N_1	H18	RT	
1	IO_L18P_1	F19	RT	
1	IO_L18N_1	F20	RT	
1	IO_L19P_1	H12	RT	
1	IO_L19N_1	G13	RT	
1	IO_L20P_1	J16	RT	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L20N_1	H16	RT	
1	IO_L21P_1	H13	RT	
1	IO_L21N_1	H14	RT	
1	IO_L28P_1	L15	RT	
1	IO_L28N_VREF_1	K16	RT	
1	IO_L29P_A23_M1A13_1	F21	RT	
1	IO_L29N_A22_M1A14_1	F22	RT	
1	IO_L30P_A21_M1RESET_1	H19	RT	
1	IO_L30N_A20_M1A11_1	H20	RT	
1	IO_L31P_A19_M1CKE_1	E20	RT	
1	IO_L31N_A18_M1A12_1	E22	RT	
1	IO_L32P_A17_M1A8_1	G20	RT	
1	IO_L32N_A16_M1A9_1	G22	RT	
1	IO_L33P_A15_M1A10_1	D21	RT	
1	IO_L33N_A14_M1A4_1	D22	RT	
1	IO_L34P_A13_M1WE_1	H21	RT	
1	IO_L34N_A12_M1BA2_1	H22	RT	
1	IO_L35P_A11_M1A7_1	C20	RT	
1	IO_L35N_A10_M1A2_1	C22	RT	
1	IO_L36P_A9_M1BA0_1	K18	RT	
1	IO_L36N_A8_M1BA1_1	K19	RT	
1	IO_L37P_A7_M1A0_1	B21	RT	
1	IO_L37N_A6_M1A1_1	B22	RT	
1	IO_L38P_A5_M1CLK_1	J17	RT	
1	IO_L38N_A4_M1CLKN_1	J19	RT	
1	IO_L39P_M1A3_1	J21	RT	
1	IO_L39N_M1ODT_1	J22	RT	
1	IO_L40P_GCLK11_M1A5_1	L17	RT	
1	IO_L40N_GCLK10_M1A6_1	K17	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	M18	RT	
1	IO_L41N_GCLK8_M1CASN_1	M19	RT	
1	IO_L42P_GCLK7_M1UDM_1	L19	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	K20	RB	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L43P_GCLK5_M1DQ4_1	L20	RB	
1	IO_L43N_GCLK4_M1DQ5_1	L22	RB	
1	IO_L44P_A3_M1DQ6_1	K21	RB	
1	IO_L44N_A2_M1DQ7_1	K22	RB	
1	IO_L45P_A1_M1LDQS_1	M21	RB	
1	IO_L45N_A0_M1LDQSN_1	M22	RB	
1	IO_L46P_FCS_B_M1DQ2_1	N19	RB	
1	IO_L46N_FOE_B_M1DQ3_1	M20	RB	
1	IO_L47P_FWE_B_M1DQ0_1	N20	RB	
1	IO_L47N_LDC_M1DQ1_1	N22	RB	
1	IO_L48P_HDC_M1DQ8_1	P21	RB	
1	IO_L48N_M1DQ9_1	P22	RB	
1	IO_L49P_M1DQ10_1	R20	RB	
1	IO_L49N_M1DQ11_1	R22	RB	
1	IO_L50P_M1UDQS_1	T21	RB	
1	IO_L50N_M1UDQSN_1	T22	RB	
1	IO_L51P_M1DQ12_1	U20	RB	
1	IO_L51N_M1DQ13_1	U22	RB	
1	IO_L52P_M1DQ14_1	V21	RB	
1	IO_L52N_M1DQ15_1	V22	RB	
1	IO_L53P_1	W20	RB	
1	IO_L53N_VREF_1	W22	RB	
1	IO_L58P_1	M16	RB	
1	IO_L58N_1	M17	RB	
1	IO_L59P_1	Y21	RB	
1	IO_L59N_1	Y22	RB	
1	IO_L60P_1	N15	RB	
1	IO_L60N_1	N16	RB	
1	IO_L61P_1	AA20	RB	
1	IO_L61N_1	AB21	RB	
1	IO_L62P_1	P15	RB	
1	IO_L62N_1	P16	RB	
1	IO_L63P_1	AA21	RB	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L63N_1	AA22	RB	
1	IO_L64P_1	P19	RB	
1	IO_L64N_1	P20	RB	
1	IO_L65P_1	AB19	RB	
1	IO_L65N_1	AB20	RB	
1	IO_L66P_1	P17	RB	
1	IO_L66N_1	P18	RB	
1	IO_L67P_1	Y19	RB	
1	IO_L67N_1	Y20	RB	
1	IO_L68P_1	R15	RB	
1	IO_L68N_1	R16	RB	
1	IO_L70P_1	R17	RB	
1	IO_L70N_1	R19	RB	
1	IO_L71P_1	V19	RB	
1	IO_L71N_1	V20	RB	
1	IO_L72P_1	T17	RB	
1	IO_L72N_1	T18	RB	
1	IO_L73P_1	V17	RB	
1	IO_L73N_1	V18	RB	
1	IO_L74P_AWAKE_1	T19	RB	
1	IO_L74N_DOUT_BUSY_1	T20	RB	
NA	VFS	U19	NA	LX45
NA	RFUSE	T16	NA	LX45
NA	VBATT	U17	NA	LX45
NA	SUSPEND	W18	NA	
2	CMPCS_B_2	T15	NA	
2	DONE_2	U16	NA	
2	IO_L1P_CCLK_2	W17	BR	
2	IO_L1N_M0_CPMISO_2	Y18	BR	
2	IO_L2P_CMPCLK_2	AA18	BR	
2	IO_L2N_CPMOSI_2	AB18	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	Y17	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB17	BR	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L4P_2	AA16	BR	
2	IO_L4N_VREF_2	AB16	BR	
2	IO_L5P_2	Y15	BR	
2	IO_L5N_2	AB15	BR	
2	IO_L12P_D1_MISO2_2	V13	BR	
2	IO_L12N_D2_MISO3_2	W13	BR	
2	IO_L13P_M1_2	U15	BR	
2	IO_L13N_D10_2	V15	BR	
2	IO_L14P_D11_2	W15	BR	
2	IO_L14N_D12_2	Y16	BR	
2	IO_L15P_2	AA14	BR	
2	IO_L15N_2	AB14	BR	
2	IO_L16P_2	W14	BR	
2	IO_L16N_VREF_2	Y14	BR	
2	IO_L20P_2	T14	BR	
2	IO_L20N_2	U14	BR	
2	IO_L29P_GCLK3_2	W11	BR	
2	IO_L29N_GCLK2_2	Y10	BR	
2	IO_L30P_GCLK1_D13_2	AA12	BR	
2	IO_L30N_GCLK0_USERCLK_2	AB12	BR	
2	IO_L31P_GCLK31_D14_2	Y11	BL	
2	IO_L31N_GCLK30_D15_2	AB11	BL	
2	IO_L32P_GCLK29_2	AA10	BL	
2	IO_L32N_GCLK28_2	AB10	BL	
2	IO_L33P_2	R13	BL	LX45
2	IO_L33N_2	U13	BL	LX45
2	IO_L34P_2	T12	BL	LX45
2	IO_L34N_2	U12	BL	LX45
2	IO_L41P_2	Y13	BL	
2	IO_L41N_VREF_2	AB13	BL	
2	IO_L42P_2	W12	BL	
2	IO_L42N_2	Y12	BL	
2	IO_L43P_2	R11	BL	LX75

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L43N_2	T11	BL	LX75
2	IO_L44P_2	V11	BL	LX75
2	IO_L44N_2	W10	BL	LX75
2	IO_L45P_2	T10	BL	LX75
2	IO_L45N_2	U10	BL	LX75
2	IO_L46P_2	U9	BL	LX75
2	IO_L46N_2	V9	BL	LX75
2	IO_L47P_2	W9	BL	
2	IO_L47N_2	Y8	BL	
2	IO_L48P_D7_2	Y9	BL	
2	IO_L48N_RDWR_B_VREF_2	AB9	BL	
2	IO_L49P_D3_2	AA8	BL	
2	IO_L49N_D4_2	AB8	BL	
2	IO_L50P_2	V7	BL	LX75
2	IO_L50N_2	W8	BL	LX75
2	IO_L62P_D5_2	W6	BL	
2	IO_L62N_D6_2	Y6	BL	
2	IO_L63P_2	Y7	BL	
2	IO_L63N_2	AB7	BL	
2	IO_L64P_D8_2	AA6	BL	
2	IO_L64N_D9_2	AB6	BL	
2	IO_L65P_INIT_B_2	Y5	BL	
2	IO_L65N_CSO_B_2	AB5	BL	
2	PROGRAM_B_2	AA1	NA	
3	IO_L1P_3	AA2	LB	
3	IO_L1N_VREF_3	AB2	LB	
3	IO_L2P_3	Y2	LB	
3	IO_L2N_3	Y1	LB	
3	IO_L7P_3	W4	LB	
3	IO_L7N_3	Y4	LB	
3	IO_L8P_3	Y3	LB	
3	IO_L8N_3	AB3	LB	
3	IO_L9P_3	W3	LB	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L9N_3	W1	LB	
3	IO_L10P_3	U8	LB	
3	IO_L10N_3	T7	LB	
3	IO_L11P_3	T8	LB	
3	IO_L11N_3	R7	LB	
3	IO_L12P_3	AA4	LB	
3	IO_L12N_3	AB4	LB	
3	IO_L13P_3	U6	LB	
3	IO_L13N_3	V5	LB	
3	IO_L18P_3	U4	LB	
3	IO_L18N_3	V3	LB	
3	IO_L19P_3	R9	LB	LX45
3	IO_L19N_3	R8	LB	LX45
3	IO_L20P_3	T6	LB	LX45
3	IO_L20N_3	T5	LB	LX45
3	IO_L21P_3	P4	LB	
3	IO_L21N_3	R4	LB	
3	IO_L22P_3	P6	LB	
3	IO_L22N_3	P5	LB	
3	IO_L23P_3	P8	LB	
3	IO_L23N_3	P7	LB	
3	IO_L24P_3	N7	LB	
3	IO_L24N_3	N6	LB	
3	IO_L25P_3	M8	LB	
3	IO_L25N_3	M7	LB	
3	IO_L26P_3	T4	LB	
3	IO_L26N_3	T3	LB	
3	IO_L31P_3	M6	LB	
3	IO_L31N_VREF_3	L6	LB	
3	IO_L32P_M3DQ14_3	V2	LB	
3	IO_L32N_M3DQ15_3	V1	LB	
3	IO_L33P_M3DQ12_3	U3	LB	
3	IO_L33N_M3DQ13_3	U1	LB	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L34P_M3UDQS_3	T2	LB	
3	IO_L34N_M3UDQSN_3	T1	LB	
3	IO_L35P_M3DQ10_3	R3	LB	
3	IO_L35N_M3DQ11_3	R1	LB	
3	IO_L36P_M3DQ8_3	P2	LB	
3	IO_L36N_M3DQ9_3	P1	LB	
3	IO_L37P_M3DQ0_3	N3	LB	
3	IO_L37N_M3DQ1_3	N1	LB	
3	IO_L38P_M3DQ2_3	M2	LB	
3	IO_L38N_M3DQ3_3	M1	LB	
3	IO_L39P_M3LDQS_3	L3	LB	
3	IO_L39N_M3LDQSN_3	L1	LB	
3	IO_L40P_M3DQ6_3	K2	LB	
3	IO_L40N_M3DQ7_3	K1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	J3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	H2	LB	
3	IO_L42N_GCLK24_M3LDM_3	H1	LB	
3	IO_L43P_GCLK23_M3RASN_3	N4	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P3	LT	
3	IO_L44P_GCLK21_M3A5_3	G3	LT	
3	IO_L44N_GCLK20_M3A6_3	G1	LT	
3	IO_L45P_M3A3_3	M4	LT	
3	IO_L45N_M3ODT_3	M3	LT	
3	IO_L46P_M3CLK_3	F2	LT	
3	IO_L46N_M3CLKN_3	F1	LT	
3	IO_L47P_M3A0_3	M5	LT	
3	IO_L47N_M3A1_3	L4	LT	
3	IO_L48P_M3BA0_3	E3	LT	
3	IO_L48N_M3BA1_3	E1	LT	
3	IO_L49P_M3A7_3	K4	LT	
3	IO_L49N_M3A2_3	K3	LT	
3	IO_L50P_M3WE_3	D2	LT	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L50N_M3BA2_3	D1	LT	
3	IO_L51P_M3A10_3	K6	LT	
3	IO_L51N_M3A4_3	K5	LT	
3	IO_L52P_M3A8_3	C3	LT	
3	IO_L52N_M3A9_3	C1	LT	
3	IO_L53P_M3CKE_3	J6	LT	
3	IO_L53N_M3A12_3	J4	LT	
3	IO_L54P_M3RESET_3	B2	LT	
3	IO_L54N_M3A11_3	B1	LT	
3	IO_L55P_M3A13_3	H4	LT	
3	IO_L55N_M3A14_3	H3	LT	
3	IO_L57P_3	H6	LT	
3	IO_L57N_VREF_3	H5	LT	
3	IO_L58P_3	H8	LT	
3	IO_L58N_3	J7	LT	
3	IO_L59P_3	K8	LT	
3	IO_L59N_3	K7	LT	
3	IO_L60P_3	E4	LT	
3	IO_L60N_3	F3	LT	
3	IO_L73P_3	G8	LT	
3	IO_L73N_3	G7	LT	
3	IO_L74P_3	G6	LT	
3	IO_L74N_3	G4	LT	
3	IO_L75P_3	F5	LT	
3	IO_L75N_3	E5	LT	
3	IO_L80P_3	F8	LT	
3	IO_L80N_3	F7	LT	
3	IO_L81P_3	C4	LT	
3	IO_L81N_3	D3	LT	
3	IO_L82P_3	E6	LT	
3	IO_L82N_3	D5	LT	
3	IO_L83P_3	A3	LT	
3	IO_L83N_VREF_3	A2	LT	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	A1	NA	
NA	GND	A22	NA	
NA	GND	B5	NA	
NA	GND	B9	NA	
NA	GND	B13	NA	
NA	GND	B17	NA	
NA	GND	D4	NA	
NA	GND	D18	NA	
NA	GND	E2	NA	
NA	GND	E7	NA	
NA	GND	E11	NA	
NA	GND	E15	NA	
NA	GND	E21	NA	
NA	GND	G5	NA	
NA	GND	G18	NA	
NA	GND	H7	NA	
NA	GND	J2	NA	
NA	GND	J9	NA	
NA	GND	J11	NA	
NA	GND	J13	NA	
NA	GND	J15	NA	
NA	GND	J20	NA	
NA	GND	K10	NA	
NA	GND	K12	NA	
NA	GND	K14	NA	
NA	GND	L5	NA	
NA	GND	L9	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	
NA	GND	L18	NA	
NA	GND	M10	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	N2	NA	
NA	GND	N9	NA	
NA	GND	N11	NA	
NA	GND	N13	NA	
NA	GND	N17	NA	
NA	GND	N21	NA	
NA	GND	P10	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	
NA	GND	R5	NA	
NA	GND	R18	NA	
NA	GND	U2	NA	
NA	GND	U7	NA	
NA	GND	U21	NA	
NA	GND	V4	NA	
NA	GND	V10	NA	
NA	GND	V14	NA	
NA	GND	W7	NA	
NA	GND	W16	NA	
NA	GND	W19	NA	
NA	GND	AA5	NA	
NA	GND	AA9	NA	
NA	GND	AA13	NA	
NA	GND	AA17	NA	
NA	GND	AB1	NA	
NA	GND	AB22	NA	
NA	VCCAUX	D16	NA	
NA	VCCAUX	F11	NA	
NA	VCCAUX	G12	NA	
NA	VCCAUX	H9	NA	
NA	VCCAUX	H15	NA	
NA	VCCAUX	K15	NA	
NA	VCCAUX	L8	NA	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	M15	NA	
NA	VCCAUX	N8	NA	
NA	VCCAUX	R6	NA	
NA	VCCAUX	R10	NA	
NA	VCCAUX	R12	NA	
NA	VCCAUX	U11	NA	
NA	VCCAUX	V6	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J12	NA	
NA	VCCINT	J14	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K13	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	M9	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	N10	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	P9	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	R14	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	B7	NA	
0	VCCO_0	B11	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	E9	NA	
0	VCCO_0	E13	NA	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	VCCO_0	E17	NA	
0	VCCO_0	G10	NA	
1	VCCO_1	B19	NA	
1	VCCO_1	C21	NA	
1	VCCO_1	E19	NA	
1	VCCO_1	G14	NA	
1	VCCO_1	G21	NA	
1	VCCO_1	J18	NA	
1	VCCO_1	L16	NA	
1	VCCO_1	L21	NA	
1	VCCO_1	N18	NA	
1	VCCO_1	R21	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	W21	NA	
1	VCCO_1	AA19	NA	
2	VCCO_2	T9	NA	
2	VCCO_2	T13	NA	
2	VCCO_2	V8	NA	
2	VCCO_2	V12	NA	
2	VCCO_2	V16	NA	
2	VCCO_2	AA7	NA	
2	VCCO_2	AA11	NA	
2	VCCO_2	AA15	NA	
3	VCCO_3	C2	NA	
3	VCCO_3	F4	NA	
3	VCCO_3	F6	NA	
3	VCCO_3	G2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	L2	NA	
3	VCCO_3	L7	NA	
3	VCCO_3	N5	NA	
3	VCCO_3	R2	NA	
3	VCCO_3	U5	NA	

Table 2-11: CS(G)484 Package—LX45, LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	VCCO_3	W2	NA	
3	VCCO_3	W5	NA	
3	VCCO_3	AA3	NA	

CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	B3	TL	
0	IO_L1N_VREF_0	A4	TL	
0	IO_L2P_0	C5	TL	
0	IO_L2N_0	A5	TL	
0	IO_L3P_0	F7	TL	
0	IO_L3N_0	E6	TL	
0	IO_L4P_0	E5	TL	
0	IO_L4N_0	D5	TL	
0	IO_L5P_0	G7	TL	
0	IO_L5N_0	G8	TL	
0	IO_L6P_0	F9	TL	
0	IO_L6N_0	E8	TL	
0	IO_L7P_0	G9	TL	
0	IO_L7N_0	F8	TL	
0	IO_L34P_GCLK19_0	H10	TL	
0	IO_L34N_GCLK18_0	G10	TL	
0	IO_L35P_GCLK17_0	F10	TL	
0	IO_L35N_GCLK16_0	F11	TL	
0	IO_L36P_GCLK15_0	H11	TR	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L36N_GCLK14_0	G11	TR	
0	IO_L37P_GCLK13_0	G12	TR	
0	IO_L37N_GCLK12_0	F12	TR	
0	IO_L38P_0	H12	TR	
0	IO_L38N_VREF_0	H13	TR	
0	IO_L49P_0	H14	TR	
0	IO_L49N_0	G15	TR	
0	IO_L50P_0	G16	TR	
0	IO_L50N_0	F16	TR	
0	IO_L51P_0	E16	TR	
0	IO_L51N_0	D17	TR	
0	IO_L62P_0	C17	TR	
0	IO_L62N_VREF_0	A17	TR	
0	IO_L63P_SCP7_0	B18	TR	
0	IO_L63N_SCP6_0	A18	TR	
0	IO_L64P_SCP5_0	B20	TR	
0	IO_L64N_SCP4_0	A19	TR	
0	IO_L65P_SCP3_0	D18	TR	
0	IO_L65N_SCP2_0	C18	TR	
0	IO_L66P_SCP1_0	D19	TR	
0	IO_L66N_SCP0_0	D20	TR	
NA	TCK	C19	NA	
NA	TDI	F17	NA	
NA	TMS	E18	NA	
NA	TDO	H16	NA	
1	IO_L1P_A25_1	G17	RT	
1	IO_L1N_A24_VREF_1	G19	RT	
1	IO_L15P_1	J16	RT	
1	IO_L15N_1	K17	RT	
1	IO_L16P_1	A20	RT	
1	IO_L16N_1	A21	RT	
1	IO_L17P_1	H17	RT	
1	IO_L17N_1	H18	RT	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L18P_1	F19	RT	
1	IO_L18N_1	F20	RT	
1	IO_L19P_1	N16	RT	
1	IO_L19N_1	M16	RT	
1	IO_L20P_1	L15	RT	
1	IO_L20N_1	K16	RT	
1	IO_L28P_1	N14	RT	
1	IO_L28N_VREF_1	N15	RT	
1	IO_L29P_A23_M1A13_1	F21	RT	
1	IO_L29N_A22_M1A14_1	F22	RT	
1	IO_L30P_A21_M1RESET_1	H19	RT	
1	IO_L30N_A20_M1A11_1	H20	RT	
1	IO_L31P_A19_M1CKE_1	E20	RT	
1	IO_L31N_A18_M1A12_1	E22	RT	
1	IO_L32P_A17_M1A8_1	G20	RT	
1	IO_L32N_A16_M1A9_1	G22	RT	
1	IO_L33P_A15_M1A10_1	D21	RT	
1	IO_L33N_A14_M1A4_1	D22	RT	
1	IO_L34P_A13_M1WE_1	H21	RT	
1	IO_L34N_A12_M1BA2_1	H22	RT	
1	IO_L35P_A11_M1A7_1	C20	RT	
1	IO_L35N_A10_M1A2_1	C22	RT	
1	IO_L36P_A9_M1BA0_1	K18	RT	
1	IO_L36N_A8_M1BA1_1	K19	RT	
1	IO_L37P_A7_M1A0_1	B21	RT	
1	IO_L37N_A6_M1A1_1	B22	RT	
1	IO_L38P_A5_M1CLK_1	J17	RT	
1	IO_L38N_A4_M1CLKN_1	J19	RT	
1	IO_L39P_M1A3_1	J20	RT	
1	IO_L39N_M1ODT_1	J22	RT	
1	IO_L40P_GCLK11_M1A5_1	M17	RT	
1	IO_L40N_GCLK10_M1A6_1	L17	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	M18	RT	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L41N_GCLK8_M1CASN_1	M19	RT	
1	IO_L42P_GCLK7_M1UDM_1	L19	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	K20	RB	
1	IO_L43P_GCLK5_M1DQ4_1	L20	RB	
1	IO_L43N_GCLK4_M1DQ5_1	L22	RB	
1	IO_L44P_A3_M1DQ6_1	K21	RB	
1	IO_L44N_A2_M1DQ7_1	K22	RB	
1	IO_L45P_A1_M1LDQS_1	M21	RB	
1	IO_L45N_A0_M1LDQSN_1	M22	RB	
1	IO_L46P_FCS_B_M1DQ2_1	N19	RB	
1	IO_L46N_FOE_B_M1DQ3_1	M20	RB	
1	IO_L47P_FWE_B_M1DQ0_1	N20	RB	
1	IO_L47N_LDC_M1DQ1_1	N22	RB	
1	IO_L48P_HDC_M1DQ8_1	P21	RB	
1	IO_L48N_M1DQ9_1	P22	RB	
1	IO_L49P_M1DQ10_1	R20	RB	
1	IO_L49N_M1DQ11_1	R22	RB	
1	IO_L50P_M1UDQS_1	T21	RB	
1	IO_L50N_M1UDQSN_1	T22	RB	
1	IO_L51P_M1DQ12_1	U20	RB	
1	IO_L51N_M1DQ13_1	U22	RB	
1	IO_L52P_M1DQ14_1	V21	RB	
1	IO_L52N_M1DQ15_1	V22	RB	
1	IO_L53P_1	AA21	RB	
1	IO_L53N_VREF_1	AA22	RB	
1	IO_L58P_1	R12	RB	
1	IO_L58N_1	R13	RB	
1	IO_L59P_1	W20	RB	
1	IO_L59N_1	W22	RB	
1	IO_L60P_1	T12	RB	
1	IO_L60N_1	T13	RB	
1	IO_L61P_1	AA20	RB	
1	IO_L61N_1	AB21	RB	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L62P_1	P15	RB	
1	IO_L62N_1	P16	RB	
1	IO_L63P_1	Y21	RB	
1	IO_L63N_1	Y22	RB	
1	IO_L64P_1	P19	RB	
1	IO_L64N_1	P20	RB	
1	IO_L65P_1	AB19	RB	
1	IO_L65N_1	AB20	RB	
1	IO_L66P_1	P17	RB	
1	IO_L66N_1	P18	RB	
1	IO_L67P_1	Y19	RB	
1	IO_L67N_1	Y20	RB	
1	IO_L68P_1	T15	RB	
1	IO_L68N_1	R16	RB	
1	IO_L70P_1	R17	RB	
1	IO_L70N_1	R19	RB	
1	IO_L71P_1	V19	RB	
1	IO_L71N_1	V20	RB	
1	IO_L72P_1	T17	RB	
1	IO_L72N_1	T18	RB	
1	IO_L73P_1	V17	RB	
1	IO_L73N_1	V18	RB	
1	IO_L74P_AWAKE_1	T19	RB	
1	IO_L74N_DOUT_BUSY_1	T20	RB	
NA	VFS	U19	NA	LX45T
NA	RFUSE	T16	NA	LX45T
NA	VBATT	R14	NA	LX45T
NA	SUSPEND	W18	NA	
2	CMPCS_B_2	U12	NA	
2	DONE_2	U16	NA	
2	IO_L1P_CCLK_2	W17	BR	
2	IO_L1N_M0_CPMISO_2	Y18	BR	
2	IO_L2P_CMPCLK_2	AA18	BR	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L2N_CMPMOSI_2	AB18	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	Y17	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AB17	BR	
2	IO_L4P_2	AA16	BR	
2	IO_L4N_VREF_2	AB16	BR	
2	IO_L5P_2	Y15	BR	
2	IO_L5N_2	AB15	BR	
2	IO_L12P_D1_MISO2_2	V13	BR	
2	IO_L12N_D2_MISO3_2	W13	BR	
2	IO_L13P_M1_2	U15	BR	
2	IO_L13N_D10_2	V15	BR	
2	IO_L14P_D11_2	W15	BR	
2	IO_L14N_D12_2	Y16	BR	
2	IO_L15P_2	AA14	BR	
2	IO_L15N_2	AB14	BR	
2	IO_L16P_2	W14	BR	
2	IO_L16N_VREF_2	Y14	BR	
2	IO_L20P_2	T14	BR	
2	IO_L20N_2	U13	BR	
2	IO_L29P_GCLK3_2	W11	BR	
2	IO_L29N_GCLK2_2	Y10	BR	
2	IO_L30P_GCLK1_D13_2	AA12	BR	
2	IO_L30N_GCLK0_USERCLK_2	AB12	BR	
2	IO_L31P_GCLK31_D14_2	Y11	BL	
2	IO_L31N_GCLK30_D15_2	AB11	BL	
2	IO_L32P_GCLK29_2	AA10	BL	
2	IO_L32N_GCLK28_2	AB10	BL	
2	IO_L41P_2	Y13	BL	
2	IO_L41N_VREF_2	AB13	BL	
2	IO_L42P_2	W12	BL	
2	IO_L42N_2	Y12	BL	
2	IO_L43P_2	W9	BL	
2	IO_L43N_2	Y8	BL	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L44P_2	V9	BL	LX75T
2	IO_L44N_2	W10	BL	LX75T
2	IO_L48P_D7_2	Y9	BL	
2	IO_L48N_RDWR_B_VREF_2	AB9	BL	
2	IO_L49P_D3_2	AA8	BL	
2	IO_L49N_D4_2	AB8	BL	
2	IO_L50P_2	V7	BL	LX75T
2	IO_L50N_2	W8	BL	LX75T
2	IO_L62P_D5_2	W6	BL	
2	IO_L62N_D6_2	Y6	BL	
2	IO_L63P_2	Y7	BL	
2	IO_L63N_2	AB7	BL	
2	IO_L64P_D8_2	AA6	BL	
2	IO_L64N_D9_2	AB6	BL	
2	IO_L65P_INIT_B_2	Y5	BL	
2	IO_L65N_CSO_B_2	AB5	BL	
2	PROGRAM_B_2	AA1	NA	
3	IO_L1P_3	AA2	LB	
3	IO_L1N_VREF_3	AB2	LB	
3	IO_L2P_3	Y2	LB	
3	IO_L2N_3	Y1	LB	
3	IO_L7P_3	U4	LB	
3	IO_L7N_3	V3	LB	
3	IO_L8P_3	Y3	LB	
3	IO_L8N_3	AB3	LB	
3	IO_L9P_3	W3	LB	
3	IO_L9N_3	W1	LB	
3	IO_L10P_3	W4	LB	
3	IO_L10N_3	Y4	LB	
3	IO_L11P_3	V11	LB	
3	IO_L11N_3	U10	LB	
3	IO_L12P_3	AA4	LB	
3	IO_L12N_3	AB4	LB	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L13P_3	U6	LB	
3	IO_L13N_3	V5	LB	
3	IO_L20P_3	T6	LB	
3	IO_L20N_3	T5	LB	
3	IO_L21P_3	P4	LB	
3	IO_L21N_3	R4	LB	
3	IO_L22P_3	T7	LB	
3	IO_L22N_3	R6	LB	
3	IO_L23P_3	P6	LB	
3	IO_L23N_3	P5	LB	
3	IO_L24P_3	U9	LB	
3	IO_L24N_3	U8	LB	
3	IO_L25P_3	R9	LB	
3	IO_L25N_3	T8	LB	
3	IO_L26P_3	T4	LB	
3	IO_L26N_3	T3	LB	
3	IO_L31P_3	T11	LB	
3	IO_L31N_VREF_3	T10	LB	
3	IO_L32P_M3DQ14_3	V2	LB	
3	IO_L32N_M3DQ15_3	V1	LB	
3	IO_L33P_M3DQ12_3	U3	LB	
3	IO_L33N_M3DQ13_3	U1	LB	
3	IO_L34P_M3UDQS_3	T2	LB	
3	IO_L34N_M3UDQSN_3	T1	LB	
3	IO_L35P_M3DQ10_3	R3	LB	
3	IO_L35N_M3DQ11_3	R1	LB	
3	IO_L36P_M3DQ8_3	P2	LB	
3	IO_L36N_M3DQ9_3	P1	LB	
3	IO_L37P_M3DQ0_3	N3	LB	
3	IO_L37N_M3DQ1_3	N1	LB	
3	IO_L38P_M3DQ2_3	M2	LB	
3	IO_L38N_M3DQ3_3	M1	LB	
3	IO_L39P_M3LDQS_3	L3	LB	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L39N_M3LDQSN_3	L1	LB	
3	IO_L40P_M3DQ6_3	K2	LB	
3	IO_L40N_M3DQ7_3	K1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	J3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	J1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	H2	LB	
3	IO_L42N_GCLK24_M3LDM_3	H1	LB	
3	IO_L43P_GCLK23_M3RASN_3	N4	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P3	LT	
3	IO_L44P_GCLK21_M3A5_3	G3	LT	
3	IO_L44N_GCLK20_M3A6_3	G1	LT	
3	IO_L45P_M3A3_3	M4	LT	
3	IO_L45N_M3ODT_3	M3	LT	
3	IO_L46P_M3CLK_3	F2	LT	
3	IO_L46N_M3CLKN_3	F1	LT	
3	IO_L47P_M3A0_3	M5	LT	
3	IO_L47N_M3A1_3	L4	LT	
3	IO_L48P_M3BA0_3	E3	LT	
3	IO_L48N_M3BA1_3	E1	LT	
3	IO_L49P_M3A7_3	K4	LT	
3	IO_L49N_M3A2_3	K3	LT	
3	IO_L50P_M3WE_3	D2	LT	
3	IO_L50N_M3BA2_3	D1	LT	
3	IO_L51P_M3A10_3	N6	LT	
3	IO_L51N_M3A4_3	M6	LT	
3	IO_L52P_M3A8_3	C3	LT	
3	IO_L52N_M3A9_3	C1	LT	
3	IO_L53P_M3CKE_3	K5	LT	
3	IO_L53N_M3A12_3	J4	LT	
3	IO_L54P_M3RESET_3	B2	LT	
3	IO_L54N_M3A11_3	B1	LT	
3	IO_L55P_M3A13_3	L6	LT	
3	IO_L55N_M3A14_3	K6	LT	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L57P_3	P7	LT	
3	IO_L57N_VREF_3	N7	LT	
3	IO_L58P_3	M8	LT	
3	IO_L58N_3	M7	LT	
3	IO_L59P_3	R8	LT	
3	IO_L59N_3	P8	LT	
3	IO_L60P_3	K8	LT	
3	IO_L60N_3	K7	LT	
3	IO_L69P_3	A3	LT	
3	IO_L69N_3	A2	LT	
3	IO_L70P_3	J7	LT	
3	IO_L70N_3	J6	LT	
3	IO_L71P_3	F5	LT	
3	IO_L71N_3	F3	LT	
3	IO_L72P_3	H6	LT	
3	IO_L72N_3	H5	LT	
3	IO_L73P_3	G6	LT	
3	IO_L73N_3	G4	LT	
3	IO_L74P_3	H4	LT	
3	IO_L74N_3	H3	LT	
3	IO_L75P_3	D4	LT	
3	IO_L75N_3	C4	LT	
3	IO_L83P_3	E4	LT	
3	IO_L83N_VREF_3	D3	LT	
101	MGTTXN0_101	A6	NA	
101	MGTTXP0_101	B6	NA	
101	MGTAVCCPLL0_101	B9	NA	
101	MGTREFCLK0N_101	A10	NA	
101	MGTREFCLK0P_101	B10	NA	
101	MGTRXN0_101	C7	NA	
101	MGTRXP0_101	D7	NA	
101	MGTRREF_101	E9	NA	
101	MGTRXN1_101	C9	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
101	MGTAVTTRCAL_101	E11	NA	
101	MGTRXP1_101	D9	NA	
101	MGTAVCCPLL1_101	D12	NA	
101	MGTREFCLK1N_101	C11	NA	
101	MGTREFCLK1P_101	D11	NA	
101	MGTTXN1_101	A8	NA	
101	MGTTXP1_101	B8	NA	
123	MGTTXN0_123	A14	NA	
123	MGTTXP0_123	B14	NA	
123	MGTAVCCPLL0_123	B13	NA	
123	MGTREFCLK0N_123	A12	NA	
123	MGTREFCLK0P_123	B12	NA	
123	MGTRXN0_123	C13	NA	
123	MGTRXP0_123	D13	NA	
123	MGTRXN1_123	C15	NA	
123	MGTRXP1_123	D15	NA	
123	MGTAVCCPLL1_123	E13	NA	
123	MGTREFCLK1N_123	E14	NA	
123	MGTREFCLK1P_123	F14	NA	
123	MGTTXN1_123	A16	NA	
123	MGTTXP1_123	B16	NA	
NA	GND	A1	NA	
NA	GND	A11	NA	
NA	GND	A13	NA	
NA	GND	A22	NA	
NA	GND	A9	NA	
NA	GND	AA13	NA	
NA	GND	AA17	NA	
NA	GND	AA5	NA	
NA	GND	AA9	NA	
NA	GND	AB1	NA	
NA	GND	AB22	NA	
NA	GND	B11	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	B15	NA	
NA	GND	B17	NA	
NA	GND	B5	NA	
NA	GND	B7	NA	
NA	GND	C12	NA	
NA	GND	C14	NA	
NA	GND	C16	NA	
NA	GND	C6	NA	
NA	GND	C8	NA	
NA	GND	D10	NA	
NA	GND	E12	NA	
NA	GND	E2	NA	
NA	GND	E21	NA	
NA	GND	E7	NA	
NA	GND	F13	NA	
NA	GND	F15	NA	
NA	GND	G14	NA	
NA	GND	G18	NA	
NA	GND	G5	NA	
NA	GND	H7	NA	
NA	GND	J11	NA	
NA	GND	J13	NA	
NA	GND	J15	NA	
NA	GND	J2	NA	
NA	GND	J21	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K12	NA	
NA	GND	K14	NA	
NA	GND	L13	NA	
NA	GND	L18	NA	
NA	GND	L5	NA	
NA	GND	L9	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	M10	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	
NA	GND	N11	NA	
NA	GND	N17	NA	
NA	GND	N2	NA	
NA	GND	N21	NA	
NA	GND	N9	NA	
NA	GND	P10	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	
NA	GND	R18	NA	
NA	GND	R5	NA	
NA	GND	U2	NA	
NA	GND	U21	NA	
NA	GND	U7	NA	
NA	GND	V10	NA	
NA	GND	V14	NA	
NA	GND	V16	NA	
NA	GND	V4	NA	
NA	GND	W19	NA	
NA	GND	W7	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J12	NA	
NA	VCCINT	J14	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K13	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L11	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M9	NA	
NA	VCCINT	N10	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N13	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	P9	NA	
NA	VCCAUX	D16	NA	
NA	VCCAUX	D6	NA	
NA	VCCAUX	F18	NA	
NA	VCCAUX	H15	NA	
NA	VCCAUX	H9	NA	
NA	VCCAUX	K15	NA	
NA	VCCAUX	L8	NA	
NA	VCCAUX	M15	NA	
NA	VCCAUX	N8	NA	
NA	VCCAUX	R10	NA	
NA	VCCAUX	R11	NA	
NA	VCCAUX	U11	NA	
NA	VCCAUX	U17	NA	
NA	VCCAUX	V6	NA	
0	VCCO_0	B19	NA	
0	VCCO_0	B4	NA	
0	VCCO_0	E10	NA	
0	VCCO_0	E17	NA	
0	VCCO_0	F6	NA	
0	VCCO_0	G13	NA	
0	VCCO_0	H8	NA	
1	VCCO_1	AA19	NA	
1	VCCO_1	C21	NA	
1	VCCO_1	E19	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	VCCO_1	G21	NA	
1	VCCO_1	J18	NA	
1	VCCO_1	L16	NA	
1	VCCO_1	L21	NA	
1	VCCO_1	N18	NA	
1	VCCO_1	R15	NA	
1	VCCO_1	R21	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	W21	NA	
2	VCCO_2	AA11	NA	
2	VCCO_2	AA15	NA	
2	VCCO_2	AA7	NA	
2	VCCO_2	U14	NA	
2	VCCO_2	V12	NA	
2	VCCO_2	V8	NA	
2	VCCO_2	W16	NA	
2	VCCO_2	W5	NA	
3	VCCO_3	AA3	NA	
3	VCCO_3	C2	NA	
3	VCCO_3	F4	NA	
3	VCCO_3	G2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	L2	NA	
3	VCCO_3	L7	NA	
3	VCCO_3	N5	NA	
3	VCCO_3	R2	NA	
3	VCCO_3	R7	NA	
3	VCCO_3	T9	NA	
3	VCCO_3	U5	NA	
3	VCCO_3	W2	NA	
101	MGTAVCC_101	C10	NA	
123	MGTAVCC_123	E15	NA	
101	MGTAVTTRX_101	D8	NA	

Table 2-12: CS(G)484 Package—LX45T, LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
123	MGTAVTTRX_123	D14	NA	
101	MGTAVTTTX_101	A7	NA	
123	MGTAVTTTX_123	A15	NA	

FG(G)676 Package—LX45

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-13: FG(G)676 Package—LX45

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B4	TL	
0	IO_L2N_0	A4	TL	
0	IO_L4P_0	C5	TL	
0	IO_L4N_0	A5	TL	
0	IO_L6P_0	B6	TL	
0	IO_L6N_0	A6	TL	
0	IO_L12P_0	C7	TL	
0	IO_L12N_0	A7	TL	
0	IO_L16P_0	B8	TL	
0	IO_L16N_0	A8	TL	
0	IO_L17P_0	C9	TL	
0	IO_L17N_0	A9	TL	
0	IO_L8P_0	D6	TL	
0	IO_L8N_VREF_0	C6	TL	
0	IO_L24P_0	C11	TL	
0	IO_L24N_0	A11	TL	
0	IO_L26P_0	B12	TL	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L26N_0	A12	TL	
0	IO_L34P_GCLK19_0	C13	TL	
0	IO_L34N_GCLK18_0	A13	TL	
0	IO_L35P_GCLK17_0	B14	TL	
0	IO_L35N_GCLK16_0	A14	TL	
0	IO_L36P_GCLK15_0	D14	TR	
0	IO_L36N_GCLK14_0	C14	TR	
0	IO_L37P_GCLK13_0	C15	TR	
0	IO_L37N_GCLK12_0	A15	TR	
0	IO_L38P_0	B16	TR	
0	IO_L38N_VREF_0	A16	TR	
0	IO_L50P_0	C17	TR	
0	IO_L50N_0	A17	TR	
0	IO_L52P_0	D18	TR	
0	IO_L52N_0	C18	TR	
0	IO_L56P_0	D21	TR	
0	IO_L56N_0	C20	TR	
0	IO_L62P_0	B18	TR	
0	IO_L62N_VREF_0	A18	TR	
0	IO_L63P_SCP7_0	C19	TR	
0	IO_L63N_SCP6_0	A19	TR	
0	IO_L64P_SCP5_0	B20	TR	
0	IO_L64N_SCP4_0	A20	TR	
0	IO_L65P_SCP3_0	C21	TR	
0	IO_L65N_SCP2_0	A21	TR	
0	IO_L66P_SCP1_0	B22	TR	
0	IO_L66N_SCP0_0	A22	TR	
NA	TCK	E21	NA	
NA	TDI	F20	NA	
NA	TMS	C23	NA	
NA	TDO	A24	NA	
1	IO_L1P_A25_1	B23	RT	
1	IO_L1N_A24_VREF_1	A23	RT	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L10P_1	B24	RT	
1	IO_L10N_1	A25	RT	
1	IO_L11P_1	C25	RT	
1	IO_L11N_1	C26	RT	
1	IO_L12P_1	B25	RT	
1	IO_L12N_1	B26	RT	
1	IO_L16P_1	E25	RT	
1	IO_L16N_1	E26	RT	
1	IO_L17P_1	D24	RT	
1	IO_L17N_1	D26	RT	
1	IO_L18P_1	F24	RT	
1	IO_L18N_1	F26	RT	
1	IO_L19P_1	H24	RT	
1	IO_L19N_1	H26	RT	
1	IO_L20P_1	G25	RT	
1	IO_L20N_1	G26	RT	
1	IO_L21P_1	K24	RT	
1	IO_L21N_1	K26	RT	
1	IO_L22P_1	J25	RT	
1	IO_L22N_1	J26	RT	
1	IO_L23P_1	M24	RT	
1	IO_L23N_1	M26	RT	
1	IO_L24P_1	L25	RT	
1	IO_L24N_1	L26	RT	
1	IO_L25P_1	N25	RT	
1	IO_L25N_1	N26	RT	
1	IO_L28P_1	L19	RT	
1	IO_L28N_VREF_1	K19	RT	
1	IO_L29P_A23_M1A13_1	L23	RT	
1	IO_L29N_A22_M1A14_1	L24	RT	
1	IO_L30P_A21_M1RESET_1	P20	RT	
1	IO_L30N_A20_M1A11_1	N21	RT	
1	IO_L31P_A19_M1CKE_1	M23	RT	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L31N_A18_M1A12_1	N24	RT	
1	IO_L32P_A17_M1A8_1	L17	RT	
1	IO_L32N_A16_M1A9_1	K18	RT	
1	IO_L33P_A15_M1A10_1	P24	RT	
1	IO_L33N_A14_M1A4_1	P26	RT	
1	IO_L34P_A13_M1WE_1	M19	RT	
1	IO_L34N_A12_M1BA2_1	L18	RT	
1	IO_L35P_A11_M1A7_1	R25	RT	
1	IO_L35N_A10_M1A2_1	R26	RT	
1	IO_L36P_A9_M1BA0_1	M18	RT	
1	IO_L36N_A8_M1BA1_1	N19	RT	
1	IO_L37P_A7_M1A0_1	N22	RT	
1	IO_L37N_A6_M1A1_1	N23	RT	
1	IO_L38P_A5_M1CLK_1	N17	RT	
1	IO_L38N_A4_M1CLKN_1	N18	RT	
1	IO_L39P_M1A3_1	R23	RT	
1	IO_L39N_M1ODT_1	R24	RT	
1	IO_L40P_GCLK11_M1A5_1	N20	RT	
1	IO_L40N_GCLK10_M1A6_1	M21	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	P21	RT	
1	IO_L41N_GCLK8_M1CASN_1	P22	RT	
1	IO_L42P_GCLK7_M1UDM_1	V23	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	RB	
1	IO_L43P_GCLK5_M1DQ4_1	U25	RB	
1	IO_L43N_GCLK4_M1DQ5_1	U26	RB	
1	IO_L44P_A3_M1DQ6_1	W25	RB	
1	IO_L44N_A2_M1DQ7_1	W26	RB	
1	IO_L45P_A1_M1LDQS_1	V24	RB	
1	IO_L45N_A0_M1LDQSN_1	V26	RB	
1	IO_L46P_FCS_B_M1DQ2_1	T24	RB	
1	IO_L46N_FOE_B_M1DQ3_1	T26	RB	
1	IO_L47P_FWE_B_M1DQ0_1	Y24	RB	
1	IO_L47N_LDC_M1DQ1_1	Y26	RB	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L48P_HDC_M1DQ8_1	AD24	RB	
1	IO_L48N_M1DQ9_1	AD26	RB	
1	IO_L49P_M1DQ10_1	AB24	RB	
1	IO_L49N_M1DQ11_1	AB26	RB	
1	IO_L50P_M1UDQS_1	AC25	RB	
1	IO_L50N_M1UDQSN_1	AC26	RB	
1	IO_L51P_M1DQ12_1	AA25	RB	
1	IO_L51N_M1DQ13_1	AA26	RB	
1	IO_L52P_M1DQ14_1	AE25	RB	
1	IO_L52N_M1DQ15_1	AE26	RB	
1	IO_L53P_1	T23	RB	
1	IO_L53N_VREF_1	U24	RB	
1	IO_L57P_1	R20	RB	
1	IO_L57N_1	R19	RB	
1	IO_L59P_1	T22	RB	
1	IO_L59N_1	U23	RB	
1	IO_L60P_1	T18	RB	
1	IO_L60N_1	T19	RB	
1	IO_L61P_1	U21	RB	
1	IO_L61N_1	U22	RB	
1	IO_L63P_1	AA23	RB	
1	IO_L63N_1	AA24	RB	
1	IO_L64P_1	T20	RB	
1	IO_L64N_1	U20	RB	
1	IO_L65P_1	AC23	RB	
1	IO_L65N_1	AC24	RB	
1	IO_L66P_1	V18	RB	
1	IO_L66N_1	V19	RB	
1	IO_L67P_1	AE24	RB	
1	IO_L67N_1	AF25	RB	
1	IO_L68P_1	W18	RB	
1	IO_L68N_1	W19	RB	
1	IO_L62P_1	U17	RB	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L62N_1	V17	RB	
1	IO_L70P_1	U19	RB	
1	IO_L70N_1	V20	RB	
1	IO_L71P_1	V22	RB	
1	IO_L71N_1	W22	RB	
1	IO_L72P_1	Y20	RB	
1	IO_L72N_1	Y21	RB	
1	IO_L73P_1	Y22	RB	
1	IO_L73N_1	AA22	RB	
1	IO_L74P_AWAKE_1	AE23	RB	
1	IO_L74N_DOUT_BUSY_1	AF24	RB	
NA	SUSPEND	AD23	NA	
2	CMPCS_B_2	AC22	NA	
2	DONE_2	AF23	NA	
2	IO_L1P_CCLK_2	AD22	BR	
2	IO_L1N_M0_CMPMISO_2	AF22	BR	
2	IO_L2P_CMPCLK_2	AE21	BR	
2	IO_L2N_CMPMOSI_2	AF21	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD20	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF20	BR	
2	IO_L4P_2	AE19	BR	
2	IO_L4N_VREF_2	AF19	BR	
2	IO_L5P_2	AC20	BR	
2	IO_L5N_2	AD21	BR	
2	IO_L6P_2	Y18	BR	
2	IO_L6N_2	AA19	BR	
2	IO_L7P_2	AC19	BR	
2	IO_L7N_2	AD19	BR	
2	IO_L8P_2	V16	BR	
2	IO_L8N_2	W17	BR	
2	IO_L9P_2	AD18	BR	
2	IO_L9N_2	AF18	BR	
2	IO_L10P_2	Y16	BR	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L10N_2	AA17	BR	
2	IO_L11P_2	AA18	BR	
2	IO_L11N_2	AB18	BR	
2	IO_L12P_D1_MISO2_2	AE17	BR	
2	IO_L12N_D2_MISO3_2	AF17	BR	
2	IO_L13P_M1_2	AD16	BR	
2	IO_L13N_D10_2	AF16	BR	
2	IO_L14P_D11_2	AE15	BR	
2	IO_L14N_D12_2	AF15	BR	
2	IO_L15P_2	AB17	BR	
2	IO_L15N_2	AC17	BR	
2	IO_L16P_2	AC15	BR	
2	IO_L16N_VREF_2	AD15	BR	
2	IO_L17P_2	AC16	BR	
2	IO_L17N_2	AD17	BR	
2	IO_L18P_2	V15	BR	
2	IO_L18N_2	W16	BR	
2	IO_L19P_2	AB15	BR	
2	IO_L19N_2	AC14	BR	
2	IO_L20P_2	Y15	BR	
2	IO_L20N_2	AA15	BR	
2	IO_L28P_2	Y14	BR	
2	IO_L28N_2	AA14	BR	
2	IO_L29P_GCLK3_2	AD14	BR	
2	IO_L29N_GCLK2_2	AF14	BR	
2	IO_L30P_GCLK1_D13_2	AE13	BR	
2	IO_L30N_GCLK0_USERCCLK_2	AF13	BR	
2	IO_L31P_GCLK31_D14_2	AC13	BL	
2	IO_L31N_GCLK30_D15_2	AD13	BL	
2	IO_L32P_GCLK29_2	AD12	BL	
2	IO_L32N_GCLK28_2	AF12	BL	
2	IO_L34P_2	AA13	BL	
2	IO_L34N_2	AB13	BL	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L41P_2	AA12	BL	
2	IO_L41N_VREF_2	AC12	BL	
2	IO_L42P_2	U15	BL	
2	IO_L42N_2	V14	BL	
2	IO_L43P_2	AA11	BL	
2	IO_L43N_2	AB11	BL	
2	IO_L44P_2	V13	BL	
2	IO_L44N_2	W14	BL	
2	IO_L45P_2	AC11	BL	
2	IO_L45N_2	AD11	BL	
2	IO_L46P_2	V12	BL	
2	IO_L46N_2	W12	BL	
2	IO_L47P_2	AE11	BL	
2	IO_L47N_2	AF11	BL	
2	IO_L48P_D7_2	AE9	BL	
2	IO_L48N_RDWR_B_VREF_2	AF9	BL	
2	IO_L49P_D3_2	AD10	BL	
2	IO_L49N_D4_2	AF10	BL	
2	IO_L50P_2	U13	BL	
2	IO_L50N_2	U12	BL	
2	IO_L51P_2	Y10	BL	
2	IO_L51N_2	AB10	BL	
2	IO_L52P_2	V11	BL	
2	IO_L52N_2	W11	BL	
2	IO_L58P_2	AC9	BL	
2	IO_L58N_2	AD9	BL	
2	IO_L53P_2	AD8	BL	
2	IO_L53N_2	AF8	BL	
2	IO_L62P_D5_2	AE7	BL	
2	IO_L62N_D6_2	AF7	BL	
2	IO_L63P_2	AD6	BL	
2	IO_L63N_2	AF6	BL	
2	IO_L64P_D8_2	AE5	BL	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L64N_D9_2	AF5	BL	
2	IO_L65P_INIT_B_2	AE4	BL	
2	IO_L65N_CSO_B_2	AF4	BL	
2	PROGRAM_B_2	AF3	NA	
3	IO_L1P_3	AC7	LB	
3	IO_L1N_VREF_3	AD7	LB	
3	IO_L2P_3	AE3	LB	
3	IO_L2N_3	AF2	LB	
3	IO_L3P_3	AC4	LB	
3	IO_L3N_3	AD4	LB	
3	IO_L7P_3	AA7	LB	
3	IO_L7N_3	Y6	LB	
3	IO_L8P_3	AB7	LB	
3	IO_L8N_3	AB6	LB	
3	IO_L10P_3	AC5	LB	
3	IO_L10N_3	AD5	LB	
3	IO_L16P_3	AA5	LB	
3	IO_L16N_3	AB5	LB	
3	IO_L15P_3	W8	LB	
3	IO_L15N_3	W7	LB	
3	IO_L18P_3	AB4	LB	
3	IO_L18N_3	AC3	LB	
3	IO_L20P_3	AA4	LB	
3	IO_L20N_3	AA3	LB	
3	IO_L22P_3	W5	LB	
3	IO_L22N_3	Y5	LB	
3	IO_L23P_3	U8	LB	
3	IO_L23N_3	U7	LB	
3	IO_L24P_3	U5	LB	
3	IO_L24N_3	V5	LB	
3	IO_L28P_3	U4	LB	
3	IO_L28N_3	U3	LB	
3	IO_L29P_3	T8	LB	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L29N_3	T6	LB	
3	IO_L30P_3	R5	LB	
3	IO_L30N_3	T4	LB	
3	IO_L31P_3	R7	LB	
3	IO_L31N_VREF_3	R6	LB	
3	IO_L32P_M3DQ14_3	AB3	LB	
3	IO_L32N_M3DQ15_3	AB1	LB	
3	IO_L33P_M3DQ12_3	AD3	LB	
3	IO_L33N_M3DQ13_3	AD1	LB	
3	IO_L34P_M3UDQS_3	AC2	LB	
3	IO_L34N_M3UDQSN_3	AC1	LB	
3	IO_L35P_M3DQ10_3	AE2	LB	
3	IO_L35N_M3DQ11_3	AE1	LB	
3	IO_L36P_M3DQ8_3	AA2	LB	
3	IO_L36N_M3DQ9_3	AA1	LB	
3	IO_L37P_M3DQ0_3	Y3	LB	
3	IO_L37N_M3DQ1_3	Y1	LB	
3	IO_L38P_M3DQ2_3	W2	LB	
3	IO_L38N_M3DQ3_3	W1	LB	
3	IO_L39P_M3LDQS_3	V3	LB	
3	IO_L39N_M3LDQSN_3	V1	LB	
3	IO_L40P_M3DQ6_3	U2	LB	
3	IO_L40N_M3DQ7_3	U1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	T3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	T1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	LB	
3	IO_L42N_GCLK24_M3LDM_3	W3	LB	
3	IO_L43P_GCLK23_M3RASN_3	N8	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P8	LT	
3	IO_L44P_GCLK21_M3A5_3	R2	LT	
3	IO_L44N_GCLK20_M3A6_3	R1	LT	
3	IO_L45P_M3A3_3	P7	LT	
3	IO_L45N_M3ODT_3	P6	LT	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L46P_M3CLK_3	R4	LT	
3	IO_L46N_M3CLKN_3	R3	LT	
3	IO_L47P_M3A0_3	N7	LT	
3	IO_L47N_M3A1_3	N6	LT	
3	IO_L48P_M3BA0_3	P3	LT	
3	IO_L48N_M3BA1_3	P1	LT	
3	IO_L49P_M3A7_3	P10	LT	
3	IO_L49N_M3A2_3	R9	LT	
3	IO_L50P_M3WE_3	P5	LT	
3	IO_L50N_M3BA2_3	N5	LT	
3	IO_L51P_M3A10_3	M10	LT	
3	IO_L51N_M3A4_3	N9	LT	
3	IO_L52P_M3A8_3	N4	LT	
3	IO_L52N_M3A9_3	N3	LT	
3	IO_L53P_M3CKE_3	M9	LT	
3	IO_L53N_M3A12_3	M8	LT	
3	IO_L54P_M3RESET_3	L4	LT	
3	IO_L54N_M3A11_3	L3	LT	
3	IO_L55P_M3A13_3	M6	LT	
3	IO_L55N_M3A14_3	M4	LT	
3	IO_L57P_3	L7	LT	
3	IO_L57N_VREF_3	L6	LT	
3	IO_L59P_3	N2	LT	
3	IO_L59N_3	N1	LT	
3	IO_L60P_3	M3	LT	
3	IO_L60N_3	M1	LT	
3	IO_L61P_3	L2	LT	
3	IO_L61N_3	L1	LT	
3	IO_L62P_3	K3	LT	
3	IO_L62N_3	K1	LT	
3	IO_L63P_3	J2	LT	
3	IO_L63N_3	J1	LT	
3	IO_L64P_3	H3	LT	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L64N_3	H1	LT	
3	IO_L65P_3	G2	LT	
3	IO_L65N_3	G1	LT	
3	IO_L66P_3	F3	LT	
3	IO_L66N_3	F1	LT	
3	IO_L67P_3	E2	LT	
3	IO_L67N_3	E1	LT	
3	IO_L68P_3	D3	LT	
3	IO_L68N_3	D1	LT	
3	IO_L77P_3	E4	LT	
3	IO_L77N_3	E3	LT	
3	IO_L79P_3	C2	LT	
3	IO_L79N_3	C1	LT	
3	IO_L81P_3	B2	LT	
3	IO_L81N_3	B1	LT	
3	IO_L83P_3	C4	LT	
3	IO_L83N_VREF_3	C3	LT	
NA	GND	A1	NA	
NA	GND	A26	NA	
NA	GND	AB12	NA	
NA	GND	AB16	NA	
NA	GND	AB2	NA	
NA	GND	AB20	NA	
NA	GND	AB25	NA	
NA	GND	AC8	NA	
NA	GND	AE10	NA	
NA	GND	AE14	NA	
NA	GND	AE18	NA	
NA	GND	AE22	NA	
NA	GND	AE6	NA	
NA	GND	AF1	NA	
NA	GND	AF26	NA	
NA	GND	B13	NA	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	B17	NA	
NA	GND	B21	NA	
NA	GND	B5	NA	
NA	GND	B9	NA	
NA	GND	D4	NA	
NA	GND	E11	NA	
NA	GND	E15	NA	
NA	GND	E22	NA	
NA	GND	E7	NA	
NA	GND	F19	NA	
NA	GND	F2	NA	
NA	GND	F25	NA	
NA	GND	H11	NA	
NA	GND	H23	NA	
NA	GND	H4	NA	
NA	GND	J19	NA	
NA	GND	J8	NA	
NA	GND	K16	NA	
NA	GND	K2	NA	
NA	GND	K25	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	
NA	GND	L15	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	
NA	GND	M16	NA	
NA	GND	M22	NA	
NA	GND	M5	NA	
NA	GND	N11	NA	
NA	GND	N13	NA	
NA	GND	N15	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	P16	NA	
NA	GND	P19	NA	
NA	GND	P2	NA	
NA	GND	P25	NA	
NA	GND	R11	NA	
NA	GND	R13	NA	
NA	GND	R15	NA	
NA	GND	R8	NA	
NA	GND	T12	NA	
NA	GND	T14	NA	
NA	GND	T16	NA	
NA	GND	T21	NA	
NA	GND	T5	NA	
NA	GND	U11	NA	
NA	GND	V2	NA	
NA	GND	V25	NA	
NA	GND	W15	NA	
NA	GND	W20	NA	
NA	GND	Y11	NA	
NA	GND	Y23	NA	
NA	GND	Y4	NA	
NA	GND	Y7	NA	
NA	VCCAUX	AA10	NA	
NA	VCCAUX	AA16	NA	
NA	VCCAUX	AA21	NA	
NA	VCCAUX	AA6	NA	
NA	VCCAUX	F21	NA	
NA	VCCAUX	F6	NA	
NA	VCCAUX	G12	NA	
NA	VCCAUX	G15	NA	
NA	VCCAUX	J18	NA	
NA	VCCAUX	J9	NA	
NA	VCCAUX	K13	NA	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	L22	NA	
NA	VCCAUX	L5	NA	
NA	VCCAUX	M17	NA	
NA	VCCAUX	N10	NA	
NA	VCCAUX	U14	NA	
NA	VCCAUX	U6	NA	
NA	VCCAUX	V9	NA	
NA	VCCAUX	Y19	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K17	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	L16	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M15	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	N16	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	P15	NA	
NA	VCCINT	R12	NA	
NA	VCCINT	R14	NA	
NA	VCCINT	R16	NA	
NA	VCCINT	T11	NA	
NA	VCCINT	T13	NA	
NA	VCCINT	T15	NA	
NA	VCCINT	T17	NA	
NA	VCCINT	U10	NA	
NA	VCCINT	U16	NA	
0	VCCO_0	B11	NA	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	VCCO_0	B15	NA	
0	VCCO_0	B19	NA	
0	VCCO_0	B3	NA	
0	VCCO_0	B7	NA	
0	VCCO_0	C22	NA	
0	VCCO_0	D17	NA	
0	VCCO_0	D9	NA	
0	VCCO_0	E13	NA	
0	VCCO_0	G10	NA	
0	VCCO_0	G18	NA	
0	VCCO_0	H14	NA	
1	VCCO_1	AB23	NA	
1	VCCO_1	AD25	NA	
1	VCCO_1	M20	NA	
1	VCCO_1	P23	NA	
1	VCCO_1	T25	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	V21	NA	
1	VCCO_1	W23	NA	
1	VCCO_1	Y25	NA	
1	VCCO_1	D25	NA	
1	VCCO_1	F23	NA	
1	VCCO_1	H25	NA	
1	VCCO_1	J21	NA	
1	VCCO_1	K23	NA	
1	VCCO_1	M25	NA	
2	VCCO_2	AB14	NA	
2	VCCO_2	AC10	NA	
2	VCCO_2	AC18	NA	
2	VCCO_2	AC21	NA	
2	VCCO_2	AE12	NA	
2	VCCO_2	AE16	NA	
2	VCCO_2	AE20	NA	

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	VCCO_2	AE8	NA	
2	VCCO_2	Y12	NA	
2	VCCO_2	Y17	NA	
3	VCCO_3	AC6	NA	
3	VCCO_3	AD2	NA	
3	VCCO_3	M7	NA	
3	VCCO_3	P4	NA	
3	VCCO_3	P9	NA	
3	VCCO_3	T2	NA	
3	VCCO_3	T7	NA	
3	VCCO_3	W4	NA	
3	VCCO_3	W6	NA	
3	VCCO_3	Y2	NA	
3	VCCO_3	D2	NA	
3	VCCO_3	F4	NA	
3	VCCO_3	H2	NA	
3	VCCO_3	J6	NA	
3	VCCO_3	K4	NA	
3	VCCO_3	M2	NA	
NC	No connect	A10		LX45
NC	No connect	AA20		LX45
NC	No connect	AA8		LX45
NC	No connect	AB19		LX45
NC	No connect	AB8		LX45
NC	No connect	C10		LX45
NC	No connect	C12		LX45
NC	No connect	C16		LX45
NC	No connect	C24		LX45
NC	No connect	C8		LX45
NC	No connect	B10		LX45
NC	No connect	D10		LX45
NC	No connect	D11		LX45
NC	No connect	D12		LX45

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NC	No connect	D13		LX45
NC	No connect	D15		LX45
NC	No connect	D16		LX45
NC	No connect	D19		LX45
NC	No connect	D20		LX45
NC	No connect	D22		LX45
NC	No connect	D23		LX45
NC	No connect	D5		LX45
NC	No connect	D7		LX45
NC	No connect	D8		LX45
NC	No connect	E10		LX45
NC	No connect	E12		LX45
NC	No connect	E14		LX45
NC	No connect	E16		LX45
NC	No connect	E17		LX45
NC	No connect	E18		LX45
NC	No connect	E19		LX45
NC	No connect	E20		LX45
NC	No connect	E23		LX45
NC	No connect	E24		LX45
NC	No connect	E5		LX45
NC	No connect	E6		LX45
NC	No connect	E8		LX45
NC	No connect	E9		LX45
NC	No connect	F10		LX45
NC	No connect	F11		LX45
NC	No connect	F12		LX45
NC	No connect	F13		LX45
NC	No connect	F14		LX45
NC	No connect	F15		LX45
NC	No connect	F16		LX45
NC	No connect	F17		LX45
NC	No connect	F18		LX45

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NC	No connect	F22		LX45
NC	No connect	F5		LX45
NC	No connect	F7		LX45
NC	No connect	F8		LX45
NC	No connect	F9		LX45
NC	No connect	G11		LX45
NC	No connect	G13		LX45
NC	No connect	G14		LX45
NC	No connect	G16		LX45
NC	No connect	G17		LX45
NC	No connect	G19		LX45
NC	No connect	G20		LX45
NC	No connect	G21		LX45
NC	No connect	G22		LX45
NC	No connect	G23		LX45
NC	No connect	G24		LX45
NC	No connect	G3		LX45
NC	No connect	G4		LX45
NC	No connect	G5		LX45
NC	No connect	G6		LX45
NC	No connect	G7		LX45
NC	No connect	G8		LX45
NC	No connect	G9		LX45
NC	No connect	H10		LX45
NC	No connect	H12		LX45
NC	No connect	H13		LX45
NC	No connect	H15		LX45
NC	No connect	H16		LX45
NC	No connect	H17		LX45
NC	No connect	H18		LX45
NC	No connect	H19		LX45
NC	No connect	H20		LX45
NC	No connect	H21		LX45

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NC	No connect	H22		LX45
NC	No connect	H5		LX45
NC	No connect	H6		LX45
NC	No connect	H7		LX45
NC	No connect	H8		LX45
NC	No connect	H9		LX45
NC	No connect	J10		LX45
NC	No connect	J11		LX45
NC	No connect	J12		LX45
NC	No connect	J13		LX45
NC	No connect	J14		LX45
NC	No connect	J15		LX45
NC	No connect	J16		LX45
NC	No connect	J17		LX45
NC	No connect	J20		LX45
NC	No connect	J22		LX45
NC	No connect	J23		LX45
NC	No connect	J24		LX45
NC	No connect	J5		LX45
NC	No connect	J7		LX45
NC	No connect	K10		LX45
NC	No connect	K12		LX45
NC	No connect	K14		LX45
NC	No connect	K15		LX45
NC	No connect	K20		LX45
NC	No connect	K21		LX45
NC	No connect	K22		LX45
NC	No connect	K5		LX45
NC	No connect	K6		LX45
NC	No connect	K7		LX45
NC	No connect	K8		LX45
NC	No connect	K9		LX45
NC	No connect	L20		LX45

Table 2-13: FG(G)676 Package—LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NC	No connect	L21		LX45
NC	No connect	J3		LX45
NC	No connect	J4		LX45
NC	No connect	L8		LX45
NC	No connect	L9		LX45
NC	No connect	P17		LX45
NC	No connect	P18		LX45
NC	No connect	R10		LX45
NC	No connect	R17		LX45
NC	No connect	R18		LX45
NC	No connect	R21		LX45
NC	No connect	R22		LX45
NC	No connect	T10		LX45
NC	No connect	T9		LX45
NC	No connect	AA9		LX45
NC	No connect	AB9		LX45
NC	No connect	U9		LX45
NC	No connect	V10		LX45
NC	No connect	W10		LX45
NC	No connect	W13		LX45
NC	No connect	W21		LX45
NC	No connect	W9		LX45
NC	No connect	Y13		LX45
NC	No connect	Y8		LX45
NC	No connect	Y9		LX45
NC	No connect	V6		LX45
NC	No connect	V7		LX45
NC	No connect	V8		LX45
NC	No connect	AB21		LX45
NC	No connect	AB22		LX45

FG(G)676 Package—LX75, LX100, and LX150

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 and bank 5 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 and bank 4 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	A3	TL	
0	IO_L1N_VREF_0	A2	TL	
0	IO_L2P_0	B4	TL	
0	IO_L2N_0	A4	TL	
0	IO_L3P_0	E6	TL	LX75
0	IO_L3N_0	D5	TL	LX75
0	IO_L4P_0	C5	TL	
0	IO_L4N_0	A5	TL	
0	IO_L5P_0	G8	TL	
0	IO_L5N_0	F7	TL	
0	IO_L6P_0	B6	TL	
0	IO_L6N_0	A6	TL	
0	IO_L7P_0	G9	TL	LX75, LX100
0	IO_L7N_0	F8	TL	LX75, LX100
0	IO_L8P_0	D6	TL	
0	IO_L8N_VREF_0	C6	TL	
0	IO_L9P_0	K12	TL	LX75, LX100
0	IO_L9N_0	J11	TL	LX75, LX100
0	IO_L11P_0	H10	TL	LX75, LX100

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L11N_0	H9	TL	LX75, LX100
0	IO_L12P_0	C7	TL	
0	IO_L12N_0	A7	TL	
0	IO_L13P_0	E8	TL	LX75
0	IO_L13N_0	D7	TL	LX75
0	IO_L14P_0	D8	TL	LX75
0	IO_L14N_0	C8	TL	LX75
0	IO_L15P_0	F9	TL	LX75
0	IO_L15N_0	E9	TL	LX75
0	IO_L16P_0	B8	TL	
0	IO_L16N_0	A8	TL	
0	IO_L17P_0	C9	TL	
0	IO_L17N_0	A9	TL	
0	IO_L18P_0	E10	TL	LX75
0	IO_L18N_0	F10	TL	LX75
0	IO_L19P_0	D10	TL	LX75
0	IO_L19N_0	C10	TL	LX75
0	IO_L21P_0	J12	TL	LX75, LX100
0	IO_L21N_0	H13	TL	LX75, LX100
0	IO_L22P_0	B10	TL	
0	IO_L22N_0	A10	TL	
0	IO_L23P_0	D11	TL	LX75
0	IO_L23N_0	F11	TL	LX75
0	IO_L24P_0	C11	TL	
0	IO_L24N_0	A11	TL	
0	IO_L25P_0	H12	TL	LX75, LX100
0	IO_L25N_0	G11	TL	LX75, LX100
0	IO_L26P_0	B12	TL	
0	IO_L26N_0	A12	TL	
0	IO_L30P_0	F12	TL	LX75, LX100
0	IO_L30N_0	E12	TL	LX75, LX100
0	IO_L31P_0	D12	TL	LX75
0	IO_L31N_0	C12	TL	LX75

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L32P_0	G13	TL	LX75, LX100
0	IO_L32N_0	F14	TL	LX75, LX100
0	IO_L33P_0	F13	TL	LX75
0	IO_L33N_0	D13	TL	LX75
0	IO_L34P_GCLK19_0	C13	TL	
0	IO_L34N_GCLK18_0	A13	TL	
0	IO_L35P_GCLK17_0	B14	TL	
0	IO_L35N_GCLK16_0	A14	TL	
0	IO_L36P_GCLK15_0	D14	TR	
0	IO_L36N_GCLK14_0	C14	TR	
0	IO_L37P_GCLK13_0	C15	TR	
0	IO_L37N_GCLK12_0	A15	TR	
0	IO_L38P_0	B16	TR	
0	IO_L38N_VREF_0	A16	TR	
0	IO_L43P_0	J14	TR	LX75
0	IO_L43N_0	G14	TR	LX75
0	IO_L44P_0	E14	TR	LX75
0	IO_L44N_0	D15	TR	LX75
0	IO_L45P_0	J13	TR	LX75, LX100
0	IO_L45N_0	K14	TR	LX75, LX100
0	IO_L46P_0	D16	TR	LX75
0	IO_L46N_0	C16	TR	LX75
0	IO_L47P_0	G16	TR	LX75
0	IO_L47N_0	F15	TR	LX75
0	IO_L48P_0	F17	TR	
0	IO_L48N_0	E17	TR	
0	IO_L49P_0	F16	TR	
0	IO_L49N_0	E16	TR	
0	IO_L50P_0	C17	TR	
0	IO_L50N_0	A17	TR	
0	IO_L51P_0	J15	TR	
0	IO_L51N_0	H15	TR	
0	IO_L52P_0	D18	TR	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L52N_0	C18	TR	
0	IO_L53P_0	K15	TR	LX75, LX100
0	IO_L53N_0	J16	TR	LX75, LX100
0	IO_L54P_0	E19	TR	LX75
0	IO_L54N_0	D19	TR	LX75
0	IO_L55P_0	H16	TR	LX75
0	IO_L55N_0	G17	TR	LX75
0	IO_L56P_0	D21	TR	
0	IO_L56N_0	C20	TR	
0	IO_L57P_0	F18	TR	LX75
0	IO_L57N_0	E18	TR	LX75
0	IO_L58P_0	E20	TR	LX75
0	IO_L58N_0	D20	TR	LX75
0	IO_L59P_0	J17	TR	LX75
0	IO_L59N_0	H17	TR	LX75
0	IO_L62P_0	B18	TR	
0	IO_L62N_VREF_0	A18	TR	
0	IO_L63P_SCP7_0	C19	TR	
0	IO_L63N_SCP6_0	A19	TR	
0	IO_L64P_SCP5_0	B20	TR	
0	IO_L64N_SCP4_0	A20	TR	
0	IO_L65P_SCP3_0	C21	TR	
0	IO_L65N_SCP2_0	A21	TR	
0	IO_L66P_SCP1_0	B22	TR	
0	IO_L66N_SCP0_0	A22	TR	
NA	TCK	E21	NA	
NA	TDI	F20	NA	
NA	TMS	C23	NA	
NA	TDO	A24	NA	
5	IO_L1P_A25_5	B23	RT	
5	IO_L1N_A24_VREF_5	A23	RT	
5	IO_L2P_M5A13_5	G20	RT	
5	IO_L2N_M5A14_5	G21	RT	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L3P_M5RESET_5	D23	RT	
5	IO_L3N_M5A11_5	C24	RT	
5	IO_L4P_M5CKE_5	F22	RT	
5	IO_L4N_M5A12_5	D22	RT	
5	IO_L5P_M5A8_5	H20	RT	
5	IO_L5N_M5A9_5	H21	RT	
5	IO_L6P_M5A10_5	H22	RT	
5	IO_L6N_M5A4_5	G22	RT	
5	IO_L7P_M5WE_5	E23	RT	
5	IO_L7N_M5BA2_5	E24	RT	
5	IO_L8P_M5A7_5	G23	RT	
5	IO_L8N_M5A2_5	G24	RT	
5	IO_L9P_M5BA0_5	H18	RT	
5	IO_L9N_M5BA1_5	G19	RT	
5	IO_L10P_M5A0_5	B24	RT	
5	IO_L10N_M5A1_5	A25	RT	
5	IO_L11P_M5CLK_5	C25	RT	
5	IO_L11N_M5CLKN_5	C26	RT	
5	IO_L12P_M5A3_5	B25	RT	
5	IO_L12N_M5ODT_5	B26	RT	
5	IO_L13P_M5A5_5	K20	RT	
5	IO_L13N_M5A6_5	K21	RT	
5	IO_L14P_M5RASN_5	K22	RT	
5	IO_L14N_M5CASN_5	J22	RT	
5	IO_L15P_M5UDM_5	J23	RT	
5	IO_L15N_M5LDM_5	J24	RT	
5	IO_L16P_M5DQ4_5	E25	RT	
5	IO_L16N_M5DQ5_5	E26	RT	
5	IO_L17P_M5DQ6_5	D24	RT	
5	IO_L17N_M5DQ7_5	D26	RT	
5	IO_L18P_M5LDQS_5	F24	RT	
5	IO_L18N_M5LDQSN_5	F26	RT	
5	IO_L19P_M5DQ2_5	H24	RT	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L19N_M5DQ3_5	H26	RT	
5	IO_L20P_M5DQ0_5	G25	RT	
5	IO_L20N_M5DQ1_5	G26	RT	
5	IO_L21P_M5DQ8_5	K24	RT	
5	IO_L21N_M5DQ9_5	K26	RT	
5	IO_L22P_M5DQ10_5	J25	RT	
5	IO_L22N_M5DQ11_5	J26	RT	
5	IO_L23P_M5UDQS_5	M24	RT	
5	IO_L23N_M5UDQSN_5	M26	RT	
5	IO_L24P_M5DQ12_5	L25	RT	
5	IO_L24N_M5DQ13_5	L26	RT	
5	IO_L25P_M5DQ14_5	N25	RT	
5	IO_L25N_M5DQ15_5	N26	RT	
5	IO_L26P_5	L20	RT	
5	IO_L26N_VREF_5	L21	RT	
5	IO_L27P_5	H19	RT	
5	IO_L27N_5	J20	RT	
1	IO_L28P_1	L19	RT	
1	IO_L28N_VREF_1	K19	RT	
1	IO_L29P_A23_M1A13_1	L23	RT	
1	IO_L29N_A22_M1A14_1	L24	RT	
1	IO_L30P_A21_M1RESET_1	P20	RT	
1	IO_L30N_A20_M1A11_1	N21	RT	
1	IO_L31P_A19_M1CKE_1	M23	RT	
1	IO_L31N_A18_M1A12_1	N24	RT	
1	IO_L32P_A17_M1A8_1	L17	RT	
1	IO_L32N_A16_M1A9_1	K18	RT	
1	IO_L33P_A15_M1A10_1	P24	RT	
1	IO_L33N_A14_M1A4_1	P26	RT	
1	IO_L34P_A13_M1WE_1	M19	RT	
1	IO_L34N_A12_M1BA2_1	L18	RT	
1	IO_L35P_A11_M1A7_1	R25	RT	
1	IO_L35N_A10_M1A2_1	R26	RT	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L36P_A9_M1BA0_1	M18	RT	
1	IO_L36N_A8_M1BA1_1	N19	RT	
1	IO_L37P_A7_M1A0_1	N22	RT	
1	IO_L37N_A6_M1A1_1	N23	RT	
1	IO_L38P_A5_M1CLK_1	N17	RT	
1	IO_L38N_A4_M1CLKN_1	N18	RT	
1	IO_L39P_M1A3_1	R23	RT	
1	IO_L39N_M1ODT_1	R24	RT	
1	IO_L40P_GCLK11_M1A5_1	N20	RT	
1	IO_L40N_GCLK10_M1A6_1	M21	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	P21	RT	
1	IO_L41N_GCLK8_M1CASN_1	P22	RT	
1	IO_L42P_GCLK7_M1UDM_1	V23	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	RB	
1	IO_L43P_GCLK5_M1DQ4_1	U25	RB	
1	IO_L43N_GCLK4_M1DQ5_1	U26	RB	
1	IO_L44P_A3_M1DQ6_1	W25	RB	
1	IO_L44N_A2_M1DQ7_1	W26	RB	
1	IO_L45P_A1_M1LDQS_1	V24	RB	
1	IO_L45N_A0_M1LDQSN_1	V26	RB	
1	IO_L46P_FCS_B_M1DQ2_1	T24	RB	
1	IO_L46N_FOE_B_M1DQ3_1	T26	RB	
1	IO_L47P_FWE_B_M1DQ0_1	Y24	RB	
1	IO_L47N_LDC_M1DQ1_1	Y26	RB	
1	IO_L48P_HDC_M1DQ8_1	AD24	RB	
1	IO_L48N_M1DQ9_1	AD26	RB	
1	IO_L49P_M1DQ10_1	AB24	RB	
1	IO_L49N_M1DQ11_1	AB26	RB	
1	IO_L50P_M1UDQS_1	AC25	RB	
1	IO_L50N_M1UDQSN_1	AC26	RB	
1	IO_L51P_M1DQ12_1	AA25	RB	
1	IO_L51N_M1DQ13_1	AA26	RB	
1	IO_L52P_M1DQ14_1	AE25	RB	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L52N_M1DQ15_1	AE26	RB	
1	IO_L53P_1	T23	RB	
1	IO_L53N_VREF_1	U24	RB	
1	IO_L55P_1	R22	RB	
1	IO_L55N_1	R21	RB	
1	IO_L56P_1	P17	RB	
1	IO_L56N_1	P18	RB	
1	IO_L57P_1	R20	RB	
1	IO_L57N_1	R19	RB	
1	IO_L58P_1	R17	RB	
1	IO_L58N_1	R18	RB	
1	IO_L59P_1	T22	RB	
1	IO_L59N_1	U23	RB	
1	IO_L60P_1	T18	RB	
1	IO_L60N_1	T19	RB	
1	IO_L61P_1	U21	RB	
1	IO_L61N_1	U22	RB	
1	IO_L62P_1	U17	RB	
1	IO_L62N_1	V17	RB	
1	IO_L63P_1	AA23	RB	
1	IO_L63N_1	AA24	RB	
1	IO_L64P_1	T20	RB	
1	IO_L64N_1	U20	RB	
1	IO_L65P_1	AC23	RB	
1	IO_L65N_1	AC24	RB	
1	IO_L66P_1	V18	RB	
1	IO_L66N_1	V19	RB	
1	IO_L67P_1	AE24	RB	
1	IO_L67N_1	AF25	RB	
1	IO_L68P_1	W18	RB	
1	IO_L68N_1	W19	RB	
1	IO_L69P_1	AB21	RB	
1	IO_L69N_VREF_1	AB22	RB	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L70P_1	U19	RB	
1	IO_L70N_1	V20	RB	
1	IO_L71P_1	V22	RB	
1	IO_L71N_1	W22	RB	
1	IO_L72P_1	Y20	RB	
1	IO_L72N_1	Y21	RB	
1	IO_L73P_1	Y22	RB	
1	IO_L73N_1	AA22	RB	
1	IO_L74P_AWAKE_1	AE23	RB	
1	IO_L74N_DOUT_BUSY_1	AF24	RB	
NA	VFS	AB19	NA	
NA	RFUSE	AA20	NA	
NA	VBATT	W21	NA	
NA	SUSPEND	AD23	NA	
2	CMPCS_B_2	AC22	NA	
2	DONE_2	AF23	NA	
2	IO_L1P_CCLK_2	AD22	BR	
2	IO_L1N_M0_CPMISO_2	AF22	BR	
2	IO_L2P_CMPCLK_2	AE21	BR	
2	IO_L2N_CPMOSI_2	AF21	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD20	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF20	BR	
2	IO_L4P_2	AE19	BR	
2	IO_L4N_VREF_2	AF19	BR	
2	IO_L5P_2	AC20	BR	LX75
2	IO_L5N_2	AD21	BR	LX75
2	IO_L6P_2	Y18	BR	LX75
2	IO_L6N_2	AA19	BR	LX75
2	IO_L7P_2	AC19	BR	LX75
2	IO_L7N_2	AD19	BR	LX75
2	IO_L8P_2	V16	BR	LX75
2	IO_L8N_2	W17	BR	LX75
2	IO_L9P_2	AD18	BR	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L9N_2	AF18	BR	
2	IO_L10P_2	Y16	BR	LX75
2	IO_L10N_2	AA17	BR	LX75
2	IO_L11P_2	AA18	BR	LX75
2	IO_L11N_2	AB18	BR	LX75
2	IO_L12P_D1_MISO2_2	AE17	BR	
2	IO_L12N_D2_MISO3_2	AF17	BR	
2	IO_L13P_M1_2	AD16	BR	
2	IO_L13N_D10_2	AF16	BR	
2	IO_L14P_D11_2	AE15	BR	
2	IO_L14N_D12_2	AF15	BR	
2	IO_L15P_2	AB17	BR	
2	IO_L15N_2	AC17	BR	
2	IO_L16P_2	AC15	BR	
2	IO_L16N_VREF_2	AD15	BR	
2	IO_L17P_2	AC16	BR	LX75
2	IO_L17N_2	AD17	BR	LX75
2	IO_L18P_2	V15	BR	LX75
2	IO_L18N_2	W16	BR	LX75
2	IO_L19P_2	AB15	BR	
2	IO_L19N_2	AC14	BR	
2	IO_L20P_2	Y15	BR	
2	IO_L20N_2	AA15	BR	
2	IO_L28P_2	Y14	BR	LX75
2	IO_L28N_2	AA14	BR	LX75
2	IO_L29P_GCLK3_2	AD14	BR	
2	IO_L29N_GCLK2_2	AF14	BR	
2	IO_L30P_GCLK1_D13_2	AE13	BR	
2	IO_L30N_GCLK0_USERCLK_2	AF13	BR	
2	IO_L31P_GCLK31_D14_2	AC13	BL	
2	IO_L31N_GCLK30_D15_2	AD13	BL	
2	IO_L32P_GCLK29_2	AD12	BL	
2	IO_L32N_GCLK28_2	AF12	BL	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L33P_2	W13	BL	LX75
2	IO_L33N_2	Y13	BL	LX75
2	IO_L34P_2	AA13	BL	
2	IO_L34N_2	AB13	BL	
2	IO_L41P_2	AA12	BL	
2	IO_L41N_VREF_2	AC12	BL	
2	IO_L42P_2	U15	BL	LX75
2	IO_L42N_2	V14	BL	LX75
2	IO_L43P_2	AA11	BL	LX75
2	IO_L43N_2	AB11	BL	LX75
2	IO_L44P_2	V13	BL	LX75
2	IO_L44N_2	W14	BL	LX75
2	IO_L45P_2	AC11	BL	LX75
2	IO_L45N_2	AD11	BL	LX75
2	IO_L46P_2	V12	BL	
2	IO_L46N_2	W12	BL	
2	IO_L47P_2	AE11	BL	
2	IO_L47N_2	AF11	BL	
2	IO_L48P_D7_2	AE9	BL	
2	IO_L48N_RDWR_B_VREF_2	AF9	BL	
2	IO_L49P_D3_2	AD10	BL	
2	IO_L49N_D4_2	AF10	BL	
2	IO_L50P_2	U13	BL	LX75
2	IO_L50N_2	U12	BL	LX75
2	IO_L51P_2	Y10	BL	LX75
2	IO_L51N_2	AB10	BL	LX75
2	IO_L52P_2	V11	BL	LX75
2	IO_L52N_2	W11	BL	LX75
2	IO_L53P_2	AD8	BL	
2	IO_L53N_2	AF8	BL	
2	IO_L58P_2	AC9	BL	LX75
2	IO_L58N_2	AD9	BL	LX75
2	IO_L61P_2	AA9	BL	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L61N_VREF_2	AB9	BL	
2	IO_L62P_D5_2	AE7	BL	
2	IO_L62N_D6_2	AF7	BL	
2	IO_L63P_2	AD6	BL	
2	IO_L63N_2	AF6	BL	
2	IO_L64P_D8_2	AE5	BL	
2	IO_L64N_D9_2	AF5	BL	
2	IO_L65P_INIT_B_2	AE4	BL	
2	IO_L65N_CSO_B_2	AF4	BL	
2	PROGRAM_B_2	AF3	NA	
3	IO_L1P_3	AC7	LB	
3	IO_L1N_VREF_3	AD7	LB	
3	IO_L2P_3	AE3	LB	
3	IO_L2N_3	AF2	LB	
3	IO_L3P_3	AC4	LB	
3	IO_L3N_3	AD4	LB	
3	IO_L4P_3	AA8	LB	
3	IO_L4N_3	AB8	LB	
3	IO_L7P_3	AA7	LB	
3	IO_L7N_3	Y6	LB	
3	IO_L8P_3	AB7	LB	
3	IO_L8N_3	AB6	LB	
3	IO_L9P_3	Y9	LB	
3	IO_L9N_3	Y8	LB	
3	IO_L10P_3	AC5	LB	
3	IO_L10N_3	AD5	LB	
3	IO_L15P_3	W8	LB	
3	IO_L15N_3	W7	LB	
3	IO_L16P_3	AA5	LB	
3	IO_L16N_3	AB5	LB	
3	IO_L17P_3	V7	LB	
3	IO_L17N_VREF_3	V6	LB	
3	IO_L18P_3	AB4	LB	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L18N_3	AC3	LB	
3	IO_L19P_3	W9	LB	
3	IO_L19N_3	V8	LB	
3	IO_L20P_3	AA4	LB	
3	IO_L20N_3	AA3	LB	
3	IO_L21P_3	W10	LB	
3	IO_L21N_3	V10	LB	
3	IO_L22P_3	W5	LB	
3	IO_L22N_3	Y5	LB	
3	IO_L23P_3	U8	LB	
3	IO_L23N_3	U7	LB	
3	IO_L24P_3	U5	LB	
3	IO_L24N_3	V5	LB	
3	IO_L25P_3	T10	LB	
3	IO_L25N_3	U9	LB	
3	IO_L27P_3	R10	LB	
3	IO_L27N_3	T9	LB	
3	IO_L28P_3	U4	LB	
3	IO_L28N_3	U3	LB	
3	IO_L29P_3	T8	LB	
3	IO_L29N_3	T6	LB	
3	IO_L30P_3	R5	LB	
3	IO_L30N_3	T4	LB	
3	IO_L31P_3	R7	LB	
3	IO_L31N_VREF_3	R6	LB	
3	IO_L32P_M3DQ14_3	AB3	LB	
3	IO_L32N_M3DQ15_3	AB1	LB	
3	IO_L33P_M3DQ12_3	AD3	LB	
3	IO_L33N_M3DQ13_3	AD1	LB	
3	IO_L34P_M3UDQS_3	AC2	LB	
3	IO_L34N_M3UDQSN_3	AC1	LB	
3	IO_L35P_M3DQ10_3	AE2	LB	
3	IO_L35N_M3DQ11_3	AE1	LB	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L36P_M3DQ8_3	AA2	LB	
3	IO_L36N_M3DQ9_3	AA1	LB	
3	IO_L37P_M3DQ0_3	Y3	LB	
3	IO_L37N_M3DQ1_3	Y1	LB	
3	IO_L38P_M3DQ2_3	W2	LB	
3	IO_L38N_M3DQ3_3	W1	LB	
3	IO_L39P_M3LDQS_3	V3	LB	
3	IO_L39N_M3LDQSN_3	V1	LB	
3	IO_L40P_M3DQ6_3	U2	LB	
3	IO_L40N_M3DQ7_3	U1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	T3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	T1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	LB	
3	IO_L42N_GCLK24_M3LDM_3	W3	LB	
3	IO_L43P_GCLK23_M3RASN_3	N8	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	P8	LT	
3	IO_L44P_GCLK21_M3A5_3	R2	LT	
3	IO_L44N_GCLK20_M3A6_3	R1	LT	
3	IO_L45P_M3A3_3	P7	LT	
3	IO_L45N_M3ODT_3	P6	LT	
3	IO_L46P_M3CLK_3	R4	LT	
3	IO_L46N_M3CLKN_3	R3	LT	
3	IO_L47P_M3A0_3	N7	LT	
3	IO_L47N_M3A1_3	N6	LT	
3	IO_L48P_M3BA0_3	P3	LT	
3	IO_L48N_M3BA1_3	P1	LT	
3	IO_L49P_M3A7_3	P10	LT	
3	IO_L49N_M3A2_3	R9	LT	
3	IO_L50P_M3WE_3	P5	LT	
3	IO_L50N_M3BA2_3	N5	LT	
3	IO_L51P_M3A10_3	M10	LT	
3	IO_L51N_M3A4_3	N9	LT	
3	IO_L52P_M3A8_3	N4	LT	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L52N_M3A9_3	N3	LT	
3	IO_L53P_M3CKE_3	M9	LT	
3	IO_L53N_M3A12_3	M8	LT	
3	IO_L54P_M3RESET_3	L4	LT	
3	IO_L54N_M3A11_3	L3	LT	
3	IO_L55P_M3A13_3	M6	LT	
3	IO_L55N_M3A14_3	M4	LT	
3	IO_L57P_3	L7	LT	
3	IO_L57N_VREF_3	L6	LT	
4	IO_L58P_4	K8	LT	
4	IO_L58N_VREF_4	L8	LT	
4	IO_L59P_M4DQ14_4	N2	LT	
4	IO_L59N_M4DQ15_4	N1	LT	
4	IO_L60P_M4DQ12_4	M3	LT	
4	IO_L60N_M4DQ13_4	M1	LT	
4	IO_L61P_M4UDQS_4	L2	LT	
4	IO_L61N_M4UDQSN_4	L1	LT	
4	IO_L62P_M4DQ10_4	K3	LT	
4	IO_L62N_M4DQ11_4	K1	LT	
4	IO_L63P_M4DQ8_4	J2	LT	
4	IO_L63N_M4DQ9_4	J1	LT	
4	IO_L64P_M4DQ0_4	H3	LT	
4	IO_L64N_M4DQ1_4	H1	LT	
4	IO_L65P_M4DQ2_4	G2	LT	
4	IO_L65N_M4DQ3_4	G1	LT	
4	IO_L66P_M4LDQS_4	F3	LT	
4	IO_L66N_M4LDQSN_4	F1	LT	
4	IO_L67P_M4DQ6_4	E2	LT	
4	IO_L67N_M4DQ7_4	E1	LT	
4	IO_L68P_M4DQ4_4	D3	LT	
4	IO_L68N_M4DQ5_4	D1	LT	
4	IO_L69P_M4UDM_4	J4	LT	
4	IO_L69N_M4LDM_4	J3	LT	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L70P_M4RASN_4	K7	LT	
4	IO_L70N_M4CASN_4	K6	LT	
4	IO_L71P_M4A5_4	K5	LT	
4	IO_L71N_M4A6_4	J5	LT	
4	IO_L72P_M4A3_4	J7	LT	
4	IO_L72N_M4ODT_4	H7	LT	
4	IO_L73P_M4CLK_4	G4	LT	
4	IO_L73N_M4CLKN_4	G3	LT	
4	IO_L74P_M4A0_4	K10	LT	
4	IO_L74N_M4A1_4	L9	LT	
4	IO_L75P_M4BA0_4	H6	LT	
4	IO_L75N_M4BA1_4	H5	LT	
4	IO_L76P_M4A7_4	J10	LT	
4	IO_L76N_M4A2_4	K9	LT	
4	IO_L77P_M4WE_4	E4	LT	
4	IO_L77N_M4BA2_4	E3	LT	
4	IO_L78P_M4A10_4	G6	LT	
4	IO_L78N_M4A4_4	G5	LT	
4	IO_L79P_M4A8_4	C2	LT	
4	IO_L79N_M4A9_4	C1	LT	
4	IO_L80P_M4CKE_4	F5	LT	
4	IO_L80N_M4A12_4	E5	LT	
4	IO_L81P_M4RESET_4	B2	LT	
4	IO_L81N_M4A11_4	B1	LT	
4	IO_L82P_M4A13_4	H8	LT	
4	IO_L82N_M4A14_4	G7	LT	
4	IO_L83P_4	C4	LT	
4	IO_L83N_VREF_4	C3	LT	
NA	GND	A1	NA	
NA	GND	A26	NA	
NA	GND	AB12	NA	
NA	GND	AB16	NA	
NA	GND	AB2	NA	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	AB20	NA	
NA	GND	AB25	NA	
NA	GND	AC8	NA	
NA	GND	AE10	NA	
NA	GND	AE14	NA	
NA	GND	AE18	NA	
NA	GND	AE22	NA	
NA	GND	AE6	NA	
NA	GND	AF1	NA	
NA	GND	AF26	NA	
NA	GND	B13	NA	
NA	GND	B17	NA	
NA	GND	B21	NA	
NA	GND	B5	NA	
NA	GND	B9	NA	
NA	GND	D4	NA	
NA	GND	E11	NA	
NA	GND	E15	NA	
NA	GND	E22	NA	
NA	GND	E7	NA	
NA	GND	F19	NA	
NA	GND	F2	NA	
NA	GND	F25	NA	
NA	GND	H11	NA	
NA	GND	H23	NA	
NA	GND	H4	NA	
NA	GND	J19	NA	
NA	GND	J8	NA	
NA	GND	K16	NA	
NA	GND	K2	NA	
NA	GND	K25	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	L15	NA	
NA	GND	M12	NA	
NA	GND	M14	NA	
NA	GND	M16	NA	
NA	GND	M22	NA	
NA	GND	M5	NA	
NA	GND	N11	NA	
NA	GND	N13	NA	
NA	GND	N15	NA	
NA	GND	P12	NA	
NA	GND	P14	NA	
NA	GND	P16	NA	
NA	GND	P19	NA	
NA	GND	P2	NA	
NA	GND	P25	NA	
NA	GND	R11	NA	
NA	GND	R13	NA	
NA	GND	R15	NA	
NA	GND	R8	NA	
NA	GND	T12	NA	
NA	GND	T14	NA	
NA	GND	T16	NA	
NA	GND	T21	NA	
NA	GND	T5	NA	
NA	GND	U11	NA	
NA	GND	V2	NA	
NA	GND	V25	NA	
NA	GND	W15	NA	
NA	GND	W20	NA	
NA	GND	Y11	NA	
NA	GND	Y23	NA	
NA	GND	Y4	NA	
NA	GND	Y7	NA	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	AA10	NA	
NA	VCCAUX	AA16	NA	
NA	VCCAUX	AA21	NA	
NA	VCCAUX	AA6	NA	
NA	VCCAUX	F21	NA	
NA	VCCAUX	F6	NA	
NA	VCCAUX	G12	NA	
NA	VCCAUX	G15	NA	
NA	VCCAUX	J18	NA	
NA	VCCAUX	J9	NA	
NA	VCCAUX	K13	NA	
NA	VCCAUX	L22	NA	
NA	VCCAUX	L5	NA	
NA	VCCAUX	M17	NA	
NA	VCCAUX	N10	NA	
NA	VCCAUX	U14	NA	
NA	VCCAUX	U6	NA	
NA	VCCAUX	V9	NA	
NA	VCCAUX	Y19	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K17	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	L16	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M15	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	N16	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P13	NA	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	P15	NA	
NA	VCCINT	R12	NA	
NA	VCCINT	R14	NA	
NA	VCCINT	R16	NA	
NA	VCCINT	T11	NA	
NA	VCCINT	T13	NA	
NA	VCCINT	T15	NA	
NA	VCCINT	T17	NA	
NA	VCCINT	U10	NA	
NA	VCCINT	U16	NA	
0	VCCO_0	B11	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	B19	NA	
0	VCCO_0	B3	NA	
0	VCCO_0	B7	NA	
0	VCCO_0	C22	NA	
0	VCCO_0	D17	NA	
0	VCCO_0	D9	NA	
0	VCCO_0	E13	NA	
0	VCCO_0	G10	NA	
0	VCCO_0	G18	NA	
0	VCCO_0	H14	NA	
1	VCCO_1	AB23	NA	
1	VCCO_1	AD25	NA	
1	VCCO_1	M20	NA	
1	VCCO_1	P23	NA	
1	VCCO_1	T25	NA	
1	VCCO_1	U18	NA	
1	VCCO_1	V21	NA	
1	VCCO_1	W23	NA	
1	VCCO_1	Y25	NA	
2	VCCO_2	AB14	NA	
2	VCCO_2	AC10	NA	

Table 2-14: FG(G)676 Package—LX75, LX100, and LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	VCCO_2	AC18	NA	
2	VCCO_2	AC21	NA	
2	VCCO_2	AE12	NA	
2	VCCO_2	AE16	NA	
2	VCCO_2	AE20	NA	
2	VCCO_2	AE8	NA	
2	VCCO_2	Y12	NA	
2	VCCO_2	Y17	NA	
3	VCCO_3	AC6	NA	
3	VCCO_3	AD2	NA	
3	VCCO_3	M7	NA	
3	VCCO_3	P4	NA	
3	VCCO_3	P9	NA	
3	VCCO_3	T2	NA	
3	VCCO_3	T7	NA	
3	VCCO_3	W4	NA	
3	VCCO_3	W6	NA	
3	VCCO_3	Y2	NA	
4	VCCO_4	D2	NA	
4	VCCO_4	F4	NA	
4	VCCO_4	H2	NA	
4	VCCO_4	J6	NA	
4	VCCO_4	K4	NA	
4	VCCO_4	M2	NA	
5	VCCO_5	D25	NA	
5	VCCO_5	F23	NA	
5	VCCO_5	H25	NA	
5	VCCO_5	J21	NA	
5	VCCO_5	K23	NA	
5	VCCO_5	M25	NA	

FG(G)676 Package—LX75T, LX100T, and LX150T

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 and bank 5 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 and bank 4 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	H7	TL	
0	IO_L1N_VREF_0	G7	TL	
0	IO_L2P_0	H8	TL	
0	IO_L2N_0	G8	TL	
0	IO_L3P_0	F7	TL	
0	IO_L3N_0	F6	TL	
0	IO_L4P_0	C3	TL	
0	IO_L4N_0	B3	TL	
0	IO_L5P_0	G6	TL	
0	IO_L5N_0	F5	TL	
0	IO_L8P_0	E6	TL	
0	IO_L8N_VREF_0	E5	TL	
0	IO_L13P_0	H9	TL	
0	IO_L13N_0	G9	TL	
0	IO_L14P_0	A3	TL	
0	IO_L14N_0	A2	TL	
0	IO_L15P_0	F9	TL	LX75T
0	IO_L15N_0	E8	TL	LX75T
0	IO_L16P_0	D5	TL	LX75T

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L16N_0	C5	TL	LX75T
0	IO_L21P_0	H10	TL	LX75T
0	IO_L21N_0	G10	TL	LX75T
0	IO_L22P_0	B4	TL	
0	IO_L22N_0	A4	TL	
0	IO_L23P_0	F10	TL	LX75T
0	IO_L23N_0	E10	TL	LX75T
0	IO_L24P_0	B5	TL	
0	IO_L24N_0	A5	TL	
101	MGTTXN0_101	A6	NA	
101	MGTTXP0_101	B6	NA	
101	MGTAVCCPLL0_101	B11	NA	
101	MGTREFCLK0N_101	A10	NA	
101	MGTREFCLK0P_101	B10	NA	
101	MGTRXN0_101	C7	NA	
101	MGTRXP0_101	D7	NA	
101	MGTREF_101	E9	NA	
101	MGTRXN1_101	C9	NA	
101	MGTAVTTRCAL_101	E11	NA	
101	MGTRXP1_101	D9	NA	
101	MGTAVCCPLL1_101	C12	NA	
101	MGTREFCLK1N_101	C11	NA	
101	MGTREFCLK1P_101	D11	NA	
101	MGTTXN1_101	A8	NA	
101	MGTTXP1_101	B8	NA	
0	IO_L30P_0	G12	TL	LX75T, LX100T
0	IO_L30N_0	F11	TL	LX75T, LX100T
0	IO_L31P_0	F12	TL	LX75T, LX100T
0	IO_L31N_0	E12	TL	LX75T, LX100T
0	IO_L32P_0	J11	TL	
0	IO_L32N_0	G11	TL	
0	IO_L33P_0	H12	TL	
0	IO_L33N_0	G13	TL	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L34P_GCLK19_0	E13	TL	
0	IO_L34N_GCLK18_0	D13	TL	
0	IO_L35P_GCLK17_0	C13	TL	
0	IO_L35N_GCLK16_0	A13	TL	
0	IO_L36P_GCLK15_0	B12	TR	
0	IO_L36N_GCLK14_0	A12	TR	
0	IO_L37P_GCLK13_0	B14	TR	
0	IO_L37N_GCLK12_0	A14	TR	
0	IO_L38P_0	K12	TR	
0	IO_L38N_VREF_0	J12	TR	
0	IO_L39P_0	J13	TR	LX75T, LX100T
0	IO_L39N_0	H13	TR	LX75T, LX100T
0	IO_L40P_0	F14	TR	LX75T, LX100T
0	IO_L40N_0	E14	TR	LX75T, LX100T
0	IO_L41P_0	K14	TR	LX75T, LX100T
0	IO_L41N_0	H14	TR	LX75T, LX100T
123	MGTTXN0_123	A18	NA	
123	MGTTXP0_123	B18	NA	
123	MGTAVCCPLL0_123	C14	NA	
123	MGTREFCLK0N_123	C15	NA	
123	MGTREFCLK0P_123	D15	NA	
123	MGTRXN0_123	C17	NA	
123	MGTRXP0_123	D17	NA	
123	MGTRXN1_123	C19	NA	
123	MGTRXP1_123	D19	NA	
123	MGTAVCCPLL1_123	B15	NA	
123	MGTREFCLK1N_123	A16	NA	
123	MGTREFCLK1P_123	B16	NA	
123	MGTTXN1_123	A20	NA	
123	MGTTXP1_123	B20	NA	
0	IO_L43P_0	J15	TR	
0	IO_L43N_0	H15	TR	
0	IO_L48P_0	J16	TR	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L48N_0	J17	TR	
0	IO_L49P_0	F16	TR	LX75T
0	IO_L49N_0	E16	TR	LX75T
0	IO_L50P_0	G15	TR	LX75T
0	IO_L50N_0	F15	TR	LX75T
0	IO_L51P_0	F18	TR	LX75T
0	IO_L51N_0	E18	TR	LX75T
0	IO_L56P_0	G16	TR	
0	IO_L56N_0	F17	TR	
0	IO_L57P_0	F20	TR	
0	IO_L57N_0	E20	TR	
0	IO_L58P_0	H17	TR	
0	IO_L58N_0	G17	TR	
0	IO_L59P_0	C21	TR	
0	IO_L59N_0	B21	TR	
0	IO_L62P_0	H18	TR	
0	IO_L62N_VREF_0	H19	TR	
0	IO_L63P_SCP7_0	B22	TR	
0	IO_L63N_SCP6_0	A22	TR	
0	IO_L64P_SCP5_0	G19	TR	
0	IO_L64N_SCP4_0	F19	TR	
0	IO_L65P_SCP3_0	B23	TR	
0	IO_L65N_SCP2_0	A23	TR	
0	IO_L66P_SCP1_0	D21	TR	
0	IO_L66N_SCP0_0	D22	TR	
NA	TCK	A24	NA	
NA	TDI	C23	NA	
NA	TMS	F21	NA	
NA	TDO	G21	NA	
5	IO_L1P_A25_5	H20	RT	
5	IO_L1N_A24_VREF_5	G20	RT	
5	IO_L2P_M5A13_5	B24	RT	
5	IO_L2N_M5A14_5	A25	RT	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L3P_M5RESET_5	K18	RT	
5	IO_L3N_M5A11_5	K19	RT	
5	IO_L4P_M5CKE_5	D23	RT	
5	IO_L4N_M5A12_5	C24	RT	
5	IO_L5P_M5A8_5	H21	RT	
5	IO_L5N_M5A9_5	H22	RT	
5	IO_L6P_M5A10_5	F22	RT	
5	IO_L6N_M5A4_5	G23	RT	
5	IO_L7P_M5WE_5	J20	RT	
5	IO_L7N_M5BA2_5	J22	RT	
5	IO_L8P_M5A7_5	E23	RT	
5	IO_L8N_M5A2_5	E24	RT	
5	IO_L9P_M5BA0_5	L19	RT	
5	IO_L9N_M5BA1_5	K20	RT	
5	IO_L10P_M5A0_5	C25	RT	
5	IO_L10N_M5A1_5	C26	RT	
5	IO_L11P_M5CLK_5	B25	RT	
5	IO_L11N_M5CLKN_5	B26	RT	
5	IO_L12P_M5A3_5	K21	RT	
5	IO_L12N_M5ODT_5	K22	RT	
5	IO_L13P_M5A5_5	M18	RT	
5	IO_L13N_M5A6_5	M19	RT	
5	IO_L14P_M5RASN_5	F23	RT	
5	IO_L14N_M5CASN_5	G24	RT	
5	IO_L15P_M5UDM_5	J23	RT	
5	IO_L15N_M5LDM_5	J24	RT	
5	IO_L16P_M5DQ4_5	E25	RT	
5	IO_L16N_M5DQ5_5	E26	RT	
5	IO_L17P_M5DQ6_5	D24	RT	
5	IO_L17N_M5DQ7_5	D26	RT	
5	IO_L18P_M5LDQS_5	F24	RT	
5	IO_L18N_M5LDQSN_5	F26	RT	
5	IO_L19P_M5DQ2_5	H24	RT	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L19N_M5DQ3_5	H26	RT	
5	IO_L20P_M5DQ0_5	G25	RT	
5	IO_L20N_M5DQ1_5	G26	RT	
5	IO_L21P_M5DQ8_5	K24	RT	
5	IO_L21N_M5DQ9_5	K26	RT	
5	IO_L22P_M5DQ10_5	J25	RT	
5	IO_L22N_M5DQ11_5	J26	RT	
5	IO_L23P_M5UDQS_5	M24	RT	
5	IO_L23N_M5UDQSN_5	M26	RT	
5	IO_L24P_M5DQ12_5	L25	RT	
5	IO_L24N_M5DQ13_5	L26	RT	
5	IO_L25P_M5DQ14_5	N25	RT	
5	IO_L25N_M5DQ15_5	N26	RT	
5	IO_L26P_5	M21	RT	
5	IO_L26N_VREF_5	M23	RT	
5	IO_L27P_5	L20	RT	
5	IO_L27N_5	L21	RT	
1	IO_L28P_1	N17	RT	
1	IO_L28N_VREF_1	N18	RT	
1	IO_L29P_A23_M1A13_1	L23	RT	
1	IO_L29N_A22_M1A14_1	L24	RT	
1	IO_L30P_A21_M1RESET_1	N19	RT	
1	IO_L30N_A20_M1A11_1	N20	RT	
1	IO_L31P_A19_M1CKE_1	N21	RT	
1	IO_L31N_A18_M1A12_1	N22	RT	
1	IO_L32P_A17_M1A8_1	P17	RT	
1	IO_L32N_A16_M1A9_1	P19	RT	
1	IO_L33P_A15_M1A10_1	N23	RT	
1	IO_L33N_A14_M1A4_1	N24	RT	
1	IO_L34P_A13_M1WE_1	R18	RT	
1	IO_L34N_A12_M1BA2_1	R19	RT	
1	IO_L35P_A11_M1A7_1	P21	RT	
1	IO_L35N_A10_M1A2_1	P22	RT	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L36P_A9_M1BA0_1	R20	RT	
1	IO_L36N_A8_M1BA1_1	R21	RT	
1	IO_L37P_A7_M1A0_1	P24	RT	
1	IO_L37N_A6_M1A1_1	P26	RT	
1	IO_L38P_A5_M1CLK_1	R23	RT	
1	IO_L38N_A4_M1CLKN_1	R24	RT	
1	IO_L39P_M1A3_1	T22	RT	
1	IO_L39N_M1ODT_1	T23	RT	
1	IO_L40P_GCLK11_M1A5_1	U23	RT	
1	IO_L40N_GCLK10_M1A6_1	U24	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	R25	RT	
1	IO_L41N_GCLK8_M1CASN_1	R26	RT	
1	IO_L42P_GCLK7_M1UDM_1	V23	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	W24	RB	
1	IO_L43P_GCLK5_M1DQ4_1	U25	RB	
1	IO_L43N_GCLK4_M1DQ5_1	U26	RB	
1	IO_L44P_A3_M1DQ6_1	T24	RB	
1	IO_L44N_A2_M1DQ7_1	T26	RB	
1	IO_L45P_A1_M1LDQS_1	V24	RB	
1	IO_L45N_A0_M1LDQSN_1	V26	RB	
1	IO_L46P_FCS_B_M1DQ2_1	W25	RB	
1	IO_L46N_FOE_B_M1DQ3_1	W26	RB	
1	IO_L47P_FWE_B_M1DQ0_1	AA25	RB	
1	IO_L47N_LDC_M1DQ1_1	AA26	RB	
1	IO_L48P_HDC_M1DQ8_1	AD24	RB	
1	IO_L48N_M1DQ9_1	AD26	RB	
1	IO_L49P_M1DQ10_1	AB24	RB	
1	IO_L49N_M1DQ11_1	AB26	RB	
1	IO_L50P_M1UDQS_1	AC25	RB	
1	IO_L50N_M1UDQSN_1	AC26	RB	
1	IO_L51P_M1DQ12_1	Y24	RB	
1	IO_L51N_M1DQ13_1	Y26	RB	
1	IO_L52P_M1DQ14_1	AE25	RB	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L52N_M1DQ15_1	AE26	RB	
1	IO_L53P_1	U21	RB	
1	IO_L53N_VREF_1	U22	RB	
1	IO_L66P_1	T19	RB	
1	IO_L66N_1	T20	RB	
1	IO_L67P_1	AA23	RB	
1	IO_L67N_1	AA24	RB	
1	IO_L68P_1	U19	RB	
1	IO_L68N_1	U20	RB	
1	IO_L69P_1	V20	RB	
1	IO_L69N_VREF_1	V21	RB	
1	IO_L74P_AWAKE_1	AC23	RB	
1	IO_L74N_DOUT_BUSY_1	AC24	RB	
NA	VFS	W22	NA	
NA	RFUSE	V19	NA	
NA	VBATT	V22	NA	
NA	SUSPEND	Y22	NA	
2	CMPCS_B_2	Y19	NA	
2	DONE_2	AF25	NA	
2	IO_L1P_CCLK_2	AE24	BR	
2	IO_L1N_M0_CPMISO_2	AF24	BR	
2	IO_L2P_CMPCLK_2	Y21	BR	
2	IO_L2N_CPMOSI_2	AA22	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AD23	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AF23	BR	
2	IO_L4P_2	W20	BR	
2	IO_L4N_VREF_2	Y20	BR	
2	IO_L5P_2	AB22	BR	
2	IO_L5N_2	AC22	BR	
2	IO_L12P_D1_MISO2_2	V18	BR	
2	IO_L12N_D2_MISO3_2	W19	BR	
2	IO_L13P_M1_2	AD22	BR	
2	IO_L13N_D10_2	AF22	BR	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L14P_D11_2	W17	BR	
2	IO_L14N_D12_2	W18	BR	
2	IO_L15P_2	AA21	BR	
2	IO_L15N_2	AB21	BR	
2	IO_L16P_2	Y17	BR	
2	IO_L16N_VREF_2	AA17	BR	
2	IO_L17P_2	U15	BR	
2	IO_L17N_2	V16	BR	
2	IO_L18P_2	AA19	BR	LX75T
2	IO_L18N_2	AB19	BR	LX75T
2	IO_L19P_2	W16	BR	LX75T
2	IO_L19N_2	Y16	BR	LX75T
2	IO_L20P_2	AA18	BR	LX75T
2	IO_L20N_2	AB17	BR	LX75T
267	MGTTXP1_267	AE21	NA	
267	MGTTXN1_267	AF21	NA	
267	MGTAVCCPLL1_267	AE16	NA	
267	MGTREFCLK1P_267	AE17	NA	
267	MGTREFCLK1N_267	AF17	NA	
267	MGTRXP1_267	AC20	NA	
267	MGTRXN1_267	AD20	NA	
267	MGTRXP0_267	AC18	NA	
267	MGTRXN0_267	AD18	NA	
267	MGTAVCCPLL0_267	AD15	NA	
267	MGTREFCLK0P_267	AC16	NA	
267	MGTREFCLK0N_267	AD16	NA	
267	MGTTXP0_267	AE19	NA	
267	MGTTXN0_267	AF19	NA	
2	IO_L24P_2	Y15	BR	LX75T, LX100T
2	IO_L24N_VREF_2	AA16	BR	LX75T, LX100T
2	IO_L26P_2	V14	BR	LX75T, LX100T
2	IO_L26N_2	V15	BR	LX75T, LX100T
2	IO_L27P_2	U13	BR	LX75T, LX100T

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L27N_2	V13	BR	LX75T, LX100T
2	IO_L28P_2	AA15	BR	
2	IO_L28N_2	AB15	BR	
2	IO_L29P_GCLK3_2	AE15	BR	
2	IO_L29N_GCLK2_2	AF15	BR	
2	IO_L30P_GCLK1_D13_2	AB14	BR	
2	IO_L30N_GCLK0_USERCCLK_2	AC14	BR	
2	IO_L31P_GCLK31_D14_2	AE13	BL	
2	IO_L31N_GCLK30_D15_2	AF13	BL	
2	IO_L32P_GCLK29_2	AD14	BL	
2	IO_L32N_GCLK28_2	AF14	BL	
2	IO_L33P_2	Y12	BL	
2	IO_L33N_2	AA12	BL	
2	IO_L34P_2	W14	BL	
2	IO_L34N_2	Y13	BL	
2	IO_L35P_2	V12	BL	LX75T, LX100T
2	IO_L35N_2	W12	BL	LX75T, LX100T
2	IO_L36P_2	AB13	BL	LX75T, LX100T
2	IO_L36N_2	AA13	BL	LX75T, LX100T
245	MGTTPXP1_245	AE9	NA	
245	MGTTXN1_245	AF9	NA	
245	MGTAVCCPLL1_245	AD13	NA	
245	MGTREFCLK1P_245	AC12	NA	
245	MGTREFCLK1N_245	AD12	NA	
245	MGTRXP1_245	AC10	NA	
245	MGTAVTTRCAL_245	AB12	NA	
245	MGTRXN1_245	AD10	NA	
245	MGTREF_245	AB10	NA	
245	MGTRXP0_245	AC8	NA	
245	MGTRXN0_245	AD8	NA	
245	MGTAVCCPLL0_245	AE12	NA	
245	MGTREFCLK0P_245	AE11	NA	
245	MGTREFCLK0N_245	AF11	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
245	MGTTPXP0_245	AE7	NA	
245	MGTTPXN0_245	AF7	NA	
2	IO_L41P_2	Y11	BL	
2	IO_L41N_VREF_2	AA11	BL	
2	IO_L46P_2	V11	BL	
2	IO_L46N_2	V10	BL	
2	IO_L47P_2	AA9	BL	
2	IO_L47N_2	AB9	BL	
2	IO_L48P_D7_2	AA10	BL	
2	IO_L48N_RDWR_B_VREF_2	AB11	BL	
2	IO_L49P_D3_2	AD6	BL	
2	IO_L49N_D4_2	AF6	BL	
2	IO_L50P_2	W10	BL	LX75T
2	IO_L50N_2	W9	BL	LX75T
2	IO_L51P_2	AE5	BL	LX75T
2	IO_L51N_2	AF5	BL	LX75T
2	IO_L52P_2	Y9	BL	LX75T
2	IO_L52N_2	AA8	BL	LX75T
2	IO_L53P_2	AB7	BL	LX75T
2	IO_L53N_2	AC6	BL	LX75T
2	IO_L61P_2	AC5	BL	
2	IO_L61N_VREF_2	AD5	BL	
2	IO_L62P_D5_2	W8	BL	
2	IO_L62N_D6_2	W7	BL	
2	IO_L63P_2	AD4	BL	
2	IO_L63N_2	AF4	BL	
2	IO_L64P_D8_2	AA7	BL	
2	IO_L64N_D9_2	AA6	BL	
2	IO_L65P_INIT_B_2	AE3	BL	
2	IO_L65N_CSO_B_2	AF3	BL	
2	PROGRAM_B_2	AF2	NA	
3	IO_L1P_3	AB5	LB	
3	IO_L1N_VREF_3	AC4	LB	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L2P_3	AA4	LB	
3	IO_L2N_3	AA3	LB	
3	IO_L7P_3	Y6	LB	
3	IO_L7N_3	Y5	LB	
3	IO_L8P_3	AB4	LB	
3	IO_L8N_3	AC3	LB	
3	IO_L9P_3	V7	LB	
3	IO_L9N_3	V6	LB	
3	IO_L10P_3	U4	LB	
3	IO_L10N_3	U3	LB	
3	IO_L17P_3	V5	LB	
3	IO_L17N_VREF_3	W5	LB	
3	IO_L18P_3	U9	LB	
3	IO_L18N_3	U8	LB	
3	IO_L31P_3	U7	LB	
3	IO_L31N_VREF_3	T6	LB	
3	IO_L32P_M3DQ14_3	AB3	LB	
3	IO_L32N_M3DQ15_3	AB1	LB	
3	IO_L33P_M3DQ12_3	AD3	LB	
3	IO_L33N_M3DQ13_3	AD1	LB	
3	IO_L34P_M3UDQS_3	AC2	LB	
3	IO_L34N_M3UDQSN_3	AC1	LB	
3	IO_L35P_M3DQ10_3	AE2	LB	
3	IO_L35N_M3DQ11_3	AE1	LB	
3	IO_L36P_M3DQ8_3	AA2	LB	
3	IO_L36N_M3DQ9_3	AA1	LB	
3	IO_L37P_M3DQ0_3	Y3	LB	
3	IO_L37N_M3DQ1_3	Y1	LB	
3	IO_L38P_M3DQ2_3	W2	LB	
3	IO_L38N_M3DQ3_3	W1	LB	
3	IO_L39P_M3LDQS_3	V3	LB	
3	IO_L39N_M3LDQSN_3	V1	LB	
3	IO_L40P_M3DQ6_3	U2	LB	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L40N_M3DQ7_3	U1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	T3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	T1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	LB	
3	IO_L42N_GCLK24_M3LDM_3	W3	LB	
3	IO_L43P_GCLK23_M3RASN_3	R7	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	R6	LT	
3	IO_L44P_GCLK21_M3A5_3	R2	LT	
3	IO_L44N_GCLK20_M3A6_3	R1	LT	
3	IO_L45P_M3A3_3	R8	LT	
3	IO_L45N_M3ODT_3	T8	LT	
3	IO_L46P_M3CLK_3	U5	LT	
3	IO_L46N_M3CLKN_3	T4	LT	
3	IO_L47P_M3A0_3	R10	LT	
3	IO_L47N_M3A1_3	T9	LT	
3	IO_L48P_M3BA0_3	P3	LT	
3	IO_L48N_M3BA1_3	P1	LT	
3	IO_L49P_M3A7_3	N6	LT	
3	IO_L49N_M3A2_3	P6	LT	
3	IO_L50P_M3WE_3	P5	LT	
3	IO_L50N_M3BA2_3	R5	LT	
3	IO_L51P_M3A10_3	N8	LT	
3	IO_L51N_M3A4_3	N7	LT	
3	IO_L52P_M3A8_3	R4	LT	
3	IO_L52N_M3A9_3	R3	LT	
3	IO_L53P_M3CKE_3	R9	LT	
3	IO_L53N_M3A12_3	P8	LT	
3	IO_L54P_M3RESET_3	N5	LT	
3	IO_L54N_M3A11_3	N4	LT	
3	IO_L55P_M3A13_3	P10	LT	
3	IO_L55N_M3A14_3	N9	LT	
3	IO_L57P_3	M10	LT	
3	IO_L57N_VREF_3	M9	LT	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L58P_4	M4	LT	
4	IO_L58N_VREF_4	N3	LT	
4	IO_L59P_M4DQ14_4	N2	LT	
4	IO_L59N_M4DQ15_4	N1	LT	
4	IO_L60P_M4DQ12_4	M3	LT	
4	IO_L60N_M4DQ13_4	M1	LT	
4	IO_L61P_M4UDQS_4	L2	LT	
4	IO_L61N_M4UDQSN_4	L1	LT	
4	IO_L62P_M4DQ10_4	K3	LT	
4	IO_L62N_M4DQ11_4	K1	LT	
4	IO_L63P_M4DQ8_4	J2	LT	
4	IO_L63N_M4DQ9_4	J1	LT	
4	IO_L64P_M4DQ0_4	H3	LT	
4	IO_L64N_M4DQ1_4	H1	LT	
4	IO_L65P_M4DQ2_4	G2	LT	
4	IO_L65N_M4DQ3_4	G1	LT	
4	IO_L66P_M4LDQS_4	F3	LT	
4	IO_L66N_M4LDQSN_4	F1	LT	
4	IO_L67P_M4DQ6_4	E2	LT	
4	IO_L67N_M4DQ7_4	E1	LT	
4	IO_L68P_M4DQ4_4	D3	LT	
4	IO_L68N_M4DQ5_4	D1	LT	
4	IO_L69P_M4UDM_4	J4	LT	
4	IO_L69N_M4LDM_4	J3	LT	
4	IO_L70P_M4RASN_4	L9	LT	
4	IO_L70N_M4CASN_4	L8	LT	
4	IO_L71P_M4A5_4	L4	LT	
4	IO_L71N_M4A6_4	L3	LT	
4	IO_L72P_M4A3_4	M8	LT	
4	IO_L72N_M4ODT_4	M6	LT	
4	IO_L73P_M4CLK_4	K5	LT	
4	IO_L73N_M4CLKN_4	J5	LT	
4	IO_L74P_M4A0_4	L7	LT	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L74N_M4A1_4	L6	LT	
4	IO_L75P_M4BA0_4	B2	LT	
4	IO_L75N_M4BA1_4	B1	LT	
4	IO_L76P_M4A7_4	L10	LT	
4	IO_L76N_M4A2_4	K10	LT	
4	IO_L77P_M4WE_4	G4	LT	
4	IO_L77N_M4BA2_4	G3	LT	
4	IO_L78P_M4A10_4	J9	LT	
4	IO_L78N_M4A4_4	J7	LT	
4	IO_L79P_M4A8_4	C2	LT	
4	IO_L79N_M4A9_4	C1	LT	
4	IO_L80P_M4CKE_4	K9	LT	
4	IO_L80N_M4A12_4	K8	LT	
4	IO_L81P_M4RESET_4	E4	LT	
4	IO_L81N_M4A11_4	E3	LT	
4	IO_L82P_M4A13_4	K7	LT	
4	IO_L82N_M4A14_4	K6	LT	
4	IO_L83P_4	H6	LT	
4	IO_L83N_VREF_4	H5	LT	
NA	GND	A1	NA	
NA	GND	A11	NA	
NA	GND	A15	NA	
NA	GND	A17	NA	
NA	GND	A21	NA	
NA	GND	A26	NA	
NA	GND	A9	NA	
NA	GND	AB16	NA	
NA	GND	AB2	NA	
NA	GND	AB20	NA	
NA	GND	AB25	NA	
NA	GND	AC11	NA	
NA	GND	AC13	NA	
NA	GND	AC15	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	AC17	NA	
NA	GND	AD19	NA	
NA	GND	AD21	NA	
NA	GND	AD7	NA	
NA	GND	AD9	NA	
NA	GND	AE10	NA	
NA	GND	AE18	NA	
NA	GND	AE20	NA	
NA	GND	AE22	NA	
NA	GND	AE6	NA	
NA	GND	AE8	NA	
NA	GND	AF1	NA	
NA	GND	AF10	NA	
NA	GND	AF12	NA	
NA	GND	AF16	NA	
NA	GND	AF18	NA	
NA	GND	AF26	NA	
NA	GND	B17	NA	
NA	GND	B19	NA	
NA	GND	B7	NA	
NA	GND	B9	NA	
NA	GND	C18	NA	
NA	GND	C20	NA	
NA	GND	C6	NA	
NA	GND	C8	NA	
NA	GND	D10	NA	
NA	GND	D12	NA	
NA	GND	D14	NA	
NA	GND	D16	NA	
NA	GND	D4	NA	
NA	GND	E15	NA	
NA	GND	E19	NA	
NA	GND	E22	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	E7	NA	
NA	GND	F2	NA	
NA	GND	F25	NA	
NA	GND	G14	NA	
NA	GND	H23	NA	
NA	GND	H4	NA	
NA	GND	J19	NA	
NA	GND	J8	NA	
NA	GND	K16	NA	
NA	GND	K2	NA	
NA	GND	K25	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	
NA	GND	L15	NA	
NA	GND	L17	NA	
NA	GND	M22	NA	
NA	GND	M5	NA	
NA	GND	N11	NA	
NA	GND	N14	NA	
NA	GND	P13	NA	
NA	GND	P16	NA	
NA	GND	P2	NA	
NA	GND	P20	NA	
NA	GND	P25	NA	
NA	GND	P7	NA	
NA	GND	T10	NA	
NA	GND	T12	NA	
NA	GND	T14	NA	
NA	GND	T16	NA	
NA	GND	T18	NA	
NA	GND	T21	NA	
NA	GND	T5	NA	
NA	GND	U11	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	U17	NA	
NA	GND	V2	NA	
NA	GND	V25	NA	
NA	GND	V8	NA	
NA	GND	Y10	NA	
NA	GND	Y14	NA	
NA	GND	Y23	NA	
NA	GND	Y4	NA	
NA	GND	Y7	NA	
101	MGTAVCC_101	C10	NA	
123	MGTAVCC_123	C16	NA	
245	MGTAVCC_245	AD11	NA	
267	MGTAVCC_267	AD17	NA	
101	MGTAVTTRX_101	D8	NA	
123	MGTAVTTRX_123	D18	NA	
245	MGTAVTTRX_245	AC9	NA	
267	MGTAVTTRX_267	AC19	NA	
101	MGTAVTTTX_101	A7	NA	
123	MGTAVTTTX_123	A19	NA	
245	MGTAVTTTX_245	AF8	NA	
267	MGTAVTTTX_267	AF20	NA	
NA	VCCAUX	AA5	NA	
NA	VCCAUX	AB18	NA	
NA	VCCAUX	AB8	NA	
NA	VCCAUX	AC21	NA	
NA	VCCAUX	AC7	NA	
NA	VCCAUX	D20	NA	
NA	VCCAUX	D6	NA	
NA	VCCAUX	E17	NA	
NA	VCCAUX	G5	NA	
NA	VCCAUX	J10	NA	
NA	VCCAUX	J18	NA	
NA	VCCAUX	K13	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	K15	NA	
NA	VCCAUX	L18	NA	
NA	VCCAUX	L22	NA	
NA	VCCAUX	L5	NA	
NA	VCCAUX	M17	NA	
NA	VCCAUX	N10	NA	
NA	VCCAUX	R22	NA	
NA	VCCAUX	U12	NA	
NA	VCCAUX	U14	NA	
NA	VCCAUX	U18	NA	
NA	VCCAUX	U6	NA	
NA	VCCAUX	V17	NA	
NA	VCCAUX	V9	NA	
NA	VCCAUX	W13	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K17	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L14	NA	
NA	VCCINT	L16	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M12	NA	
NA	VCCINT	M13	NA	
NA	VCCINT	M14	NA	
NA	VCCINT	M15	NA	
NA	VCCINT	M16	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N13	NA	
NA	VCCINT	N15	NA	
NA	VCCINT	N16	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P12	NA	
NA	VCCINT	P14	NA	
NA	VCCINT	P15	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	R11	NA	
NA	VCCINT	R12	NA	
NA	VCCINT	R13	NA	
NA	VCCINT	R14	NA	
NA	VCCINT	R15	NA	
NA	VCCINT	R16	NA	
NA	VCCINT	R17	NA	
NA	VCCINT	T11	NA	
NA	VCCINT	T13	NA	
NA	VCCINT	T15	NA	
NA	VCCINT	T17	NA	
NA	VCCINT	U10	NA	
NA	VCCINT	U16	NA	
0	VCCO_0	B13	NA	
0	VCCO_0	C22	NA	
0	VCCO_0	C4	NA	
0	VCCO_0	E21	NA	
0	VCCO_0	F13	NA	
0	VCCO_0	F8	NA	
0	VCCO_0	G18	NA	
0	VCCO_0	H11	NA	
0	VCCO_0	H16	NA	
0	VCCO_0	J14	NA	
1	VCCO_1	AB23	NA	
1	VCCO_1	AD25	NA	
1	VCCO_1	P18	NA	
1	VCCO_1	P23	NA	
1	VCCO_1	T25	NA	
1	VCCO_1	W21	NA	
1	VCCO_1	W23	NA	
1	VCCO_1	Y25	NA	
2	VCCO_2	AA14	NA	
2	VCCO_2	AA20	NA	

Table 2-15: FG(G)676 Package—LX75T, LX100T, and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	VCCO_2	AB6	NA	
2	VCCO_2	AE14	NA	
2	VCCO_2	AE23	NA	
2	VCCO_2	AE4	NA	
2	VCCO_2	W11	NA	
2	VCCO_2	W15	NA	
2	VCCO_2	Y18	NA	
2	VCCO_2	Y8	NA	
3	VCCO_3	AD2	NA	
3	VCCO_3	P4	NA	
3	VCCO_3	P9	NA	
3	VCCO_3	T2	NA	
3	VCCO_3	T7	NA	
3	VCCO_3	W4	NA	
3	VCCO_3	W6	NA	
3	VCCO_3	Y2	NA	
4	VCCO_4	D2	NA	
4	VCCO_4	F4	NA	
4	VCCO_4	H2	NA	
4	VCCO_4	J6	NA	
4	VCCO_4	K4	NA	
4	VCCO_4	M2	NA	
4	VCCO_4	M7	NA	
5	VCCO_5	D25	NA	
5	VCCO_5	G22	NA	
5	VCCO_5	H25	NA	
5	VCCO_5	J21	NA	
5	VCCO_5	K23	NA	
5	VCCO_5	M20	NA	
5	VCCO_5	M25	NA	

FG(G)900 Package—LX150

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 and bank 5 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 and bank 4 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-16: FG(G)900 Package—LX150

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	G9	TL	
0	IO_L1N_VREF_0	F9	TL	
0	IO_L2P_0	G7	TL	
0	IO_L2N_0	F7	TL	
0	IO_L3P_0	G6	TL	
0	IO_L3N_0	F6	TL	
0	IO_L4P_0	G8	TL	
0	IO_L4N_0	F8	TL	
0	IO_L5P_0	E6	TL	
0	IO_L5N_0	D6	TL	
0	IO_L6P_0	E8	TL	
0	IO_L6N_0	D8	TL	
0	IO_L7P_0	J10	TL	
0	IO_L7N_0	G10	TL	
0	IO_L8P_0	C6	TL	
0	IO_L8N_VREF_0	A6	TL	
0	IO_L9P_0	B7	TL	
0	IO_L9N_0	A7	TL	
0	IO_L10P_0	D7	TL	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L10N_0	C7	TL	
0	IO_L11P_0	J11	TL	
0	IO_L11N_0	H11	TL	
0	IO_L12P_0	E10	TL	
0	IO_L12N_0	D10	TL	
0	IO_L13P_0	C8	TL	
0	IO_L13N_0	A8	TL	
0	IO_L14P_0	D9	TL	
0	IO_L14N_0	C9	TL	
0	IO_L15P_0	K12	TL	
0	IO_L15N_0	J12	TL	
0	IO_L16P_0	G11	TL	
0	IO_L16N_0	F11	TL	
0	IO_L17P_0	B9	TL	
0	IO_L17N_0	A9	TL	
0	IO_L18P_0	C10	TL	
0	IO_L18N_0	A10	TL	
0	IO_L19P_0	D11	TL	
0	IO_L19N_0	C11	TL	
0	IO_L20P_0	G12	TL	
0	IO_L20N_0	F12	TL	
0	IO_L21P_0	E12	TL	
0	IO_L21N_0	D12	TL	
0	IO_L22P_0	B11	TL	
0	IO_L22N_0	A11	TL	
0	IO_L23P_0	C12	TL	
0	IO_L23N_0	A12	TL	
0	IO_L24P_0	D13	TL	
0	IO_L24N_0	C13	TL	
0	IO_L25P_0	J13	TL	
0	IO_L25N_0	H13	TL	
0	IO_L26P_0	G13	TL	
0	IO_L26N_0	F13	TL	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L27P_0	K14	TL	
0	IO_L27N_0	J14	TL	
0	IO_L28P_0	G14	TL	
0	IO_L28N_0	F14	TL	
0	IO_L29P_0	E14	TL	
0	IO_L29N_0	D14	TL	
0	IO_L30P_0	B13	TL	
0	IO_L30N_0	A13	TL	
0	IO_L31P_0	C14	TL	
0	IO_L31N_0	A14	TL	
0	IO_L32P_0	J15	TL	
0	IO_L32N_0	H15	TL	
0	IO_L33P_0	G15	TL	
0	IO_L33N_0	F15	TL	
0	IO_L34P_GCLK19_0	D15	TL	
0	IO_L34N_GCLK18_0	C15	TL	
0	IO_L35P_GCLK17_0	B15	TL	
0	IO_L35N_GCLK16_0	A15	TL	
0	IO_L36P_GCLK15_0	C16	TR	
0	IO_L36N_GCLK14_0	A16	TR	
0	IO_L37P_GCLK13_0	C18	TR	
0	IO_L37N_GCLK12_0	A18	TR	
0	IO_L38P_0	B17	TR	
0	IO_L38N_VREF_0	A17	TR	
0	IO_L39P_0	E16	TR	
0	IO_L39N_0	D16	TR	
0	IO_L40P_0	G16	TR	
0	IO_L40N_0	F16	TR	
0	IO_L41P_0	D17	TR	
0	IO_L41N_0	C17	TR	
0	IO_L42P_0	G17	TR	
0	IO_L42N_0	F17	TR	
0	IO_L43P_0	J17	TR	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L43N_0	H17	TR	
0	IO_L44P_0	B19	TR	
0	IO_L44N_0	A19	TR	
0	IO_L45P_0	E18	TR	
0	IO_L45N_0	D18	TR	
0	IO_L46P_0	G18	TR	
0	IO_L46N_0	F18	TR	
0	IO_L47P_0	C20	TR	
0	IO_L47N_0	A20	TR	
0	IO_L48P_0	D19	TR	
0	IO_L48N_0	C19	TR	
0	IO_L49P_0	G19	TR	
0	IO_L49N_0	F19	TR	
0	IO_L50P_0	B21	TR	
0	IO_L50N_0	A21	TR	
0	IO_L51P_0	J19	TR	
0	IO_L51N_0	H19	TR	
0	IO_L52P_0	E20	TR	
0	IO_L52N_0	D20	TR	
0	IO_L53P_0	C22	TR	
0	IO_L53N_0	A22	TR	
0	IO_L54P_0	D21	TR	
0	IO_L54N_0	C21	TR	
0	IO_L55P_0	E22	TR	
0	IO_L55N_0	D22	TR	
0	IO_L56P_0	B23	TR	
0	IO_L56N_0	A23	TR	
0	IO_L57P_0	J20	TR	
0	IO_L57N_0	G20	TR	
0	IO_L58P_0	G21	TR	
0	IO_L58N_0	F21	TR	
0	IO_L59P_0	D23	TR	
0	IO_L59N_0	C23	TR	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L60P_0	G22	TR	
0	IO_L60N_0	F22	TR	
0	IO_L61P_0	E24	TR	
0	IO_L61N_0	D24	TR	
0	IO_L62P_0	G23	TR	
0	IO_L62N_VREF_0	F23	TR	
0	IO_L63P_SCP7_0	B25	TR	
0	IO_L63N_SCP6_0	A25	TR	
0	IO_L64P_SCP5_0	C24	TR	
0	IO_L64N_SCP4_0	A24	TR	
0	IO_L65P_SCP3_0	J21	TR	
0	IO_L65N_SCP2_0	H21	TR	
0	IO_L66P_SCP1_0	D25	TR	
0	IO_L66N_SCP0_0	C25	TR	
NA	TCK	F24	NA	
NA	TDI	H25	NA	
NA	TMS	K25	NA	
NA	TDO	G24	NA	
5	IO_L1P_A25_5	G25	RT	
5	IO_L1N_A24_VREF_5	F25	RT	
5	IO_L2P_M5A13_5	A28	RT	
5	IO_L2N_M5A14_5	A29	RT	
5	IO_L3P_M5RESET_5	C26	RT	
5	IO_L3N_M5A11_5	A26	RT	
5	IO_L4P_M5CKE_5	B29	RT	
5	IO_L4N_M5A12_5	B30	RT	
5	IO_L5P_M5A8_5	B27	RT	
5	IO_L5N_M5A9_5	A27	RT	
5	IO_L6P_M5A10_5	F26	RT	
5	IO_L6N_M5A4_5	F27	RT	
5	IO_L7P_M5WE_5	E26	RT	
5	IO_L7N_M5BA2_5	D26	RT	
5	IO_L8P_M5A7_5	C29	RT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L8N_M5A2_5	C30	RT	
5	IO_L9P_M5BA0_5	D27	RT	
5	IO_L9N_M5BA1_5	C27	RT	
5	IO_L10P_M5A0_5	D28	RT	
5	IO_L10N_M5A1_5	D30	RT	
5	IO_L11P_M5CLK_5	E27	RT	
5	IO_L11N_M5CLKN_5	E28	RT	
5	IO_L12P_M5A3_5	E29	RT	
5	IO_L12N_M5ODT_5	E30	RT	
5	IO_L13P_M5A5_5	H26	RT	
5	IO_L13N_M5A6_5	H27	RT	
5	IO_L14P_M5RASN_5	K26	RT	
5	IO_L14N_M5CASN_5	K27	RT	
5	IO_L15P_M5UDM_5	J27	RT	
5	IO_L15N_M5LDM_5	J28	RT	
5	IO_L16P_M5DQ4_5	G27	RT	
5	IO_L16N_M5DQ5_5	G28	RT	
5	IO_L17P_M5DQ6_5	F28	RT	
5	IO_L17N_M5DQ7_5	F30	RT	
5	IO_L18P_M5LDQS_5	J29	RT	
5	IO_L18N_M5LDQSN_5	J30	RT	
5	IO_L19P_M5DQ2_5	G29	RT	
5	IO_L19N_M5DQ3_5	G30	RT	
5	IO_L20P_M5DQ0_5	H28	RT	
5	IO_L20N_M5DQ1_5	H30	RT	
5	IO_L21P_M5DQ8_5	L27	RT	
5	IO_L21N_M5DQ9_5	L28	RT	
5	IO_L22P_M5DQ10_5	L29	RT	
5	IO_L22N_M5DQ11_5	L30	RT	
5	IO_L23P_M5UDQS_5	K28	RT	
5	IO_L23N_M5UDQSN_5	K30	RT	
5	IO_L24P_M5DQ12_5	M26	RT	
5	IO_L24N_M5DQ13_5	M27	RT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L25P_M5DQ14_5	M28	RT	
5	IO_L25N_M5DQ15_5	M30	RT	
5	IO_L26P_5	N24	RT	
5	IO_L26N_VREF_5	N25	RT	
5	IO_L27P_5	L24	RT	
5	IO_L27N_5	L25	RT	
1	IO_L28P_1	M23	RT	
1	IO_L28N_VREF_1	M24	RT	
1	IO_L29P_A23_M1A13_1	N29	RT	
1	IO_L29N_A22_M1A14_1	N30	RT	
1	IO_L30P_A21_M1RESET_1	N27	RT	
1	IO_L30N_A20_M1A11_1	N28	RT	
1	IO_L31P_A19_M1CKE_1	P28	RT	
1	IO_L31N_A18_M1A12_1	P30	RT	
1	IO_L32P_A17_M1A8_1	P26	RT	
1	IO_L32N_A16_M1A9_1	P27	RT	
1	IO_L33P_A15_M1A10_1	R29	RT	
1	IO_L33N_A14_M1A4_1	R30	RT	
1	IO_L34P_A13_M1WE_1	R27	RT	
1	IO_L34N_A12_M1BA2_1	R28	RT	
1	IO_L35P_A11_M1A7_1	T26	RT	
1	IO_L35N_A10_M1A2_1	T27	RT	
1	IO_L36P_A9_M1BA0_1	T28	RT	
1	IO_L36N_A8_M1BA1_1	T30	RT	
1	IO_L37P_A7_M1A0_1	U29	RT	
1	IO_L37N_A6_M1A1_1	U30	RT	
1	IO_L38P_A5_M1CLK_1	U27	RT	
1	IO_L38N_A4_M1CLKN_1	U28	RT	
1	IO_L39P_M1A3_1	V28	RT	
1	IO_L39N_M1ODT_1	V30	RT	
1	IO_L40P_GCLK11_M1A5_1	V26	RT	
1	IO_L40N_GCLK10_M1A6_1	V27	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	W27	RT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L41N_GCLK8_M1CASN_1	W28	RT	
1	IO_L42P_GCLK7_M1UDM_1	AB28	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	AB30	RB	
1	IO_L43P_GCLK5_M1DQ4_1	W29	RB	
1	IO_L43N_GCLK4_M1DQ5_1	W30	RB	
1	IO_L44P_A3_M1DQ6_1	Y28	RB	
1	IO_L44N_A2_M1DQ7_1	Y30	RB	
1	IO_L45P_A1_M1LDQS_1	AA29	RB	
1	IO_L45N_A0_M1LDQSN_1	AA30	RB	
1	IO_L46P_FCS_B_M1DQ2_1	AA27	RB	
1	IO_L46N_FOE_B_M1DQ3_1	AA28	RB	
1	IO_L47P_FWE_B_M1DQ0_1	Y26	RB	
1	IO_L47N_LDC_M1DQ1_1	Y27	RB	
1	IO_L48P_HDC_M1DQ8_1	AD28	RB	
1	IO_L48N_M1DQ9_1	AD30	RB	
1	IO_L49P_M1DQ10_1	AC27	RB	
1	IO_L49N_M1DQ11_1	AC28	RB	
1	IO_L50P_M1UDQS_1	AC29	RB	
1	IO_L50N_M1UDQSN_1	AC30	RB	
1	IO_L51P_M1DQ12_1	AE29	RB	
1	IO_L51N_M1DQ13_1	AE30	RB	
1	IO_L52P_M1DQ14_1	AE27	RB	
1	IO_L52N_M1DQ15_1	AE28	RB	
1	IO_L53P_1	W24	RB	
1	IO_L53N_VREF_1	W25	RB	
1	IO_L54P_1	R21	RB	
1	IO_L54N_1	R22	RB	
1	IO_L55P_1	AF28	RB	
1	IO_L55N_1	AF30	RB	
1	IO_L56P_1	P22	RB	
1	IO_L56N_1	P23	RB	
1	IO_L57P_1	AG29	RB	
1	IO_L57N_1	AG30	RB	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L58P_1	P24	RB	
1	IO_L58N_1	P25	RB	
1	IO_L59P_1	AH30	RB	
1	IO_L59N_1	AJ30	RB	
1	IO_L60P_1	R24	RB	
1	IO_L60N_1	R25	RB	
1	IO_L61P_1	AJ29	RB	
1	IO_L61N_1	AK29	RB	
1	IO_L62P_1	T24	RB	
1	IO_L62N_1	T25	RB	
1	IO_L63P_1	AJ28	RB	
1	IO_L63N_1	AK28	RB	
1	IO_L64P_1	U24	RB	
1	IO_L64N_1	U25	RB	
1	IO_L65P_1	AG27	RB	
1	IO_L65N_1	AG28	RB	
1	IO_L66P_1	V23	RB	
1	IO_L66N_1	V24	RB	
1	IO_L67P_1	AD26	RB	
1	IO_L67N_1	AD27	RB	
1	IO_L68P_1	W21	RB	
1	IO_L68N_1	W22	RB	
1	IO_L69P_1	AH27	RB	
1	IO_L69N_VREF_1	AK27	RB	
1	IO_L70P_1	Y22	RB	
1	IO_L70N_1	Y23	RB	
1	IO_L71P_1	AE25	RB	
1	IO_L71N_1	AE26	RB	
1	IO_L72P_1	Y24	RB	
1	IO_L72N_1	Y25	RB	
1	IO_L73P_1	AG26	RB	
1	IO_L73N_1	AH26	RB	
1	IO_L74P_AWAKE_1	AA24	RB	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L74N_DOUT_BUSY_1	AA25	RB	
NA	VFS	AF27	NA	
NA	RFUSE	AB27	NA	
NA	VBATT	AB26	NA	
NA	SUSPEND	AB25	NA	
2	CMPCS_B_2	AC25	NA	
2	DONE_2	AD25	NA	
2	IO_L1P_CCLK_2	AJ26	BR	
2	IO_L1N_M0_CPMISO_2	AK26	BR	
2	IO_L2P_CMPCLK_2	AD24	BR	
2	IO_L2N_CPMOSI_2	AE24	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AH25	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AK25	BR	
2	IO_L4P_2	AF25	BR	
2	IO_L4N_VREF_2	AG25	BR	
2	IO_L5P_2	AG24	BR	
2	IO_L5N_2	AH24	BR	
2	IO_L6P_2	AD23	BR	
2	IO_L6N_2	AE23	BR	
2	IO_L7P_2	AD22	BR	
2	IO_L7N_2	AE22	BR	
2	IO_L8P_2	AC21	BR	
2	IO_L8N_2	AD21	BR	
2	IO_L9P_2	AF23	BR	
2	IO_L9N_2	AG23	BR	
2	IO_L10P_2	AD20	BR	
2	IO_L10N_2	AE20	BR	
2	IO_L11P_2	AJ24	BR	
2	IO_L11N_2	AK24	BR	
2	IO_L12P_D1_MISO2_2	AH23	BR	
2	IO_L12N_D2_MISO3_2	AK23	BR	
2	IO_L13P_M1_2	AJ22	BR	
2	IO_L13N_D10_2	AK22	BR	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L14P_D11_2	AH21	BR	
2	IO_L14N_D12_2	AK21	BR	
2	IO_L15P_2	AG22	BR	
2	IO_L15N_2	AH22	BR	
2	IO_L16P_2	AJ20	BR	
2	IO_L16N_VREF_2	AK20	BR	
2	IO_L17P_2	AF21	BR	
2	IO_L17N_2	AG21	BR	
2	IO_L18P_2	AB20	BR	
2	IO_L18N_2	AC20	BR	
2	IO_L19P_2	AD19	BR	
2	IO_L19N_2	AE19	BR	
2	IO_L20P_2	AG20	BR	
2	IO_L20N_2	AH20	BR	
2	IO_L21P_2	AD18	BR	
2	IO_L21N_2	AE18	BR	
2	IO_L22P_2	AA19	BR	
2	IO_L22N_2	AB19	BR	
2	IO_L23P_2	AF19	BR	
2	IO_L23N_2	AG19	BR	
2	IO_L24P_2	AG18	BR	
2	IO_L24N_VREF_2	AH18	BR	
2	IO_L25P_2	AB18	BR	
2	IO_L25N_2	AC18	BR	
2	IO_L26P_2	AF17	BR	
2	IO_L26N_2	AG17	BR	
2	IO_L27P_2	AD17	BR	
2	IO_L27N_2	AE17	BR	
2	IO_L28P_2	AD16	BR	
2	IO_L28N_2	AE16	BR	
2	IO_L29P_GCLK3_2	AH19	BR	
2	IO_L29N_GCLK2_2	AK19	BR	
2	IO_L30P_GCLK1_D13_2	AJ18	BR	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L30N_GCLK0_USERCCLK_2	AK18	BR	
2	IO_L31P_GCLK31_D14_2	AJ16	BL	
2	IO_L31N_GCLK30_D15_2	AK16	BL	
2	IO_L32P_GCLK29_2	AH17	BL	
2	IO_L32N_GCLK28_2	AK17	BL	
2	IO_L33P_2	AB16	BL	
2	IO_L33N_2	AC16	BL	
2	IO_L34P_2	AF15	BL	
2	IO_L34N_2	AG15	BL	
2	IO_L35P_2	AG16	BL	
2	IO_L35N_2	AH16	BL	
2	IO_L36P_2	AD15	BL	
2	IO_L36N_2	AE15	BL	
2	IO_L37P_2	AA15	BL	
2	IO_L37N_2	AB15	BL	
2	IO_L38P_2	AH15	BL	
2	IO_L38N_2	AK15	BL	
2	IO_L39P_2	AJ14	BL	
2	IO_L39N_2	AK14	BL	
2	IO_L40P_2	AB14	BL	
2	IO_L40N_2	AC14	BL	
2	IO_L41P_2	AH13	BL	
2	IO_L41N_VREF_2	AK13	BL	
2	IO_L42P_2	AD14	BL	
2	IO_L42N_2	AE14	BL	
2	IO_L43P_2	AF13	BL	
2	IO_L43N_2	AG13	BL	
2	IO_L44P_2	AG14	BL	
2	IO_L44N_2	AH14	BL	
2	IO_L45P_2	AG12	BL	
2	IO_L45N_2	AH12	BL	
2	IO_L46P_2	AD13	BL	
2	IO_L46N_2	AE13	BL	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L47P_2	AD12	BL	
2	IO_L47N_2	AE12	BL	
2	IO_L48P_D7_2	AH11	BL	
2	IO_L48N_RDWR_B_VREF_2	AK11	BL	
2	IO_L49P_D3_2	AJ12	BL	
2	IO_L49N_D4_2	AK12	BL	
2	IO_L50P_2	AB12	BL	
2	IO_L50N_2	AC12	BL	
2	IO_L51P_2	AF11	BL	
2	IO_L51N_2	AG11	BL	
2	IO_L52P_2	AB11	BL	
2	IO_L52N_2	AD11	BL	
2	IO_L53P_2	AJ10	BL	
2	IO_L53N_2	AK10	BL	
2	IO_L54P_2	AH9	BL	
2	IO_L54N_2	AK9	BL	
2	IO_L55P_2	AG10	BL	
2	IO_L55N_2	AH10	BL	
2	IO_L56P_2	AD10	BL	
2	IO_L56N_2	AE10	BL	
2	IO_L57P_2	AF9	BL	
2	IO_L57N_2	AG9	BL	
2	IO_L58P_2	AG8	BL	
2	IO_L58N_2	AH8	BL	
2	IO_L59P_2	AF7	BL	
2	IO_L59N_2	AG7	BL	
2	IO_L60P_2	AD9	BL	
2	IO_L60N_2	AE9	BL	
2	IO_L61P_2	AD8	BL	
2	IO_L61N_VREF_2	AE8	BL	
2	IO_L62P_D5_2	AJ8	BL	
2	IO_L62N_D6_2	AK8	BL	
2	IO_L63P_2	AG6	BL	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L63N_2	AH6	BL	
2	IO_L64P_D8_2	AH7	BL	
2	IO_L64N_D9_2	AK7	BL	
2	IO_L65P_INIT_B_2	AJ6	BL	
2	IO_L65N_CSO_B_2	AK6	BL	
2	PROGRAM_B_2	AB8	NA	
3	IO_L1P_3	AA10	LB	
3	IO_L1N_VREF_3	AA9	LB	
3	IO_L2P_3	AD7	LB	
3	IO_L2N_3	AE7	LB	
3	IO_L3P_3	Y9	LB	
3	IO_L3N_3	Y8	LB	
3	IO_L4P_3	AE6	LB	
3	IO_L4N_3	AF6	LB	
3	IO_L5P_3	AA12	LB	
3	IO_L5N_3	AA11	LB	
3	IO_L6P_3	AE5	LB	
3	IO_L6N_3	AG5	LB	
3	IO_L7P_3	T7	LB	
3	IO_L7N_3	T6	LB	
3	IO_L8P_3	AA7	LB	
3	IO_L8N_3	AA6	LB	
3	IO_L9P_3	AC6	LB	
3	IO_L9N_3	AD6	LB	
3	IO_L10P_3	AH5	LB	
3	IO_L10N_3	AK5	LB	
3	IO_L11P_3	W10	LB	
3	IO_L11N_3	W9	LB	
3	IO_L12P_3	AB7	LB	
3	IO_L12N_3	AB6	LB	
3	IO_L13P_3	W7	LB	
3	IO_L13N_3	W6	LB	
3	IO_L14P_3	AJ4	LB	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L14N_3	AK4	LB	
3	IO_L15P_3	T9	LB	
3	IO_L15N_3	T8	LB	
3	IO_L16P_3	AH3	LB	
3	IO_L16N_3	AK3	LB	
3	IO_L17P_3	Y7	LB	
3	IO_L17N_VREF_3	Y6	LB	
3	IO_L18P_3	AJ2	LB	
3	IO_L18N_3	AK2	LB	
3	IO_L19P_3	AE4	LB	
3	IO_L19N_3	AF4	LB	
3	IO_L20P_3	AF3	LB	
3	IO_L20N_3	AG3	LB	
3	IO_L21P_3	V8	LB	
3	IO_L21N_3	V7	LB	
3	IO_L22P_3	AH1	LB	
3	IO_L22N_3	AJ1	LB	
3	IO_L23P_3	V10	LB	
3	IO_L23N_3	V9	LB	
3	IO_L24P_3	AG4	LB	
3	IO_L24N_3	AH4	LB	
3	IO_L25P_3	N10	LB	
3	IO_L25N_3	N9	LB	
3	IO_L26P_3	AF2	LB	
3	IO_L26N_3	AH2	LB	
3	IO_L27P_3	R7	LB	
3	IO_L27N_3	R6	LB	
3	IO_L28P_3	AF1	LB	
3	IO_L28N_3	AG1	LB	
3	IO_L29P_3	U7	LB	
3	IO_L29N_3	U6	LB	
3	IO_L30P_3	AE3	LB	
3	IO_L30N_3	AE1	LB	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L31P_3	N8	LB	
3	IO_L31N_VREF_3	N7	LB	
3	IO_L32P_M3DQ14_3	AC5	LB	
3	IO_L32N_M3DQ15_3	AC4	LB	
3	IO_L33P_M3DQ12_3	AD4	LB	
3	IO_L33N_M3DQ13_3	AD3	LB	
3	IO_L34P_M3UDQS_3	AB4	LB	
3	IO_L34N_M3UDQSN_3	AB3	LB	
3	IO_L35P_M3DQ10_3	AD2	LB	
3	IO_L35N_M3DQ11_3	AD1	LB	
3	IO_L36P_M3DQ8_3	AC3	LB	
3	IO_L36N_M3DQ9_3	AC1	LB	
3	IO_L37P_M3DQ0_3	Y4	LB	
3	IO_L37N_M3DQ1_3	Y3	LB	
3	IO_L38P_M3DQ2_3	Y2	LB	
3	IO_L38N_M3DQ3_3	Y1	LB	
3	IO_L39P_M3LDQS_3	AA5	LB	
3	IO_L39N_M3LDQSN_3	AA4	LB	
3	IO_L40P_M3DQ6_3	W3	LB	
3	IO_L40N_M3DQ7_3	W1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	AA3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	AA1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	AB2	LB	
3	IO_L42N_GCLK24_M3LDM_3	AB1	LB	
3	IO_L43P_GCLK23_M3RASN_3	W5	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	W4	LT	
3	IO_L44P_GCLK21_M3A5_3	V4	LT	
3	IO_L44N_GCLK20_M3A6_3	V3	LT	
3	IO_L45P_M3A3_3	V2	LT	
3	IO_L45N_M3ODT_3	V1	LT	
3	IO_L46P_M3CLK_3	U5	LT	
3	IO_L46N_M3CLKN_3	U4	LT	
3	IO_L47P_M3A0_3	U3	LT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L47N_M3A1_3	U1	LT	
3	IO_L48P_M3BA0_3	T4	LT	
3	IO_L48N_M3BA1_3	T3	LT	
3	IO_L49P_M3A7_3	T2	LT	
3	IO_L49N_M3A2_3	T1	LT	
3	IO_L50P_M3WE_3	R5	LT	
3	IO_L50N_M3BA2_3	R4	LT	
3	IO_L51P_M3A10_3	R3	LT	
3	IO_L51N_M3A4_3	R1	LT	
3	IO_L52P_M3A8_3	P4	LT	
3	IO_L52N_M3A9_3	P3	LT	
3	IO_L53P_M3CKE_3	N5	LT	
3	IO_L53N_M3A12_3	N4	LT	
3	IO_L54P_M3RESET_3	P2	LT	
3	IO_L54N_M3A11_3	P1	LT	
3	IO_L55P_M3A13_3	N3	LT	
3	IO_L55N_M3A14_3	N1	LT	
3	IO_L56P_3	P7	LT	
3	IO_L56N_3	P6	LT	
3	IO_L57P_3	M7	LT	
3	IO_L57N_VREF_3	M6	LT	
4	IO_L58P_4	L7	LT	
4	IO_L58N_VREF_4	L6	LT	
4	IO_L59P_M4DQ14_4	M2	LT	
4	IO_L59N_M4DQ15_4	M1	LT	
4	IO_L60P_M4DQ12_4	L3	LT	
4	IO_L60N_M4DQ13_4	L1	LT	
4	IO_L61P_M4UDQS_4	K2	LT	
4	IO_L61N_M4UDQSN_4	K1	LT	
4	IO_L62P_M4DQ10_4	L5	LT	
4	IO_L62N_M4DQ11_4	L4	LT	
4	IO_L63P_M4DQ8_4	M4	LT	
4	IO_L63N_M4DQ9_4	M3	LT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L64P_M4DQ0_4	H4	LT	
4	IO_L64N_M4DQ1_4	H3	LT	
4	IO_L65P_M4DQ2_4	J3	LT	
4	IO_L65N_M4DQ3_4	J1	LT	
4	IO_L66P_M4LDQS_4	J5	LT	
4	IO_L66N_M4LDQSN_4	J4	LT	
4	IO_L67P_M4DQ6_4	H2	LT	
4	IO_L67N_M4DQ7_4	H1	LT	
4	IO_L68P_M4DQ4_4	G3	LT	
4	IO_L68N_M4DQ5_4	G1	LT	
4	IO_L69P_M4UDM_4	K4	LT	
4	IO_L69N_M4LDM_4	K3	LT	
4	IO_L70P_M4RASN_4	C1	LT	
4	IO_L70N_M4CASN_4	B1	LT	
4	IO_L71P_M4A5_4	F2	LT	
4	IO_L71N_M4A6_4	F1	LT	
4	IO_L72P_M4A3_4	E5	LT	
4	IO_L72N_M4ODT_4	E4	LT	
4	IO_L73P_M4CLK_4	E3	LT	
4	IO_L73N_M4CLKN_4	E1	LT	
4	IO_L74P_M4A0_4	D4	LT	
4	IO_L74N_M4A1_4	D3	LT	
4	IO_L75P_M4BA0_4	D2	LT	
4	IO_L75N_M4BA1_4	D1	LT	
4	IO_L76P_M4A7_4	B3	LT	
4	IO_L76N_M4A2_4	A3	LT	
4	IO_L77P_M4WE_4	F4	LT	
4	IO_L77N_M4BA2_4	F3	LT	
4	IO_L78P_M4A10_4	D5	LT	
4	IO_L78N_M4A4_4	C5	LT	
4	IO_L79P_M4A8_4	B2	LT	
4	IO_L79N_M4A9_4	A2	LT	
4	IO_L80P_M4CKE_4	C4	LT	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L80N_M4A12_4	A4	LT	
4	IO_L81P_M4RESET_4	G5	LT	
4	IO_L81N_M4A11_4	G4	LT	
4	IO_L82P_M4A13_4	B5	LT	
4	IO_L82N_M4A14_4	A5	LT	
4	IO_L83P_4	J6	LT	
4	IO_L83N_VREF_4	H6	LT	
NA	GND	A1	NA	
NA	GND	A30	NA	
NA	GND	AA13	NA	
NA	GND	AA17	NA	
NA	GND	AA2	NA	
NA	GND	AA20	NA	
NA	GND	AA22	NA	
NA	GND	AA26	NA	
NA	GND	AB10	NA	
NA	GND	AB21	NA	
NA	GND	AB22	NA	
NA	GND	AB23	NA	
NA	GND	AB24	NA	
NA	GND	AB29	NA	
NA	GND	AB5	NA	
NA	GND	AC10	NA	
NA	GND	AC13	NA	
NA	GND	AC17	NA	
NA	GND	AC23	NA	
NA	GND	AC8	NA	
NA	GND	AE2	NA	
NA	GND	AF10	NA	
NA	GND	AF14	NA	
NA	GND	AF18	NA	
NA	GND	AF22	NA	
NA	GND	AF26	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	AF29	NA	
NA	GND	AF5	NA	
NA	GND	AH28	NA	
NA	GND	AJ13	NA	
NA	GND	AJ17	NA	
NA	GND	AJ21	NA	
NA	GND	AJ25	NA	
NA	GND	AJ5	NA	
NA	GND	AJ9	NA	
NA	GND	AK1	NA	
NA	GND	AK30	NA	
NA	GND	B10	NA	
NA	GND	B14	NA	
NA	GND	B18	NA	
NA	GND	B22	NA	
NA	GND	B26	NA	
NA	GND	B6	NA	
NA	GND	C28	NA	
NA	GND	C3	NA	
NA	GND	E13	NA	
NA	GND	E17	NA	
NA	GND	E2	NA	
NA	GND	E21	NA	
NA	GND	E25	NA	
NA	GND	E9	NA	
NA	GND	F29	NA	
NA	GND	F5	NA	
NA	GND	H12	NA	
NA	GND	H16	NA	
NA	GND	H20	NA	
NA	GND	H23	NA	
NA	GND	H8	NA	
NA	GND	H9	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	J18	NA	
NA	GND	J2	NA	
NA	GND	J22	NA	
NA	GND	J24	NA	
NA	GND	J26	NA	
NA	GND	J7	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K16	NA	
NA	GND	K18	NA	
NA	GND	K21	NA	
NA	GND	K22	NA	
NA	GND	K23	NA	
NA	GND	K29	NA	
NA	GND	K5	NA	
NA	GND	K7	NA	
NA	GND	K8	NA	
NA	GND	L10	NA	
NA	GND	L11	NA	
NA	GND	L13	NA	
NA	GND	L14	NA	
NA	GND	L17	NA	
NA	GND	L18	NA	
NA	GND	L21	NA	
NA	GND	L23	NA	
NA	GND	L9	NA	
NA	GND	M10	NA	
NA	GND	M13	NA	
NA	GND	M14	NA	
NA	GND	M17	NA	
NA	GND	M18	NA	
NA	GND	M21	NA	
NA	GND	M22	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	M8	NA	
NA	GND	N11	NA	
NA	GND	N12	NA	
NA	GND	N15	NA	
NA	GND	N16	NA	
NA	GND	N19	NA	
NA	GND	N2	NA	
NA	GND	N20	NA	
NA	GND	N22	NA	
NA	GND	N26	NA	
NA	GND	P11	NA	
NA	GND	P12	NA	
NA	GND	P15	NA	
NA	GND	P16	NA	
NA	GND	P19	NA	
NA	GND	P20	NA	
NA	GND	P29	NA	
NA	GND	P5	NA	
NA	GND	P9	NA	
NA	GND	R10	NA	
NA	GND	R13	NA	
NA	GND	R14	NA	
NA	GND	R17	NA	
NA	GND	R18	NA	
NA	GND	R8	NA	
NA	GND	T13	NA	
NA	GND	T14	NA	
NA	GND	T17	NA	
NA	GND	T18	NA	
NA	GND	T22	NA	
NA	GND	T23	NA	
NA	GND	U11	NA	
NA	GND	U12	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	U15	NA	
NA	GND	U16	NA	
NA	GND	U19	NA	
NA	GND	U2	NA	
NA	GND	U20	NA	
NA	GND	U21	NA	
NA	GND	U22	NA	
NA	GND	U26	NA	
NA	GND	U9	NA	
NA	GND	V11	NA	
NA	GND	V12	NA	
NA	GND	V15	NA	
NA	GND	V16	NA	
NA	GND	V19	NA	
NA	GND	V20	NA	
NA	GND	V22	NA	
NA	GND	V29	NA	
NA	GND	V5	NA	
NA	GND	W13	NA	
NA	GND	W14	NA	
NA	GND	W17	NA	
NA	GND	W18	NA	
NA	GND	W23	NA	
NA	GND	W8	NA	
NA	GND	Y11	NA	
NA	GND	Y13	NA	
NA	GND	Y14	NA	
NA	GND	Y17	NA	
NA	GND	Y18	NA	
NA	GND	Y21	NA	
NA	VCCINT	AA16	NA	
NA	VCCINT	K15	NA	
NA	VCCINT	K19	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	K20	NA	
NA	VCCINT	L12	NA	
NA	VCCINT	L15	NA	
NA	VCCINT	L16	NA	
NA	VCCINT	L19	NA	
NA	VCCINT	L20	NA	
NA	VCCINT	M11	NA	
NA	VCCINT	M12	NA	
NA	VCCINT	M15	NA	
NA	VCCINT	M16	NA	
NA	VCCINT	M19	NA	
NA	VCCINT	M20	NA	
NA	VCCINT	N13	NA	
NA	VCCINT	N14	NA	
NA	VCCINT	N17	NA	
NA	VCCINT	N18	NA	
NA	VCCINT	P13	NA	
NA	VCCINT	P14	NA	
NA	VCCINT	P17	NA	
NA	VCCINT	P18	NA	
NA	VCCINT	R11	NA	
NA	VCCINT	R12	NA	
NA	VCCINT	R15	NA	
NA	VCCINT	R16	NA	
NA	VCCINT	R19	NA	
NA	VCCINT	R20	NA	
NA	VCCINT	T10	NA	
NA	VCCINT	T11	NA	
NA	VCCINT	T12	NA	
NA	VCCINT	T15	NA	
NA	VCCINT	T16	NA	
NA	VCCINT	T19	NA	
NA	VCCINT	T20	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	U13	NA	
NA	VCCINT	U14	NA	
NA	VCCINT	U17	NA	
NA	VCCINT	U18	NA	
NA	VCCINT	V13	NA	
NA	VCCINT	V14	NA	
NA	VCCINT	V17	NA	
NA	VCCINT	V18	NA	
NA	VCCINT	W11	NA	
NA	VCCINT	W12	NA	
NA	VCCINT	W15	NA	
NA	VCCINT	W16	NA	
NA	VCCINT	W19	NA	
NA	VCCINT	W20	NA	
NA	VCCINT	Y12	NA	
NA	VCCINT	Y15	NA	
NA	VCCINT	Y16	NA	
NA	VCCINT	Y19	NA	
NA	VCCINT	Y20	NA	
NA	VCCAUX	K17	NA	
NA	VCCAUX	K9	NA	
NA	VCCAUX	L22	NA	
NA	VCCAUX	M25	NA	
NA	VCCAUX	N21	NA	
NA	VCCAUX	N6	NA	
NA	VCCAUX	P10	NA	
NA	VCCAUX	R9	NA	
NA	VCCAUX	T21	NA	
NA	VCCAUX	U10	NA	
NA	VCCAUX	V25	NA	
NA	VCCAUX	V6	NA	
NA	VCCAUX	AA21	NA	
NA	VCCAUX	AB13	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	AB17	NA	
NA	VCCAUX	AB9	NA	
NA	VCCAUX	AC24	NA	
NA	VCCAUX	AC7	NA	
NA	VCCAUX	AE11	NA	
NA	VCCAUX	AE21	NA	
NA	VCCAUX	F10	NA	
NA	VCCAUX	F20	NA	
NA	VCCAUX	H24	NA	
NA	VCCAUX	J23	NA	
NA	VCCAUX	J8	NA	
NA	VCCAUX	K13	NA	
0	VCCO_0	B12	NA	
0	VCCO_0	B16	NA	
0	VCCO_0	B20	NA	
0	VCCO_0	B24	NA	
0	VCCO_0	B8	NA	
0	VCCO_0	E11	NA	
0	VCCO_0	E15	NA	
0	VCCO_0	E19	NA	
0	VCCO_0	E23	NA	
0	VCCO_0	E7	NA	
0	VCCO_0	H10	NA	
0	VCCO_0	H14	NA	
0	VCCO_0	H18	NA	
0	VCCO_0	H22	NA	
0	VCCO_0	H7	NA	
0	VCCO_0	J16	NA	
0	VCCO_0	K11	NA	
1	VCCO_1	N23	NA	
1	VCCO_1	P21	NA	
1	VCCO_1	R23	NA	
1	VCCO_1	R26	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	VCCO_1	T29	NA	
1	VCCO_1	U23	NA	
1	VCCO_1	V21	NA	
1	VCCO_1	W26	NA	
1	VCCO_1	Y29	NA	
1	VCCO_1	AA23	NA	
1	VCCO_1	AC26	NA	
1	VCCO_1	AD29	NA	
1	VCCO_1	AH29	NA	
1	VCCO_1	AJ27	NA	
2	VCCO_2	AA14	NA	
2	VCCO_2	AA18	NA	
2	VCCO_2	AC11	NA	
2	VCCO_2	AC15	NA	
2	VCCO_2	AC19	NA	
2	VCCO_2	AC22	NA	
2	VCCO_2	AC9	NA	
2	VCCO_2	AF12	NA	
2	VCCO_2	AF16	NA	
2	VCCO_2	AF20	NA	
2	VCCO_2	AF24	NA	
2	VCCO_2	AF8	NA	
2	VCCO_2	AJ11	NA	
2	VCCO_2	AJ15	NA	
2	VCCO_2	AJ19	NA	
2	VCCO_2	AJ23	NA	
2	VCCO_2	AJ7	NA	
3	VCCO_3	AA8	NA	
3	VCCO_3	AC2	NA	
3	VCCO_3	AD5	NA	
3	VCCO_3	AG2	NA	
3	VCCO_3	AJ3	NA	
3	VCCO_3	L8	NA	

Table 2-16: FG(G)900 Package—LX150 (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	VCCO_3	M9	NA	
3	VCCO_3	P8	NA	
3	VCCO_3	R2	NA	
3	VCCO_3	T5	NA	
3	VCCO_3	U8	NA	
3	VCCO_3	W2	NA	
3	VCCO_3	Y10	NA	
3	VCCO_3	Y5	NA	
4	VCCO_4	K6	NA	
4	VCCO_4	L2	NA	
4	VCCO_4	M5	NA	
4	VCCO_4	B4	NA	
4	VCCO_4	C2	NA	
4	VCCO_4	G2	NA	
4	VCCO_4	H5	NA	
5	VCCO_5	K24	NA	
5	VCCO_5	L26	NA	
5	VCCO_5	M29	NA	
5	VCCO_5	B28	NA	
5	VCCO_5	D29	NA	
5	VCCO_5	G26	NA	
5	VCCO_5	H29	NA	
5	VCCO_5	J25	NA	

FG(G)900 Package—LX100T and LX150T

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 and bank 5 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 and bank 4 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-17: FG(G)900 Package—LX100T and LX150T

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	H9	TL	
0	IO_L1N_VREF_0	G9	TL	
0	IO_L2P_0	F6	TL	
0	IO_L2N_0	E6	TL	
0	IO_L3P_0	J8	TL	
0	IO_L3N_0	H8	TL	
0	IO_L4P_0	D6	TL	
0	IO_L4N_0	C6	TL	
0	IO_L5P_0	H7	TL	
0	IO_L5N_0	G7	TL	
0	IO_L6P_0	E7	TL	
0	IO_L6N_0	D7	TL	
0	IO_L7P_0	M10	TL	
0	IO_L7N_0	L10	TL	
0	IO_L8P_0	B6	TL	
0	IO_L8N_VREF_0	A6	TL	
0	IO_L9P_0	K10	TL	
0	IO_L9N_0	J10	TL	
0	IO_L10P_0	F8	TL	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L10N_0	E8	TL	
0	IO_L11P_0	L11	TL	
0	IO_L11N_0	K11	TL	
0	IO_L12P_0	D8	TL	LX100T
0	IO_L12N_0	C8	TL	LX100T
0	IO_L13P_0	B7	TL	
0	IO_L13N_0	A7	TL	
0	IO_L14P_0	G10	TL	LX100T
0	IO_L14N_0	F10	TL	LX100T
0	IO_L15P_0	L12	TL	
0	IO_L15N_0	K12	TL	
0	IO_L16P_0	F9	TL	LX100T
0	IO_L16N_0	E9	TL	LX100T
0	IO_L17P_0	J12	TL	
0	IO_L17N_0	H12	TL	
0	IO_L18P_0	F11	TL	LX100T
0	IO_L18N_0	E11	TL	LX100T
0	IO_L19P_0	J13	TL	
0	IO_L19N_0	H13	TL	
0	IO_L20P_0	H11	TL	
0	IO_L20N_0	G11	TL	
0	IO_L21P_0	M13	TL	
0	IO_L21N_0	L13	TL	
0	IO_L22P_0	G12	TL	LX100T
0	IO_L22N_0	F12	TL	LX100T
0	IO_L23P_0	L14	TL	
0	IO_L23N_0	K14	TL	
0	IO_L24P_0	F13	TL	LX100T
0	IO_L24N_0	E13	TL	LX100T
0	IO_L25P_0	M15	TL	
0	IO_L25N_0	K15	TL	
0	IO_L26P_0	G14	TL	LX100T
0	IO_L26N_0	F14	TL	LX100T

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L32P_0	J14	TL	
0	IO_L32N_0	H14	TL	
0	IO_L33P_0	F15	TL	
0	IO_L33N_0	E15	TL	
0	IO_L34P_GCLK19_0	H15	TL	
0	IO_L34N_GCLK18_0	G15	TL	
0	IO_L35P_GCLK17_0	B15	TL	
0	IO_L35N_GCLK16_0	A15	TL	
0	IO_L36P_GCLK15_0	C16	TR	
0	IO_L36N_GCLK14_0	A16	TR	
0	IO_L37P_GCLK13_0	E16	TR	
0	IO_L37N_GCLK12_0	D16	TR	
0	IO_L38P_0	B17	TR	
0	IO_L38N_VREF_0	A17	TR	
0	IO_L43P_0	L17	TR	
0	IO_L43N_0	K17	TR	
0	IO_L44P_0	H17	TR	
0	IO_L44N_0	G17	TR	
0	IO_L45P_0	H16	TR	
0	IO_L45N_0	G16	TR	
0	IO_L46P_0	G18	TR	
0	IO_L46N_0	F18	TR	
0	IO_L47P_0	M18	TR	
0	IO_L47N_0	L18	TR	
0	IO_L48P_0	F17	TR	LX100T
0	IO_L48N_0	E17	TR	LX100T
0	IO_L49P_0	K19	TR	
0	IO_L49N_0	J19	TR	
0	IO_L50P_0	F19	TR	
0	IO_L50N_0	E19	TR	
0	IO_L51P_0	M19	TR	
0	IO_L51N_0	L19	TR	
0	IO_L52P_0	H19	TR	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L52N_0	G19	TR	
0	IO_L53P_0	J18	TR	
0	IO_L53N_0	H18	TR	
0	IO_L54P_0	G20	TR	
0	IO_L54N_0	F20	TR	
0	IO_L55P_0	K20	TR	
0	IO_L55N_0	J20	TR	
0	IO_L56P_0	F21	TR	LX100T
0	IO_L56N_0	E21	TR	LX100T
0	IO_L57P_0	M20	TR	LX100T
0	IO_L57N_0	L20	TR	LX100T
0	IO_L58P_0	G22	TR	LX100T
0	IO_L58N_0	F22	TR	LX100T
0	IO_L59P_0	L21	TR	
0	IO_L59N_0	K21	TR	
0	IO_L60P_0	F23	TR	
0	IO_L60N_0	E23	TR	
0	IO_L61P_0	H21	TR	
0	IO_L61N_0	G21	TR	
0	IO_L62P_0	F24	TR	
0	IO_L62N_VREF_0	E24	TR	
0	IO_L63P_SCP7_0	B25	TR	
0	IO_L63N_SCP6_0	A25	TR	
0	IO_L64P_SCP5_0	D24	TR	
0	IO_L64N_SCP4_0	C24	TR	
0	IO_L65P_SCP3_0	J22	TR	
0	IO_L65N_SCP2_0	H22	TR	
0	IO_L66P_SCP1_0	E25	TR	
0	IO_L66N_SCP0_0	D25	TR	
NA	TCK	H23	NA	
NA	TDI	J24	NA	
101	MGTTXN0_101	A9	NA	
101	MGTTXP0_101	B9	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
101	MGTAVCCPLL0_101	B14	NA	
101	MGTREFCLK0N_101	A13	NA	
101	MGTREFCLK0P_101	B13	NA	
101	MGTRXN0_101	C10	NA	
101	MGTRXP0_101	D10	NA	
101	MGTRREF_101	E12	NA	
101	MGTRXN1_101	C12	NA	
101	MGTAVTTRCAL_101	E14	NA	
101	MGTRXP1_101	D12	NA	
101	MGTAVCCPLL1_101	C15	NA	
101	MGTREFCLK1N_101	C14	NA	
101	MGTREFCLK1P_101	D14	NA	
101	MGTTXN1_101	A11	NA	
101	MGTTXP1_101	B11	NA	
123	MGTTXN0_123	A21	NA	
123	MGTTXP0_123	B21	NA	
123	MGTAVCCPLL0_123	C17	NA	
123	MGTREFCLK0N_123	C18	NA	
123	MGTREFCLK0P_123	D18	NA	
123	MGTRXN0_123	C20	NA	
123	MGTRXP0_123	D20	NA	
123	MGTRXN1_123	C22	NA	
123	MGTRXP1_123	D22	NA	
123	MGTAVCCPLL1_123	B18	NA	
123	MGTREFCLK1N_123	A19	NA	
123	MGTREFCLK1P_123	B19	NA	
123	MGTTXN1_123	A23	NA	
123	MGTTXP1_123	B23	NA	
NA	TMS	K25	NA	
NA	TDO	H25	NA	
5	IO_L1P_A25_5	G25	RT	
5	IO_L1N_A24_VREF_5	F25	RT	
5	IO_L2P_M5A13_5	A28	RT	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L2N_M5A14_5	A29	RT	
5	IO_L3P_M5RESET_5	C26	RT	
5	IO_L3N_M5A11_5	A26	RT	
5	IO_L4P_M5CKE_5	B29	RT	
5	IO_L4N_M5A12_5	B30	RT	
5	IO_L5P_M5A8_5	B27	RT	
5	IO_L5N_M5A9_5	A27	RT	
5	IO_L6P_M5A10_5	F26	RT	
5	IO_L6N_M5A4_5	F27	RT	
5	IO_L7P_M5WE_5	E26	RT	
5	IO_L7N_M5BA2_5	D26	RT	
5	IO_L8P_M5A7_5	C29	RT	
5	IO_L8N_M5A2_5	C30	RT	
5	IO_L9P_M5BA0_5	D27	RT	
5	IO_L9N_M5BA1_5	C27	RT	
5	IO_L10P_M5A0_5	D28	RT	
5	IO_L10N_M5A1_5	D30	RT	
5	IO_L11P_M5CLK_5	E27	RT	
5	IO_L11N_M5CLKN_5	E28	RT	
5	IO_L12P_M5A3_5	E29	RT	
5	IO_L12N_M5ODT_5	E30	RT	
5	IO_L13P_M5A5_5	H26	RT	
5	IO_L13N_M5A6_5	H27	RT	
5	IO_L14P_M5RASN_5	K26	RT	
5	IO_L14N_M5CASN_5	K27	RT	
5	IO_L15P_M5UDM_5	J27	RT	
5	IO_L15N_M5LDM_5	J28	RT	
5	IO_L16P_M5DQ4_5	G27	RT	
5	IO_L16N_M5DQ5_5	G28	RT	
5	IO_L17P_M5DQ6_5	F28	RT	
5	IO_L17N_M5DQ7_5	F30	RT	
5	IO_L18P_M5LDQS_5	J29	RT	
5	IO_L18N_M5LDQSN_5	J30	RT	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
5	IO_L19P_M5DQ2_5	G29	RT	
5	IO_L19N_M5DQ3_5	G30	RT	
5	IO_L20P_M5DQ0_5	H28	RT	
5	IO_L20N_M5DQ1_5	H30	RT	
5	IO_L21P_M5DQ8_5	L27	RT	
5	IO_L21N_M5DQ9_5	L28	RT	
5	IO_L22P_M5DQ10_5	L29	RT	
5	IO_L22N_M5DQ11_5	L30	RT	
5	IO_L23P_M5UDQS_5	K28	RT	
5	IO_L23N_M5UDQSN_5	K30	RT	
5	IO_L24P_M5DQ12_5	M26	RT	
5	IO_L24N_M5DQ13_5	M27	RT	
5	IO_L25P_M5DQ14_5	M28	RT	
5	IO_L25N_M5DQ15_5	M30	RT	
5	IO_L26P_5	N24	RT	
5	IO_L26N_VREF_5	N25	RT	
5	IO_L27P_5	L24	RT	
5	IO_L27N_5	L25	RT	
1	IO_L28P_1	M23	RT	
1	IO_L28N_VREF_1	M24	RT	
1	IO_L29P_A23_M1A13_1	N29	RT	
1	IO_L29N_A22_M1A14_1	N30	RT	
1	IO_L30P_A21_M1RESET_1	N27	RT	
1	IO_L30N_A20_M1A11_1	N28	RT	
1	IO_L31P_A19_M1CKE_1	P28	RT	
1	IO_L31N_A18_M1A12_1	P30	RT	
1	IO_L32P_A17_M1A8_1	P26	RT	
1	IO_L32N_A16_M1A9_1	P27	RT	
1	IO_L33P_A15_M1A10_1	R29	RT	
1	IO_L33N_A14_M1A4_1	R30	RT	
1	IO_L34P_A13_M1WE_1	R27	RT	
1	IO_L34N_A12_M1BA2_1	R28	RT	
1	IO_L35P_A11_M1A7_1	T26	RT	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L35N_A10_M1A2_1	T27	RT	
1	IO_L36P_A9_M1BA0_1	T28	RT	
1	IO_L36N_A8_M1BA1_1	T30	RT	
1	IO_L37P_A7_M1A0_1	U29	RT	
1	IO_L37N_A6_M1A1_1	U30	RT	
1	IO_L38P_A5_M1CLK_1	U27	RT	
1	IO_L38N_A4_M1CLKN_1	U28	RT	
1	IO_L39P_M1A3_1	V28	RT	
1	IO_L39N_M1ODT_1	V30	RT	
1	IO_L40P_GCLK11_M1A5_1	V26	RT	
1	IO_L40N_GCLK10_M1A6_1	V27	RT	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	W27	RT	
1	IO_L41N_GCLK8_M1CASN_1	W28	RT	
1	IO_L42P_GCLK7_M1UDM_1	AB28	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	AB30	RB	
1	IO_L43P_GCLK5_M1DQ4_1	W29	RB	
1	IO_L43N_GCLK4_M1DQ5_1	W30	RB	
1	IO_L44P_A3_M1DQ6_1	Y28	RB	
1	IO_L44N_A2_M1DQ7_1	Y30	RB	
1	IO_L45P_A1_M1LDQS_1	AA29	RB	
1	IO_L45N_A0_M1LDQSN_1	AA30	RB	
1	IO_L46P_FCS_B_M1DQ2_1	AA27	RB	
1	IO_L46N_FOE_B_M1DQ3_1	AA28	RB	
1	IO_L47P_FWE_B_M1DQ0_1	Y26	RB	
1	IO_L47N_LDC_M1DQ1_1	Y27	RB	
1	IO_L48P_HDC_M1DQ8_1	AD28	RB	
1	IO_L48N_M1DQ9_1	AD30	RB	
1	IO_L49P_M1DQ10_1	AC27	RB	
1	IO_L49N_M1DQ11_1	AC28	RB	
1	IO_L50P_M1UDQS_1	AC29	RB	
1	IO_L50N_M1UDQSN_1	AC30	RB	
1	IO_L51P_M1DQ12_1	AE29	RB	
1	IO_L51N_M1DQ13_1	AE30	RB	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L52P_M1DQ14_1	AE27	RB	
1	IO_L52N_M1DQ15_1	AE28	RB	
1	IO_L53P_1	W24	RB	
1	IO_L53N_VREF_1	W25	RB	
1	IO_L54P_1	R21	RB	
1	IO_L54N_1	R22	RB	
1	IO_L55P_1	AF28	RB	
1	IO_L55N_1	AF30	RB	
1	IO_L56P_1	P22	RB	
1	IO_L56N_1	P23	RB	
1	IO_L57P_1	AG29	RB	
1	IO_L57N_1	AG30	RB	
1	IO_L58P_1	P24	RB	
1	IO_L58N_1	P25	RB	
1	IO_L59P_1	AH30	RB	
1	IO_L59N_1	AJ30	RB	
1	IO_L60P_1	R24	RB	
1	IO_L60N_1	R25	RB	
1	IO_L61P_1	AJ29	RB	
1	IO_L61N_1	AK29	RB	
1	IO_L62P_1	T24	RB	
1	IO_L62N_1	T25	RB	
1	IO_L63P_1	AJ28	RB	
1	IO_L63N_1	AK28	RB	
1	IO_L64P_1	U24	RB	
1	IO_L64N_1	U25	RB	
1	IO_L65P_1	AG27	RB	
1	IO_L65N_1	AG28	RB	
1	IO_L66P_1	V23	RB	
1	IO_L66N_1	V24	RB	
1	IO_L67P_1	AD26	RB	
1	IO_L67N_1	AD27	RB	
1	IO_L68P_1	W21	RB	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	IO_L68N_1	W22	RB	
1	IO_L69P_1	AH27	RB	
1	IO_L69N_VREF_1	AK27	RB	
1	IO_L70P_1	Y22	RB	
1	IO_L70N_1	Y23	RB	
1	IO_L71P_1	AE25	RB	
1	IO_L71N_1	AE26	RB	
1	IO_L72P_1	Y24	RB	
1	IO_L72N_1	Y25	RB	
1	IO_L73P_1	AG26	RB	
1	IO_L73N_1	AH26	RB	
1	IO_L74P_AWAKE_1	AA24	RB	
1	IO_L74N_DOUT_BUSY_1	AA25	RB	
NA	VFS	AF27	NA	
NA	RFUSE	AB27	NA	
NA	VBATT	AB26	NA	
NA	SUSPEND	AB25	NA	
2	CMPCS_B_2	AC25	NA	
2	DONE_2	AD25	NA	
2	IO_L1P_CCLK_2	AJ26	BR	
2	IO_L1N_M0_CPMISO_2	AK26	BR	
2	IO_L2P_CMPCLK_2	AC24	BR	
2	IO_L2N_CPMOSI_2	AD24	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	AJ25	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	AK25	BR	
2	IO_L4P_2	AB23	BR	
2	IO_L4N_VREF_2	AC23	BR	
2	IO_L5P_2	AE24	BR	
2	IO_L5N_2	AF24	BR	
2	IO_L6P_2	AA22	BR	
2	IO_L6N_2	AC22	BR	
2	IO_L7P_2	AE23	BR	
2	IO_L7N_2	AF23	BR	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L8P_2	AB21	BR	
2	IO_L8N_2	AC21	BR	
2	IO_L9P_2	AD22	BR	
2	IO_L9N_2	AE22	BR	
2	IO_L10P_2	Y21	BR	
2	IO_L10N_2	AA21	BR	
2	IO_L11P_2	AF25	BR	
2	IO_L11N_2	AG25	BR	
2	IO_L12P_D1_MISO2_2	AB20	BR	
2	IO_L12N_D2_MISO3_2	AC20	BR	
2	IO_L13P_M1_2	AG24	BR	
2	IO_L13N_D10_2	AH24	BR	
2	IO_L14P_D11_2	AC19	BR	
2	IO_L14N_D12_2	AD19	BR	
2	IO_L15P_2	AE21	BR	
2	IO_L15N_2	AF21	BR	
2	IO_L16P_2	AA18	BR	
2	IO_L16N_VREF_2	AB18	BR	
2	IO_L17P_2	AD20	BR	
2	IO_L17N_2	AE20	BR	
2	IO_L18P_2	W20	BR	
2	IO_L18N_2	Y20	BR	
2	IO_L19P_2	AE19	BR	
2	IO_L19N_2	AF19	BR	
2	IO_L20P_2	AA19	BR	
2	IO_L20N_2	AB19	BR	
2	IO_L21P_2	AD18	BR	LX100T
2	IO_L21N_2	AE18	BR	LX100T
2	IO_L22P_2	W19	BR	LX100T
2	IO_L22N_2	Y19	BR	LX100T
2	IO_L23P_2	AB17	BR	LX100T
2	IO_L23N_2	AD17	BR	LX100T
2	IO_L28P_2	AE17	BR	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L28N_2	AF17	BR	
2	IO_L29P_GCLK3_2	AC16	BR	
2	IO_L29N_GCLK2_2	AD16	BR	
2	IO_L30P_GCLK1_D13_2	AF16	BR	
2	IO_L30N_GCLK0_USERCLK_2	AG16	BR	
2	IO_L31P_GCLK31_D14_2	AH16	BL	
2	IO_L31N_GCLK30_D15_2	AK16	BL	
2	IO_L32P_GCLK29_2	AJ17	BL	
2	IO_L32N_GCLK28_2	AK17	BL	
2	IO_L33P_2	Y17	BL	
2	IO_L33N_2	AA17	BL	
2	IO_L34P_2	AJ15	BL	
2	IO_L34N_2	AK15	BL	
2	IO_L40P_2	AB14	BL	LX100T
2	IO_L40N_2	AC14	BL	LX100T
2	IO_L41P_2	AD14	BL	
2	IO_L41N_VREF_2	AE14	BL	
2	IO_L42P_2	Y14	BL	
2	IO_L42N_2	AA14	BL	
2	IO_L43P_2	AE15	BL	
2	IO_L43N_2	AF15	BL	
2	IO_L44P_2	AC15	BL	
2	IO_L44N_2	AD15	BL	
2	IO_L45P_2	AD12	BL	
2	IO_L45N_2	AE12	BL	
2	IO_L46P_2	Y15	BL	
2	IO_L46N_2	AA15	BL	
2	IO_L47P_2	AE13	BL	
2	IO_L47N_2	AF13	BL	
2	IO_L48P_D7_2	AB13	BL	
2	IO_L48N_RDWR_B_VREF_2	AC13	BL	
2	IO_L49P_D3_2	AE11	BL	
2	IO_L49N_D4_2	AF11	BL	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
2	IO_L50P_2	Y16	BL	
2	IO_L50N_2	AB16	BL	
2	IO_L51P_2	AC11	BL	
2	IO_L51N_2	AD11	BL	
2	IO_L52P_2	W14	BL	
2	IO_L52N_2	Y13	BL	
2	IO_L53P_2	AD10	BL	LX100T
2	IO_L53N_2	AE10	BL	LX100T
2	IO_L54P_2	AB12	BL	LX100T
2	IO_L54N_2	AC12	BL	LX100T
2	IO_L55P_2	AG8	BL	LX100T
2	IO_L55N_2	AH8	BL	LX100T
2	IO_L56P_2	W12	BL	LX100T
2	IO_L56N_2	Y12	BL	LX100T
2	IO_L57P_2	AE9	BL	
2	IO_L57N_2	AF9	BL	
2	IO_L58P_2	AA11	BL	LX100T
2	IO_L58N_2	AB11	BL	LX100T
2	IO_L59P_2	AF7	BL	
2	IO_L59N_2	AG7	BL	
2	IO_L60P_2	AB10	BL	LX100T
2	IO_L60N_2	AB9	BL	LX100T
2	IO_L61P_2	AC9	BL	
2	IO_L61N_VREF_2	AD9	BL	
2	IO_L62P_D5_2	AH7	BL	
2	IO_L62N_D6_2	AK7	BL	
2	IO_L63P_2	AD8	BL	
2	IO_L63N_2	AE8	BL	
2	IO_L64P_D8_2	AG6	BL	
2	IO_L64N_D9_2	AH6	BL	
2	IO_L65P_INIT_B_2	AJ6	BL	
2	IO_L65N_CSO_B_2	AK6	BL	
2	PROGRAM_B_2	AB8	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
267	MGTTXP1_267	AJ23	NA	
267	MGTTXN1_267	AK23	NA	
267	MGTAVCCPLL1_267	AJ18	NA	
267	MGTREFCLK1P_267	AJ19	NA	
267	MGTREFCLK1N_267	AK19	NA	
267	MGTRXP1_267	AG22	NA	
267	MGTRXN1_267	AH22	NA	
267	MGTRXP0_267	AG20	NA	
267	MGTRXN0_267	AH20	NA	
267	MGTAVCCPLL0_267	AH17	NA	
267	MGTREFCLK0P_267	AG18	NA	
267	MGTREFCLK0N_267	AH18	NA	
267	MGTTXP0_267	AJ21	NA	
267	MGTTXN0_267	AK21	NA	
245	MGTTXP1_245	AJ11	NA	
245	MGTTXN1_245	AK11	NA	
245	MGTAVCCPLL1_245	AH15	NA	
245	MGTREFCLK1P_245	AG14	NA	
245	MGTREFCLK1N_245	AH14	NA	
245	MGTRXP1_245	AG12	NA	
245	MGTAVTTRCAL_245	AF14	NA	
245	MGTRXN1_245	AH12	NA	
245	MGTREF_245	AF12	NA	
245	MGTRXP0_245	AG10	NA	
245	MGTRXN0_245	AH10	NA	
245	MGTAVCCPLL0_245	AJ14	NA	
245	MGTREFCLK0P_245	AJ13	NA	
245	MGTREFCLK0N_245	AK13	NA	
245	MGTTXP0_245	AJ9	NA	
245	MGTTXN0_245	AK9	NA	
3	IO_L1P_3	AA10	LB	
3	IO_L1N_VREF_3	AA9	LB	
3	IO_L2P_3	AD7	LB	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L2N_3	AE7	LB	
3	IO_L3P_3	Y9	LB	
3	IO_L3N_3	Y8	LB	
3	IO_L4P_3	AE6	LB	
3	IO_L4N_3	AF6	LB	
3	IO_L5P_3	W11	LB	
3	IO_L5N_3	Y11	LB	
3	IO_L6P_3	AE5	LB	
3	IO_L6N_3	AG5	LB	
3	IO_L7P_3	T7	LB	
3	IO_L7N_3	T6	LB	
3	IO_L8P_3	AA7	LB	
3	IO_L8N_3	AA6	LB	
3	IO_L9P_3	AC6	LB	
3	IO_L9N_3	AD6	LB	
3	IO_L10P_3	AH5	LB	
3	IO_L10N_3	AK5	LB	
3	IO_L11P_3	W10	LB	
3	IO_L11N_3	W9	LB	
3	IO_L12P_3	AB7	LB	
3	IO_L12N_3	AB6	LB	
3	IO_L13P_3	W7	LB	
3	IO_L13N_3	W6	LB	
3	IO_L14P_3	AJ4	LB	
3	IO_L14N_3	AK4	LB	
3	IO_L15P_3	T9	LB	
3	IO_L15N_3	T8	LB	
3	IO_L16P_3	AH3	LB	
3	IO_L16N_3	AK3	LB	
3	IO_L17P_3	Y7	LB	
3	IO_L17N_VREF_3	Y6	LB	
3	IO_L18P_3	AJ2	LB	
3	IO_L18N_3	AK2	LB	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L19P_3	AE4	LB	
3	IO_L19N_3	AF4	LB	
3	IO_L20P_3	AF3	LB	
3	IO_L20N_3	AG3	LB	
3	IO_L21P_3	V8	LB	
3	IO_L21N_3	V7	LB	
3	IO_L22P_3	AH1	LB	
3	IO_L22N_3	AJ1	LB	
3	IO_L23P_3	V10	LB	
3	IO_L23N_3	V9	LB	
3	IO_L24P_3	AG4	LB	
3	IO_L24N_3	AH4	LB	
3	IO_L25P_3	N10	LB	
3	IO_L25N_3	N9	LB	
3	IO_L26P_3	AF2	LB	
3	IO_L26N_3	AH2	LB	
3	IO_L27P_3	R7	LB	
3	IO_L27N_3	R6	LB	
3	IO_L28P_3	AF1	LB	
3	IO_L28N_3	AG1	LB	
3	IO_L29P_3	U7	LB	
3	IO_L29N_3	U6	LB	
3	IO_L30P_3	AE3	LB	
3	IO_L30N_3	AE1	LB	
3	IO_L31P_3	N8	LB	
3	IO_L31N_VREF_3	N7	LB	
3	IO_L32P_M3DQ14_3	AC5	LB	
3	IO_L32N_M3DQ15_3	AC4	LB	
3	IO_L33P_M3DQ12_3	AD4	LB	
3	IO_L33N_M3DQ13_3	AD3	LB	
3	IO_L34P_M3UDQS_3	AB4	LB	
3	IO_L34N_M3UDQSN_3	AB3	LB	
3	IO_L35P_M3DQ10_3	AD2	LB	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L35N_M3DQ11_3	AD1	LB	
3	IO_L36P_M3DQ8_3	AC3	LB	
3	IO_L36N_M3DQ9_3	AC1	LB	
3	IO_L37P_M3DQ0_3	Y4	LB	
3	IO_L37N_M3DQ1_3	Y3	LB	
3	IO_L38P_M3DQ2_3	Y2	LB	
3	IO_L38N_M3DQ3_3	Y1	LB	
3	IO_L39P_M3LDQS_3	AA5	LB	
3	IO_L39N_M3LDQSN_3	AA4	LB	
3	IO_L40P_M3DQ6_3	W3	LB	
3	IO_L40N_M3DQ7_3	W1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	AA3	LB	
3	IO_L41N_GCLK26_M3DQ5_3	AA1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	AB2	LB	
3	IO_L42N_GCLK24_M3LDM_3	AB1	LB	
3	IO_L43P_GCLK23_M3RASN_3	W5	LT	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	W4	LT	
3	IO_L44P_GCLK21_M3A5_3	V4	LT	
3	IO_L44N_GCLK20_M3A6_3	V3	LT	
3	IO_L45P_M3A3_3	V2	LT	
3	IO_L45N_M3ODT_3	V1	LT	
3	IO_L46P_M3CLK_3	U5	LT	
3	IO_L46N_M3CLKN_3	U4	LT	
3	IO_L47P_M3A0_3	U3	LT	
3	IO_L47N_M3A1_3	U1	LT	
3	IO_L48P_M3BA0_3	T4	LT	
3	IO_L48N_M3BA1_3	T3	LT	
3	IO_L49P_M3A7_3	T2	LT	
3	IO_L49N_M3A2_3	T1	LT	
3	IO_L50P_M3WE_3	R5	LT	
3	IO_L50N_M3BA2_3	R4	LT	
3	IO_L51P_M3A10_3	R3	LT	
3	IO_L51N_M3A4_3	R1	LT	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
3	IO_L52P_M3A8_3	P4	LT	
3	IO_L52N_M3A9_3	P3	LT	
3	IO_L53P_M3CKE_3	N5	LT	
3	IO_L53N_M3A12_3	N4	LT	
3	IO_L54P_M3RESET_3	P2	LT	
3	IO_L54N_M3A11_3	P1	LT	
3	IO_L55P_M3A13_3	N3	LT	
3	IO_L55N_M3A14_3	N1	LT	
3	IO_L56P_3	P7	LT	
3	IO_L56N_3	P6	LT	
3	IO_L57P_3	M7	LT	
3	IO_L57N_VREF_3	M6	LT	
4	IO_L58P_4	L7	LT	
4	IO_L58N_VREF_4	L6	LT	
4	IO_L59P_M4DQ14_4	M2	LT	
4	IO_L59N_M4DQ15_4	M1	LT	
4	IO_L60P_M4DQ12_4	L3	LT	
4	IO_L60N_M4DQ13_4	L1	LT	
4	IO_L61P_M4UDQS_4	K2	LT	
4	IO_L61N_M4UDQSN_4	K1	LT	
4	IO_L62P_M4DQ10_4	L5	LT	
4	IO_L62N_M4DQ11_4	L4	LT	
4	IO_L63P_M4DQ8_4	M4	LT	
4	IO_L63N_M4DQ9_4	M3	LT	
4	IO_L64P_M4DQ0_4	H4	LT	
4	IO_L64N_M4DQ1_4	H3	LT	
4	IO_L65P_M4DQ2_4	J3	LT	
4	IO_L65N_M4DQ3_4	J1	LT	
4	IO_L66P_M4LDQS_4	J5	LT	
4	IO_L66N_M4LDQSN_4	J4	LT	
4	IO_L67P_M4DQ6_4	H2	LT	
4	IO_L67N_M4DQ7_4	H1	LT	
4	IO_L68P_M4DQ4_4	G3	LT	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	IO_L68N_M4DQ5_4	G1	LT	
4	IO_L69P_M4UDM_4	K4	LT	
4	IO_L69N_M4LDM_4	K3	LT	
4	IO_L70P_M4RASN_4	C1	LT	
4	IO_L70N_M4CASN_4	B1	LT	
4	IO_L71P_M4A5_4	F2	LT	
4	IO_L71N_M4A6_4	F1	LT	
4	IO_L72P_M4A3_4	E5	LT	
4	IO_L72N_M4ODT_4	E4	LT	
4	IO_L73P_M4CLK_4	E3	LT	
4	IO_L73N_M4CLKN_4	E1	LT	
4	IO_L74P_M4A0_4	D4	LT	
4	IO_L74N_M4A1_4	D3	LT	
4	IO_L75P_M4BA0_4	D2	LT	
4	IO_L75N_M4BA1_4	D1	LT	
4	IO_L76P_M4A7_4	B3	LT	
4	IO_L76N_M4A2_4	A3	LT	
4	IO_L77P_M4WE_4	F4	LT	
4	IO_L77N_M4BA2_4	F3	LT	
4	IO_L78P_M4A10_4	D5	LT	
4	IO_L78N_M4A4_4	C5	LT	
4	IO_L79P_M4A8_4	B2	LT	
4	IO_L79N_M4A9_4	A2	LT	
4	IO_L80P_M4CKE_4	C4	LT	
4	IO_L80N_M4A12_4	A4	LT	
4	IO_L81P_M4RESET_4	G5	LT	
4	IO_L81N_M4A11_4	G4	LT	
4	IO_L82P_M4A13_4	B5	LT	
4	IO_L82N_M4A14_4	A5	LT	
4	IO_L83P_4	J6	LT	
4	IO_L83N_VREF_4	H6	LT	
NA	GND	A1	NA	
NA	GND	A12	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	A14	NA	
NA	GND	A18	NA	
NA	GND	A20	NA	
NA	GND	A24	NA	
NA	GND	A30	NA	
NA	GND	A8	NA	
NA	GND	AA13	NA	
NA	GND	AA2	NA	
NA	GND	AA26	NA	
NA	GND	AB15	NA	
NA	GND	AB22	NA	
NA	GND	AB29	NA	
NA	GND	AB5	NA	
NA	GND	AC17	NA	
NA	GND	AC8	NA	
NA	GND	AE2	NA	
NA	GND	AF10	NA	
NA	GND	AF18	NA	
NA	GND	AF20	NA	
NA	GND	AF22	NA	
NA	GND	AF26	NA	
NA	GND	AF29	NA	
NA	GND	AF5	NA	
NA	GND	AG13	NA	
NA	GND	AG15	NA	
NA	GND	AG17	NA	
NA	GND	AG19	NA	
NA	GND	AH11	NA	
NA	GND	AH21	NA	
NA	GND	AH23	NA	
NA	GND	AH28	NA	
NA	GND	AH9	NA	
NA	GND	AJ10	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	AJ12	NA	
NA	GND	AJ20	NA	
NA	GND	AJ22	NA	
NA	GND	AJ24	NA	
NA	GND	AJ5	NA	
NA	GND	AJ8	NA	
NA	GND	AK1	NA	
NA	GND	AK12	NA	
NA	GND	AK14	NA	
NA	GND	AK18	NA	
NA	GND	AK20	NA	
NA	GND	AK24	NA	
NA	GND	AK30	NA	
NA	GND	AK8	NA	
NA	GND	B10	NA	
NA	GND	B12	NA	
NA	GND	B20	NA	
NA	GND	B22	NA	
NA	GND	B24	NA	
NA	GND	B26	NA	
NA	GND	B8	NA	
NA	GND	C11	NA	
NA	GND	C21	NA	
NA	GND	C23	NA	
NA	GND	C28	NA	
NA	GND	C3	NA	
NA	GND	C9	NA	
NA	GND	D13	NA	
NA	GND	D15	NA	
NA	GND	D17	NA	
NA	GND	D19	NA	
NA	GND	E10	NA	
NA	GND	E18	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	E2	NA	
NA	GND	E20	NA	
NA	GND	E22	NA	
NA	GND	F29	NA	
NA	GND	F5	NA	
NA	GND	F7	NA	
NA	GND	G24	NA	
NA	GND	J11	NA	
NA	GND	J16	NA	
NA	GND	J2	NA	
NA	GND	J21	NA	
NA	GND	J26	NA	
NA	GND	K16	NA	
NA	GND	K18	NA	
NA	GND	K22	NA	
NA	GND	K23	NA	
NA	GND	K29	NA	
NA	GND	K5	NA	
NA	GND	K7	NA	
NA	GND	K8	NA	
NA	GND	K9	NA	
NA	GND	L16	NA	
NA	GND	L23	NA	
NA	GND	L8	NA	
NA	GND	M12	NA	
NA	GND	M16	NA	
NA	GND	M22	NA	
NA	GND	M9	NA	
NA	GND	N13	NA	
NA	GND	N14	NA	
NA	GND	N17	NA	
NA	GND	N18	NA	
NA	GND	N2	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	N21	NA	
NA	GND	N22	NA	
NA	GND	N26	NA	
NA	GND	P10	NA	
NA	GND	P13	NA	
NA	GND	P14	NA	
NA	GND	P17	NA	
NA	GND	P18	NA	
NA	GND	P20	NA	
NA	GND	P29	NA	
NA	GND	P5	NA	
NA	GND	P8	NA	
NA	GND	R11	NA	
NA	GND	R12	NA	
NA	GND	R15	NA	
NA	GND	R16	NA	
NA	GND	R19	NA	
NA	GND	R20	NA	
NA	GND	R9	NA	
NA	GND	T10	NA	
NA	GND	T11	NA	
NA	GND	T12	NA	
NA	GND	T15	NA	
NA	GND	T16	NA	
NA	GND	T19	NA	
NA	GND	T20	NA	
NA	GND	T22	NA	
NA	GND	T23	NA	
NA	GND	U13	NA	
NA	GND	U14	NA	
NA	GND	U17	NA	
NA	GND	U18	NA	
NA	GND	U2	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	GND	U21	NA	
NA	GND	U22	NA	
NA	GND	U26	NA	
NA	GND	U9	NA	
NA	GND	V13	NA	
NA	GND	V14	NA	
NA	GND	V17	NA	
NA	GND	V18	NA	
NA	GND	V22	NA	
NA	GND	V29	NA	
NA	GND	V5	NA	
NA	GND	W16	NA	
NA	GND	W18	NA	
NA	GND	W8	NA	
NA	VCCAUX	AB24	NA	
NA	VCCAUX	AC7	NA	
NA	VCCAUX	AG23	NA	
NA	VCCAUX	AG9	NA	
NA	VCCAUX	D23	NA	
NA	VCCAUX	D9	NA	
NA	VCCAUX	G6	NA	
NA	VCCAUX	H24	NA	
NA	VCCAUX	J15	NA	
NA	VCCAUX	J23	NA	
NA	VCCAUX	J7	NA	
NA	VCCAUX	J9	NA	
NA	VCCAUX	L22	NA	
NA	VCCAUX	M11	NA	
NA	VCCAUX	M14	NA	
NA	VCCAUX	M25	NA	
NA	VCCAUX	N6	NA	
NA	VCCAUX	R10	NA	
NA	VCCAUX	T21	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCAUX	U10	NA	
NA	VCCAUX	V21	NA	
NA	VCCAUX	V25	NA	
NA	VCCAUX	V6	NA	
NA	VCCAUX	W13	NA	
NA	VCCAUX	W15	NA	
NA	VCCAUX	W17	NA	
NA	VCCAUX	Y18	NA	
NA	VCCINT	N11	NA	
NA	VCCINT	N12	NA	
NA	VCCINT	N15	NA	
NA	VCCINT	N16	NA	
NA	VCCINT	N19	NA	
NA	VCCINT	N20	NA	
NA	VCCINT	P11	NA	
NA	VCCINT	P12	NA	
NA	VCCINT	P15	NA	
NA	VCCINT	P16	NA	
NA	VCCINT	P19	NA	
NA	VCCINT	R13	NA	
NA	VCCINT	R14	NA	
NA	VCCINT	R17	NA	
NA	VCCINT	R18	NA	
NA	VCCINT	T13	NA	
NA	VCCINT	T14	NA	
NA	VCCINT	T17	NA	
NA	VCCINT	T18	NA	
NA	VCCINT	U11	NA	
NA	VCCINT	U12	NA	
NA	VCCINT	U15	NA	
NA	VCCINT	U16	NA	
NA	VCCINT	U19	NA	
NA	VCCINT	U20	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
NA	VCCINT	V11	NA	
NA	VCCINT	V12	NA	
NA	VCCINT	V15	NA	
NA	VCCINT	V16	NA	
NA	VCCINT	V19	NA	
NA	VCCINT	V20	NA	
0	VCCO_0	B16	NA	
0	VCCO_0	C25	NA	
0	VCCO_0	C7	NA	
0	VCCO_0	F16	NA	
0	VCCO_0	G13	NA	
0	VCCO_0	G23	NA	
0	VCCO_0	G8	NA	
0	VCCO_0	H10	NA	
0	VCCO_0	H20	NA	
0	VCCO_0	J17	NA	
0	VCCO_0	K13	NA	
0	VCCO_0	L15	NA	
0	VCCO_0	L9	NA	
0	VCCO_0	M17	NA	
0	VCCO_0	M21	NA	
1	VCCO_1	AA23	NA	
1	VCCO_1	AC26	NA	
1	VCCO_1	AD29	NA	
1	VCCO_1	AH29	NA	
1	VCCO_1	AJ27	NA	
1	VCCO_1	N23	NA	
1	VCCO_1	P21	NA	
1	VCCO_1	R23	NA	
1	VCCO_1	R26	NA	
1	VCCO_1	T29	NA	
1	VCCO_1	U23	NA	
1	VCCO_1	W23	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
1	VCCO_1	W26	NA	
1	VCCO_1	Y29	NA	
2	VCCO_2	AA12	NA	
2	VCCO_2	AA16	NA	
2	VCCO_2	AA20	NA	
2	VCCO_2	AC10	NA	
2	VCCO_2	AC18	NA	
2	VCCO_2	AD13	NA	
2	VCCO_2	AD21	NA	
2	VCCO_2	AD23	NA	
2	VCCO_2	AE16	NA	
2	VCCO_2	AF8	NA	
2	VCCO_2	AH25	NA	
2	VCCO_2	AJ16	NA	
2	VCCO_2	AJ7	NA	
3	VCCO_3	AA8	NA	
3	VCCO_3	AC2	NA	
3	VCCO_3	AD5	NA	
3	VCCO_3	AG2	NA	
3	VCCO_3	AJ3	NA	
3	VCCO_3	M8	NA	
3	VCCO_3	P9	NA	
3	VCCO_3	R2	NA	
3	VCCO_3	R8	NA	
3	VCCO_3	T5	NA	
3	VCCO_3	U8	NA	
3	VCCO_3	W2	NA	
3	VCCO_3	Y10	NA	
3	VCCO_3	Y5	NA	
4	VCCO_4	B4	NA	
4	VCCO_4	C2	NA	
4	VCCO_4	G2	NA	
4	VCCO_4	H5	NA	

Table 2-17: FG(G)900 Package—LX100T and LX150T (Cont'd)

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
4	VCCO_4	K6	NA	
4	VCCO_4	L2	NA	
4	VCCO_4	M5	NA	
5	VCCO_5	B28	NA	
5	VCCO_5	D29	NA	
5	VCCO_5	G26	NA	
5	VCCO_5	H29	NA	
5	VCCO_5	J25	NA	
5	VCCO_5	K24	NA	
5	VCCO_5	L26	NA	
5	VCCO_5	M29	NA	
101	MGTAVCC_101	C13	NA	
123	MGTAVCC_123	C19	NA	
245	MGTAVCC_245	AH13	NA	
267	MGTAVCC_267	AH19	NA	
101	MGTAVTTRX_101	D11	NA	
123	MGTAVTTRX_123	D21	NA	
245	MGTAVTTRX_245	AG11	NA	
267	MGTAVTTRX_267	AG21	NA	
101	MGTAVTTTX_101	A10	NA	
123	MGTAVTTTX_123	A22	NA	
245	MGTAVTTTX_245	AK10	NA	
267	MGTAVTTTX_267	AK22	NA	

Pinout and I/O Bank Diagrams

Summary

This chapter provides pinout diagrams for each Spartan-6 FPGA package/device combination.

The multi-function I/O pins in these diagrams are represented by symbols based on functionality, using the following precedence:

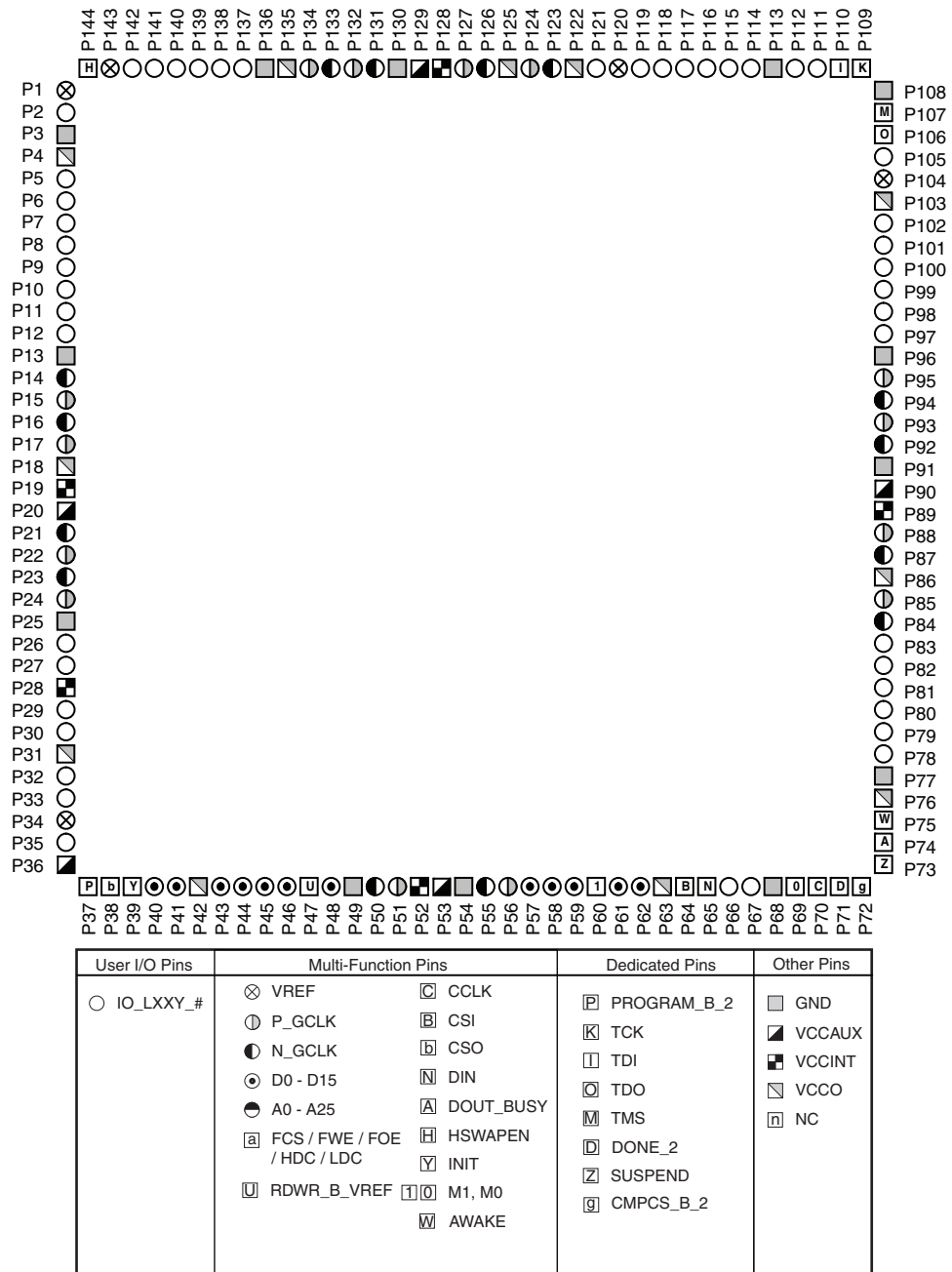
- VREF
- GCLK
- D0–D15
- A0–A25

For example, a pin description such as IO_L37N_GCLK12_0 is represented with an N_GCLK symbol, a pin description such as IO_L1N_VREF_0 is represented with a VREF symbol, and a pin description such as IO_L13N_D10_2 is represented with a D0–D15 symbol.

Table 3-1: Cross-Reference for Pinout and I/O Bank Diagrams

Device/ Package	TQG144	CPG196	CSG225	FT(G)256	CSG324	FG(G)484	CS(G)484	FG(G)676	FG(G)900
LX4	Page 274	Page 276	Page 277						
LX9	Page 274	Page 276	Page 278	Page 279	Page 280				
LX16		Page 276	Page 278	Page 279	Page 281				
LX25				Page 279	Page 282	Page 286			
LX25T					Page 283	Page 288			
LX45					Page 284	Page 290	Page 302	Page 312	
LX45T					Page 285	Page 300	Page 310		
LX75						Page 292	Page 304	Page 314	
LX75T						Page 294	Page 308	Page 316	
LX100						Page 296	Page 306	Page 318	
LX100T						Page 300	Page 310	Page 320	Page 326
LX150						Page 298	Page 306	Page 322	Page 328
LX150T						Page 300	Page 310	Page 324	Page 330

TQG144 Package—LX4 and LX9



UG385_c3_01_111909

Figure 3-1: TQG144 Package—LX4 and LX9 Pinout Diagram

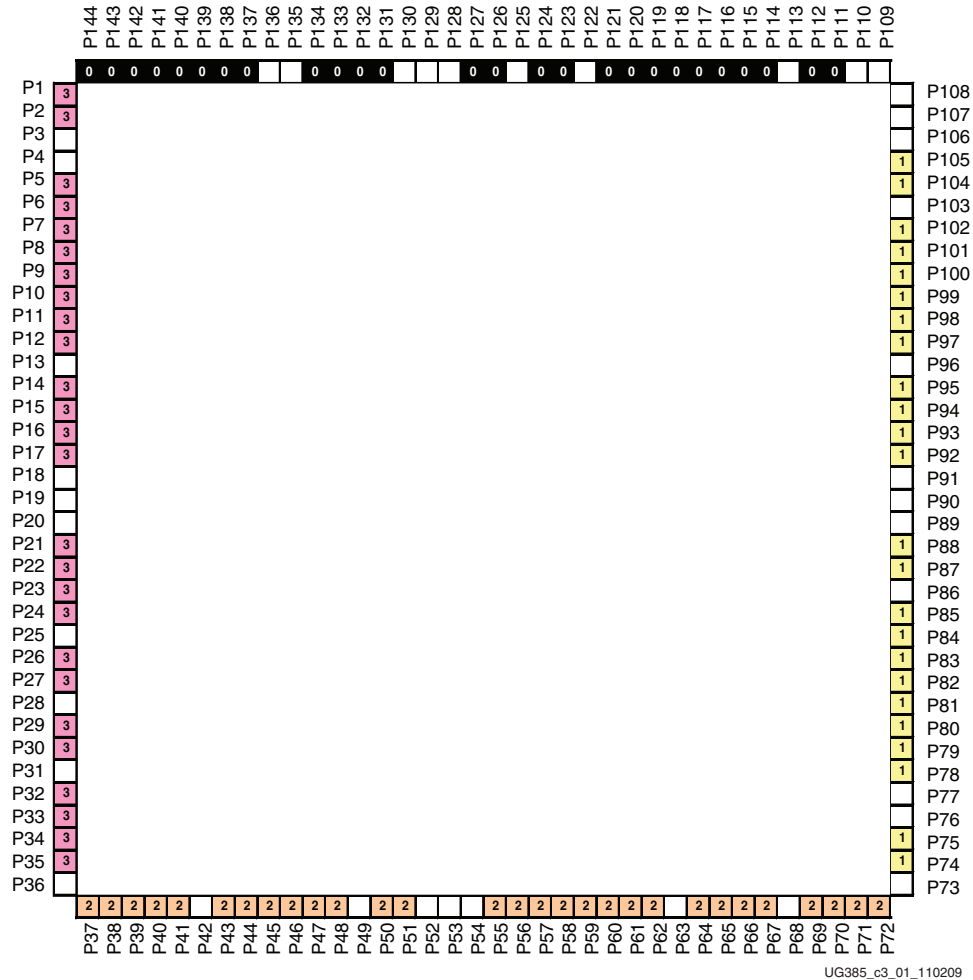
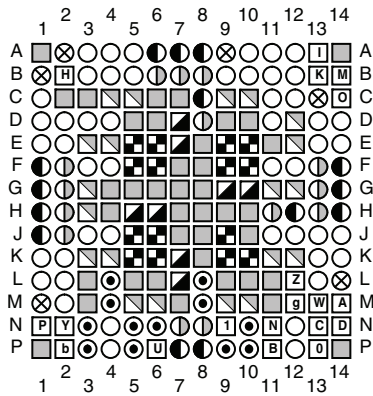


Figure 3-2: TQG144 Package—LX4 and LX9 I/O Bank Diagram

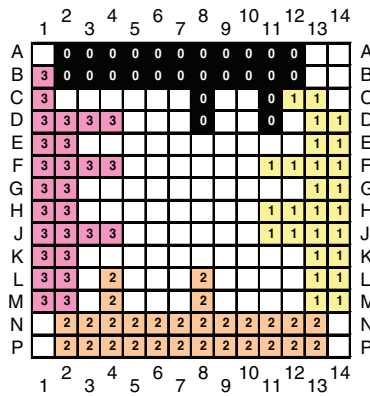
CPG196 Package—LX4, LX9, and LX16



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓜ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN Ⓨ INIT Ⓤ M1, M0 Ⓨ AWAKE	ⓐ PROGRAM_B_2 ⓑ TCK Ⓨ TDI ⓐ TDO ⓑ TMS Ⓨ DONE_2 ⓐ SUSPEND ⓑ CMPCS_B_2	■ GND ⓐ VCCAUX ⓑ VCCINT Ⓨ VCCO Ⓤ NC

UG385_c3_03_111909

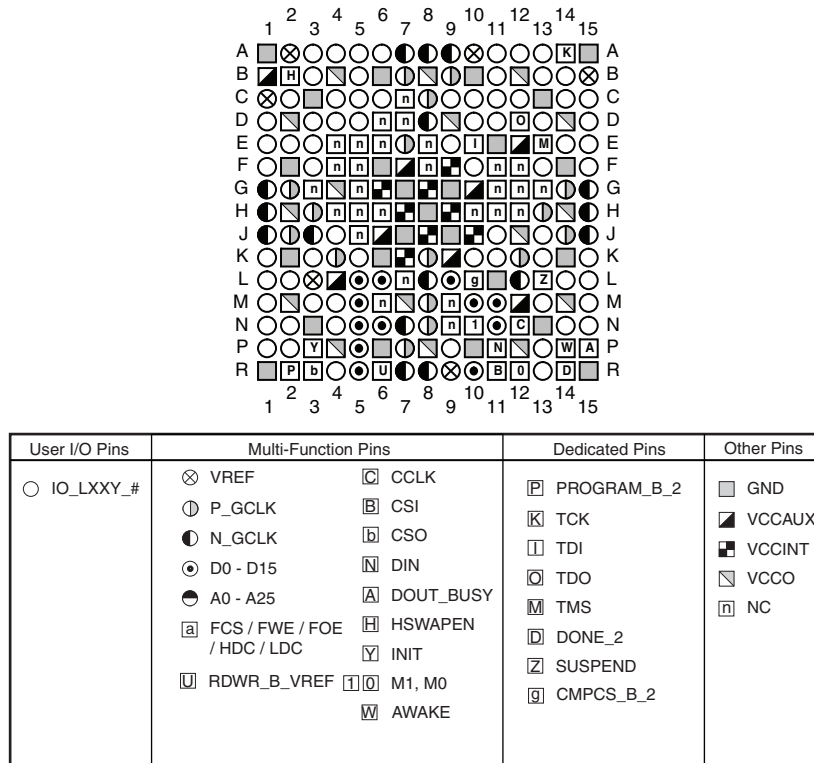
Figure 3-3: CPG196 Package—LX4, LX9, and LX16 Pinout Diagram



UG385_c3_04_110209

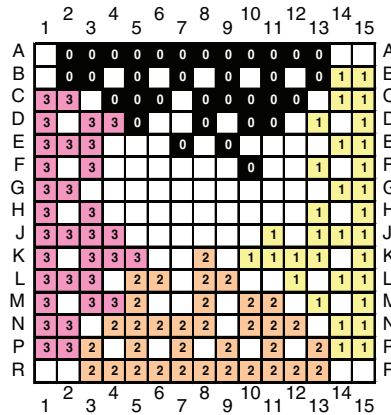
Figure 3-4: CPG196 Package—LX4, LX9, and LX16 I/O Bank Diagram

CSG225 Package—LX4



UG385_c3_05_111909

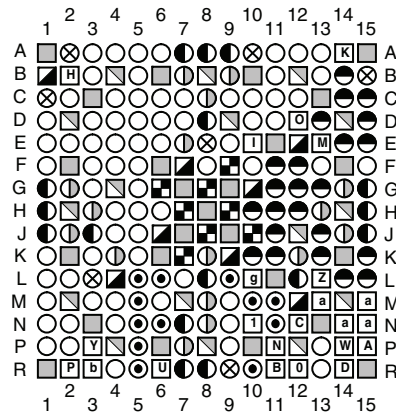
Figure 3-5: CSG225 Package—LX4 Pinout Diagram



UG385_c3_06_110209

Figure 3-6: CSG225 Package—LX4 I/O Bank Diagram

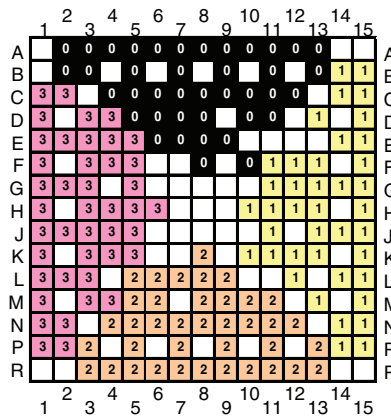
CSG225 Package—LX9 and LX16



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	Ⓜ PROGRAM_B_2	□ GND
	Ⓛ P_GCLK	Ⓚ TCK	▣ VCCAUX
	● N_GCLK	Ⓛ TDI	▣ VCCINT
	Ⓞ DO - D15	Ⓞ TDO	▣ VCCO
	Ⓢ A0 - A25	Ⓜ TMS	Ⓛ NC
	Ⓛ FCS / FWE / FOE / HDC / LDC	Ⓞ DONE_2	
	Ⓛ RDWR_B_VREF	Ⓛ SUSPEND	
	Ⓛ CCLK	Ⓛ CMPCS_B_2	
	Ⓛ CSI		
	Ⓛ CSO		
	Ⓛ DIN		
	Ⓛ DOUT_BUSY		
	Ⓛ HSWAPEN		
	Ⓛ INIT		
	Ⓛ M1, M0		
	Ⓛ AWAKE		

UG385_c3_07_111909

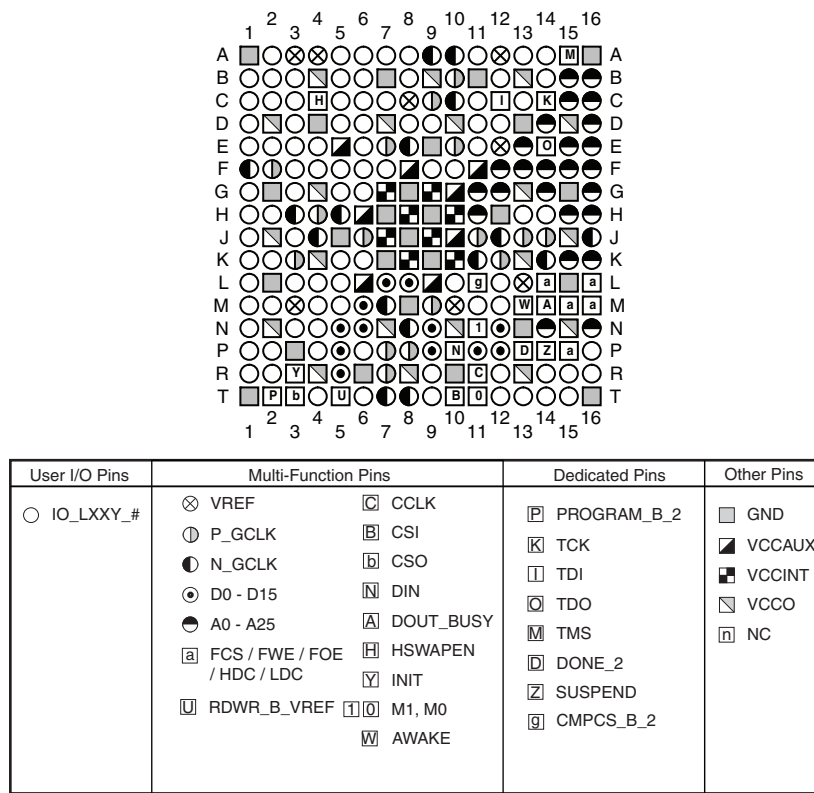
Figure 3-7: CSG225 Package—LX9 and LX16 Pinout Diagram



UG385_c3_08_110209

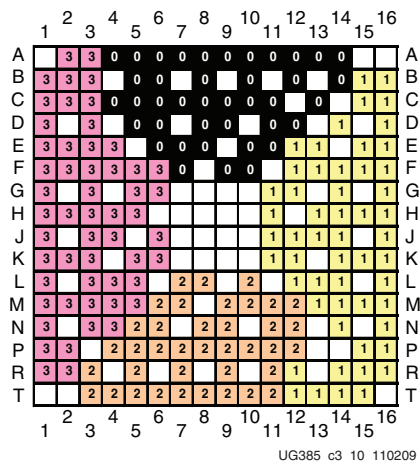
Figure 3-8: CSG225 Package—LX9 and LX16 I/O Bank Diagram

FT(G)256 Package—LX9, LX16, and LX25



UG385_c3_09_111909

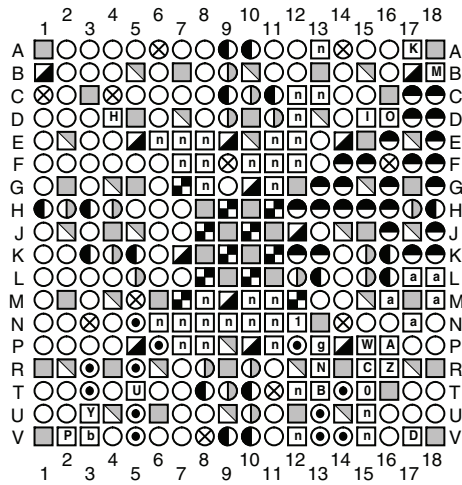
Figure 3-9: FT(G)256 Package—LX9, LX16, and LX25 Pinout Diagram



UG385_c3_10_110209

Figure 3-10: FT(G)256 Package—LX9, LX16, and LX25 I/O Bank Diagram

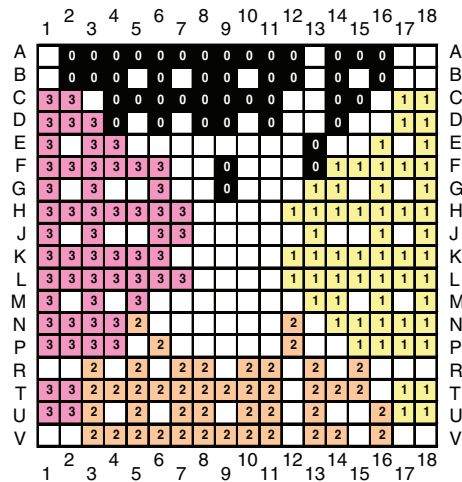
CSG324 Package—LX9



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK Ⓞ N_GCLK Ⓞ D0 - D15 Ⓞ A0 - A25 Ⓜ FCS / FWE / FOE / HDC / LDC Ⓞ RDWR_B_VREF	Ⓞ CCLK Ⓞ CSI Ⓞ CSO Ⓞ DIN Ⓞ DOUT_BUSY Ⓞ HSWAPEN Ⓞ INIT Ⓞ M1, M0 Ⓞ AWAKE	Ⓞ PROGRAM_B_2 Ⓞ TCK Ⓞ TDI Ⓞ TDO Ⓞ TMS Ⓞ DONE_2 Ⓞ SUSPEND Ⓞ CMPCS_B_2	Ⓞ GND Ⓞ VCCAUX Ⓞ VCCINT Ⓞ VCCO Ⓞ NC

UG385_c3_11_111909

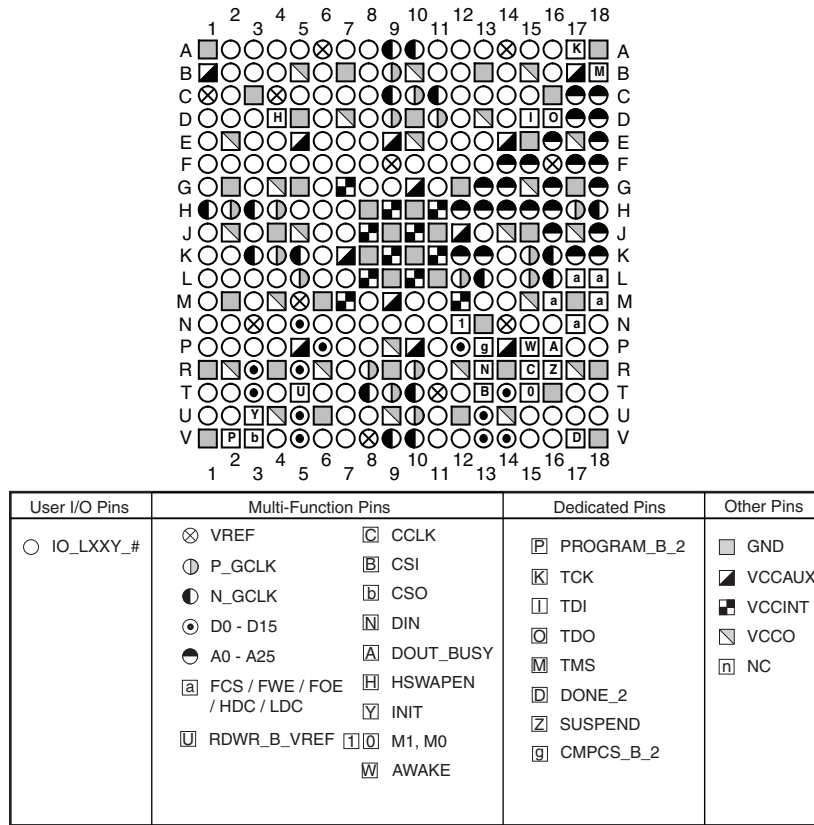
Figure 3-11: CSG324 Package—LX9 Pinout Diagram



UG385_c3_12_110209

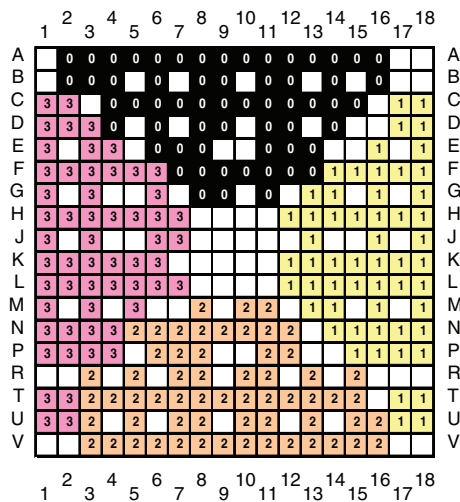
Figure 3-12: CSG324 Package—LX9 I/O Bank Diagram

CSG324 Package—LX16



UG385_c3_13_111909

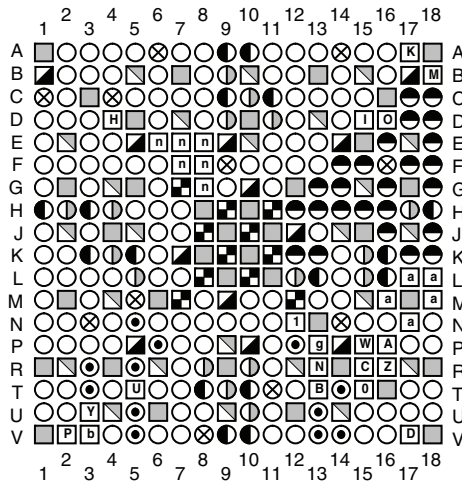
Figure 3-13: CSG324 Package—LX16 Pinout Diagram



UG385_c3_14_110209

Figure 3-14: CSG324 Package—LX16 I/O Bank Diagram

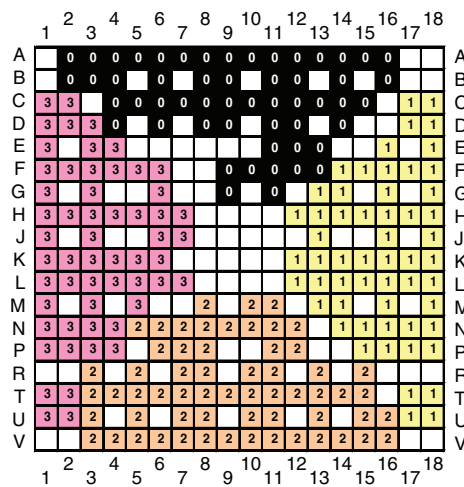
CSG324 Package—LX25



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 a FCS / FWE / FOE / HDC / LDC u RDWR_B_VREF	⊕ CCLK ⊖ CSI ⊖ CSO ⊖ DIN ⊖ DOUT_BUSY ⊖ HSWAPEN ⊖ INIT ⊖ M1, M0 ⊖ AWAKE	⊖ PROGRAM_B_2 ⊖ TCK ⊖ TDI ⊖ TDO ⊖ TMS ⊖ DONE_2 ⊖ SUSPEND ⊖ CMPCS_B_2	⊖ GND ⊖ VCCAUX ⊖ VCCINT ⊖ VCCO ⊖ NC

UG385_c3_15_111909

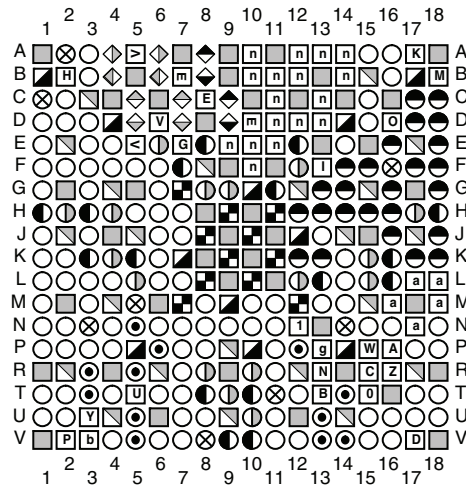
Figure 3-15: CSG324 Package—LX25 Pinout Diagram



UG385_c3_16_110209

Figure 3-16: CSG324 Package—LX25 I/O Bank Diagram

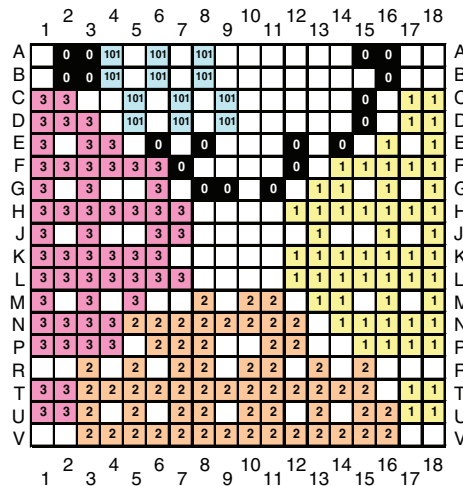
CSG324 Package—LX25T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK Ⓞ N_GCLK Ⓞ D0 - D15 Ⓞ A0 - A25 Ⓜ FCS / FWE / FOE / HDC / LDC Ⓞ RDWR_B_VREF	Ⓞ CCLK Ⓞ CSI Ⓞ CSO Ⓞ DIN Ⓞ DOUT_BUSY Ⓞ HSWAPEN Ⓞ INIT Ⓞ M1, M0 Ⓞ AWAKE	Ⓞ MGTAVCC Ⓞ MGTAVCCPLL Ⓞ MGTAVTTRX Ⓞ MGTAVTTRCAL Ⓞ MGTAVTTTX Ⓞ MGTREFCLK (P) Ⓞ MGTREFCLK (N) Ⓞ MGTRREF	Ⓞ PROGRAM_B_2 Ⓞ TCK Ⓞ TDI Ⓞ TDO Ⓞ TMS Ⓞ DONE_2 Ⓞ SUSPEND Ⓞ CMPCS_B_2	Ⓞ GND Ⓞ VCCAUX Ⓞ VCCINT Ⓞ VCCO Ⓞ NC

UG385_c3_17_111909

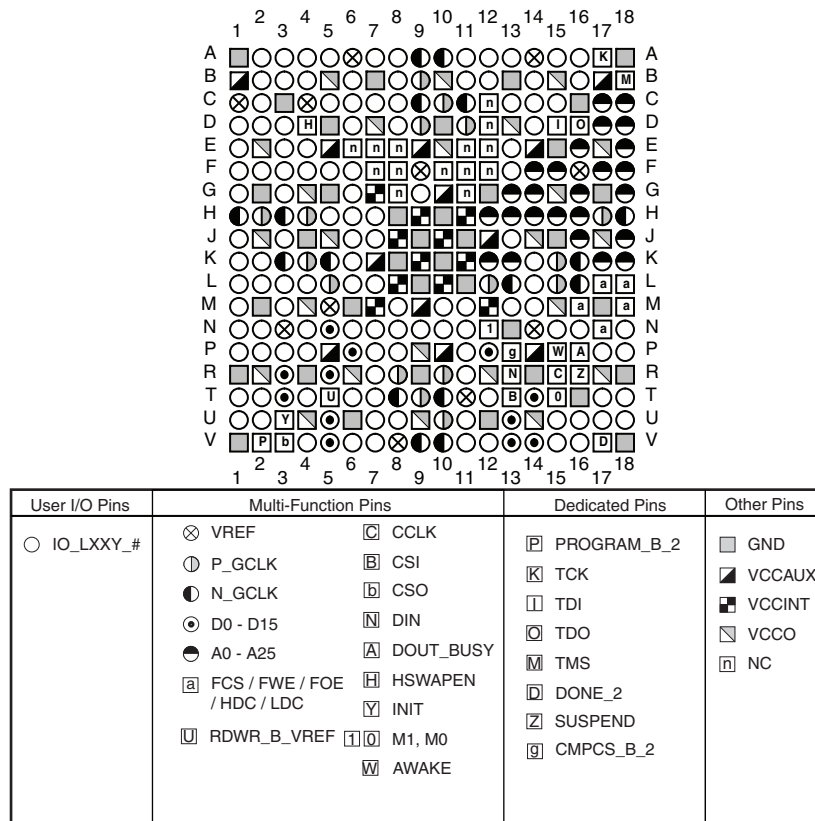
Figure 3-17: CSG324 Package—LX25T Pinout Diagram



UG385_c3_18_110209

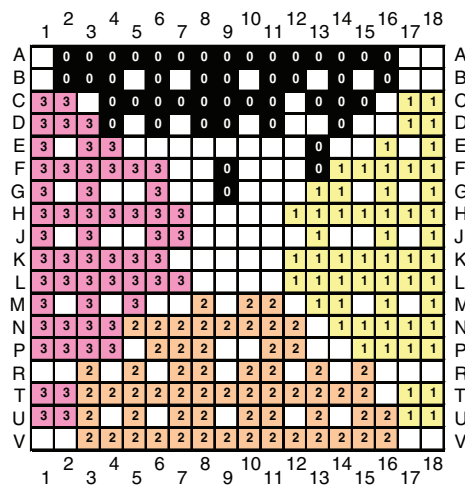
Figure 3-18: CSG324 Package—LX25T I/O Bank Diagram

CSG324 Package—LX45



UG385_c3_19_111909

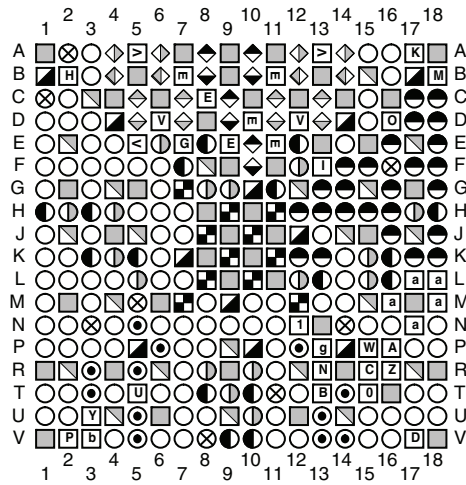
Figure 3-19: CSG324 Package—LX45 Pinout Diagram



UG385_c3_20_110209

Figure 3-20: CSG324 Package—LX45 I/O Bank Diagram

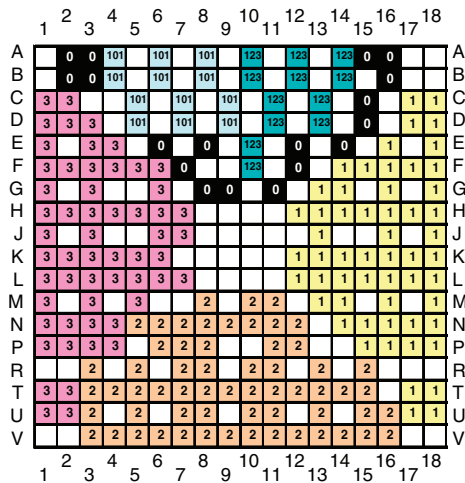
CSG324 Package—LX45T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 Ⓜ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	Ⓛ CCLK Ⓛ CSI Ⓛ CSO Ⓛ DIN Ⓛ DOUT_BUSY Ⓛ HSWAPEN Ⓛ INIT Ⓛ M1, M0 Ⓛ AWAKE	Ⓛ MGTAVCC Ⓛ MGTAVCCPLL Ⓛ MGTAVTTRX Ⓛ MGTAVTTRCAL Ⓛ MGTAVTTTX Ⓛ MGTREFCLK (P) Ⓛ MGTREFCLK (N) Ⓛ MGTTRREF	Ⓛ PROGRAM_B_2 Ⓛ TCK Ⓛ TDI Ⓛ TDO Ⓛ TMS Ⓛ DONE_2 Ⓛ SUSPEND Ⓛ CMPCS_B_2	Ⓛ GND Ⓛ VCCAUX Ⓛ VCCINT Ⓛ VCCO Ⓛ NC

UG385_c3_21_111909

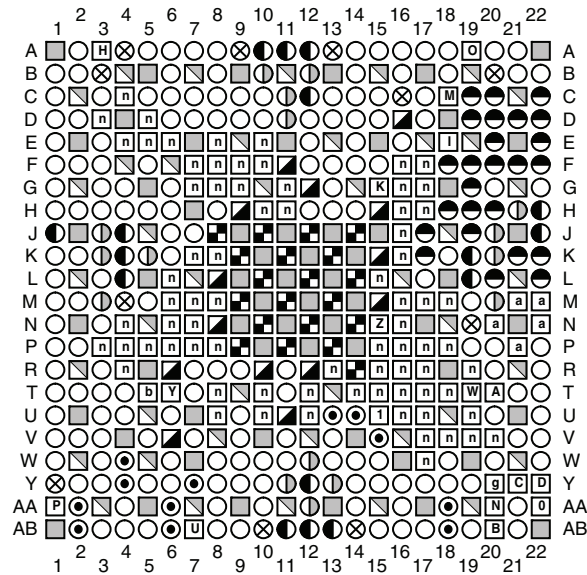
Figure 3-21: CSG324 Package—LX45T Pinout Diagram



UG385_c3_22_110209

Figure 3-22: CSG324 Package—LX45T I/O Bank Diagram

FG(G)484 Package—LX25



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ⊖ A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN Ⓨ INIT ⓐ M1, M0 Ⓨ AWAKE	ⓐ PROGRAM_B_2 ⓑ TCK ⓓ TDI Ⓨ TDO ⓐ TMS ⓑ DONE_2 Ⓨ SUSPEND ⓐ CMPCS_B_2	ⓐ GND ⓑ VCCAUX ⓓ VCCINT Ⓨ VCCO ⓐ NC

UG385_c3_23_111909

Figure 3-23: FG(G)484 Package—LX25 Pinout Diagram

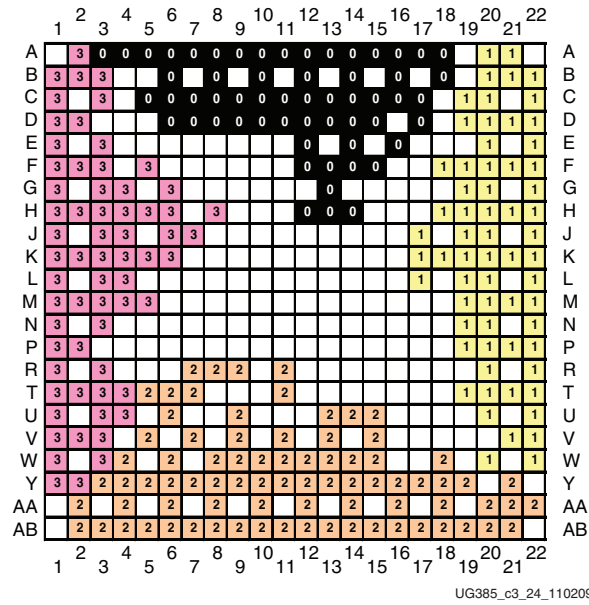
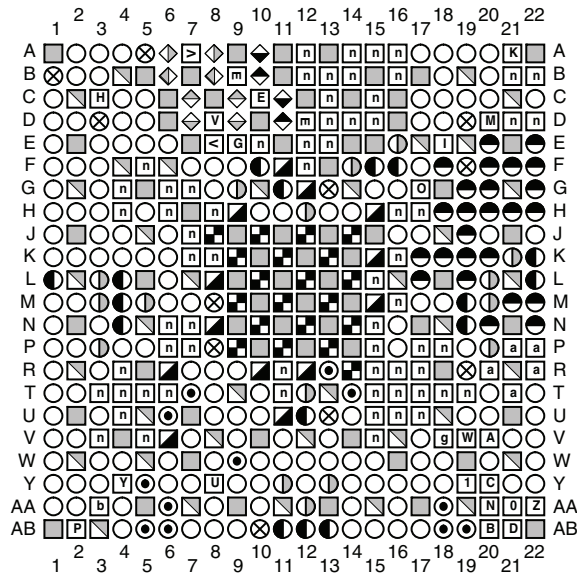


Figure 3-24: FG(G)484 Package—LX25 I/O Bank Diagram

FG(G)484 Package—LX25T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF Ⓛ P_GCLK ● N_GCLK ⦿ D0 - D15 ⦿ A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ MGTAVCC ⓐ MGTAVCCPLL Ⓥ MGTAVTTRX ⓐ MGTAVTTRCAL ⓐ MGTAVTTTX ⦿ MGTREFCLK (P) ⦿ MGTREFCLK (N) ⓐ MGTREF	ⓐ PROGRAM_B_2 ⓐ TCK ⓐ TDI ⓐ TDO ⓐ TMS ⓐ DONE_2 ⓐ SUSPEND ⓐ CMPCS_B_2	ⓐ GND ⓐ VCCAUX ⓐ VCCINT ⓐ VCCO ⓐ NC
	ⓐ CCLK ⓐ CSI ⓐ CSO ⓐ DIN ⓐ DOUT_BUSY ⓐ HSWAPEN ⓐ INIT ⓐ M1, M0 ⓐ AWAKE			

UG385_c3_25_111909

Figure 3-25: FG(G)484 Package—LX25T Pinout Diagram

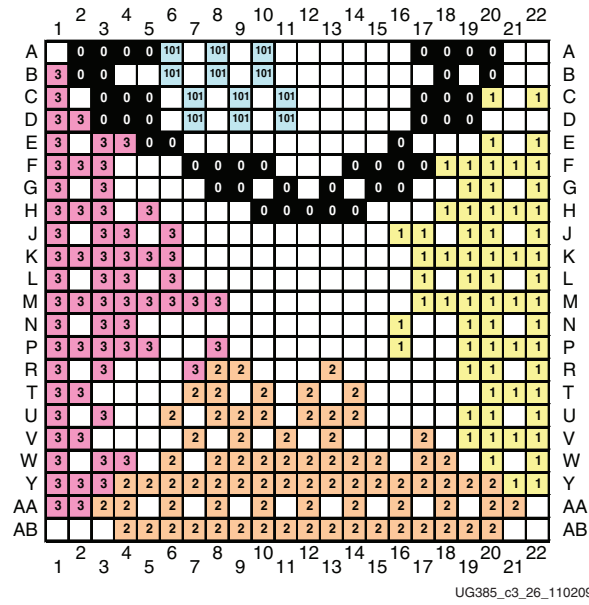
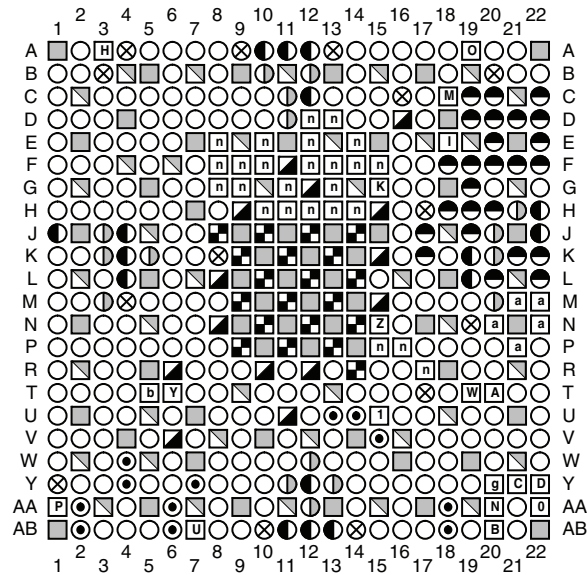


Figure 3-26: FG(G)484 Package—LX25T I/O Bank Diagram

FG(G)484 Package—LX45



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	ⓐ CCLK	■ GND
	ⓐ P_GCLK	ⓑ CSI	▣ VCCAUX
	● N_GCLK	ⓓ CSO	▤ VCCINT
	⦿ D0 - D15	Ⓨ DIN	▥ VCCO
	⦿ A0 - A25	ⓐ DOUT_BUSY	Ⓨ NC
	ⓐ FCS / FWE / FOE / HDC / LDC	Ⓨ HSWAPEN	
	Ⓨ RDWR_B_VREF	Ⓨ INIT	
	Ⓨ M1, M0	Ⓨ AWAKE	
		ⓐ PROGRAM_B_2	
		Ⓨ TCK	
		Ⓨ TDI	
		Ⓨ TDO	
		Ⓨ TMS	
		Ⓨ DONE_2	
		Ⓨ SUSPEND	
		Ⓨ CMPCS_B_2	

UG385_c3_27_111909

Figure 3-27: FG(G)484 Package—LX45 Pinout Diagram

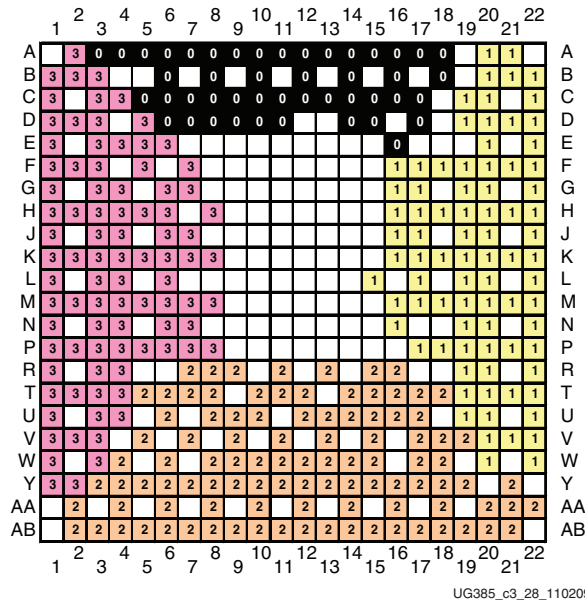
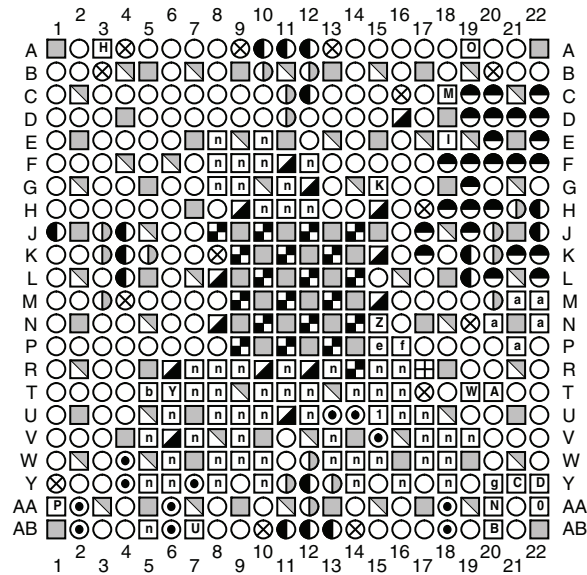


Figure 3-28: FG(G)484 Package—LX45 I/O Bank Diagram

FG(G)484 Package—LX75



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	⊞ CCLK	■ GND
	Ⓟ P_GCLK	Ⓛ CSI	Ⓛ VFS
	● N_GCLK	Ⓛ CSO	Ⓛ VBATT
	⦿ D0 - D15	Ⓛ DIN	▣ VCCAUX
	⦿ A0 - A25	Ⓛ DOUT_BUSY	▣ VCCINT
	Ⓛ FCS / FWE / FOE / HDC / LDC	Ⓛ HSWAPEN	▣ VCCO
	Ⓛ RDWR_B_VREF	Ⓛ INIT	Ⓛ NC
	Ⓛ M1, M0	Ⓛ AWAKE	
		Ⓛ PROGRAM_B_2	
		Ⓛ TCK	
		Ⓛ TDI	
		Ⓛ TDO	
		Ⓛ TMS	
		Ⓛ DONE_2	
		Ⓛ SUSPEND	
		Ⓛ CMPCS_B_2	
		Ⓛ RFUSE	

UG385_c3_29_111909

Figure 3-29: FG(G)484 Package—LX75 Pinout Diagram

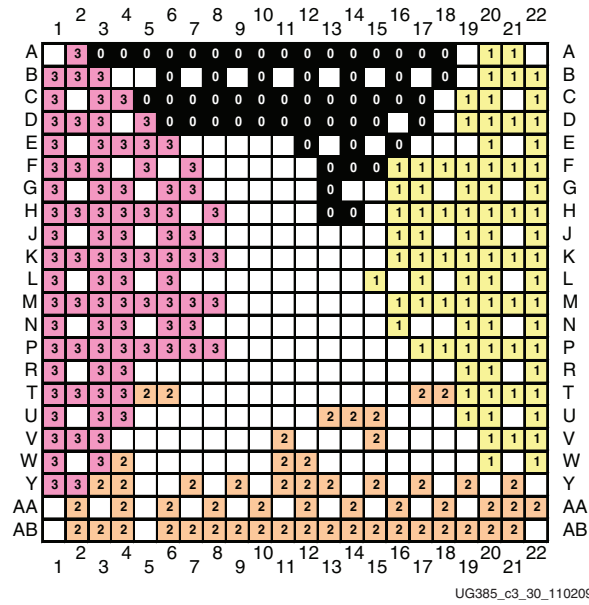
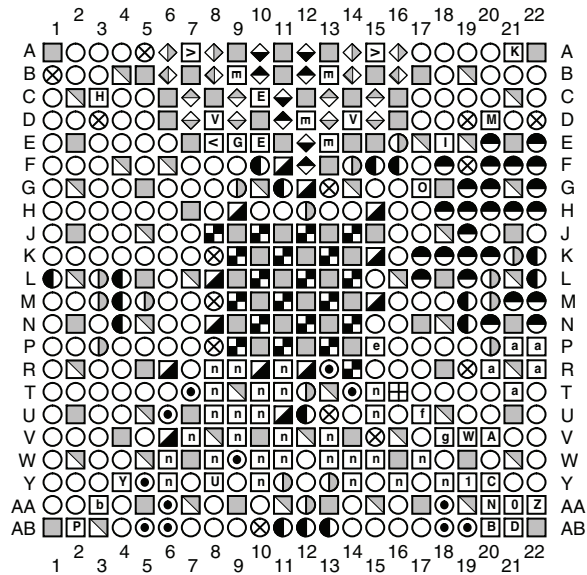


Figure 3-30: FG(G)484 Package—LX75 I/O Bank Diagram

FG(G)484 Package—LX75T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 Ⓜ FCS / FWE / FOE / HDC / LDC Ⓜ RDWR_B_VREF	Ⓜ MGTAVCC Ⓜ MGTAVCCPLL Ⓜ MGTAVTTRX Ⓜ MGTAVTTRCAL Ⓜ MGTAVTTTX Ⓜ MGTREFCLK (P) Ⓜ MGTREFCLK (N) Ⓜ MGTTRREF	Ⓜ PROGRAM_B_2 Ⓜ TCK Ⓜ TDI Ⓜ TDO Ⓜ TMS Ⓜ DONE_2 Ⓜ SUSPEND Ⓜ CMPCS_B_2 Ⓜ RFUSE	Ⓜ GND Ⓜ VFS Ⓜ VBATT Ⓜ VCCAUX Ⓜ VCCINT Ⓜ VCCO Ⓜ NC
	Ⓜ CCLK Ⓜ CSI Ⓜ CSO Ⓜ DIN Ⓜ DOUT_BUSY Ⓜ HSWAPEN Ⓜ INIT Ⓜ M1, M0 Ⓜ AWAKE	Ⓜ MGTRXP Ⓜ MGTRXN Ⓜ MGTTXN Ⓜ MGTTXP		

UG385_c3_31_111909

Figure 3-31: FG(G)484 Package—LX75T Pinout Diagram

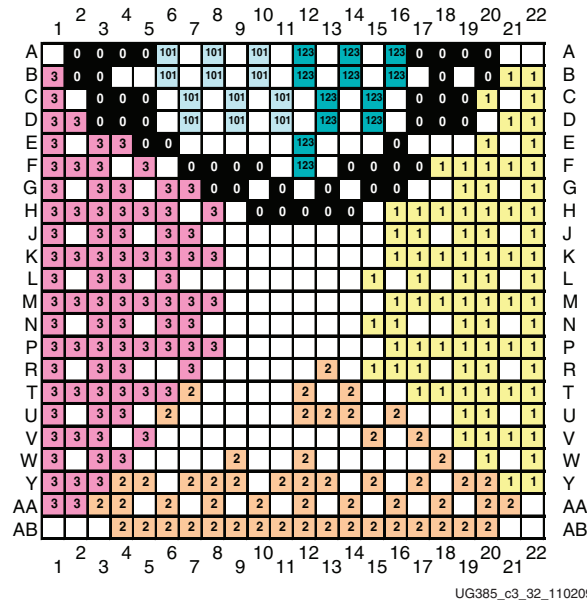
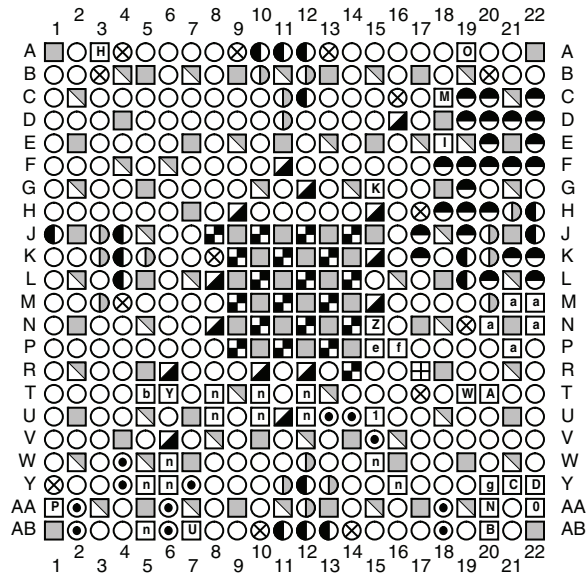


Figure 3-32: FG(G)484 Package—LX75T I/O Bank Diagram

FG(G)484 Package—LX100



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ DO - D15 ⊖ A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊞ RDWR_B_VREF	⊞ CCLK ⊞ CSI ⊞ CSO ⊞ DIN ⊞ DIN ⊞ DOUT_BUSY ⊞ HSWAPEN ⊞ INIT ⊞ M1, M0 ⊞ AWAKE	⊞ PROGRAM_B_2 ⊞ TCK ⊞ TDI ⊞ TDO ⊞ TMS ⊞ DONE_2 ⊞ SUSPEND ⊞ CMPCS_B_2 ⊞ RFUSE	⊞ GND ⊞ VFS ⊞ VBATT ⊞ VCCAUX ⊞ VCCINT ⊞ VCCO ⊞ NC

UG385_c3_33_111909

Figure 3-33: FG(G)484 Package—LX100 Pinout Diagram

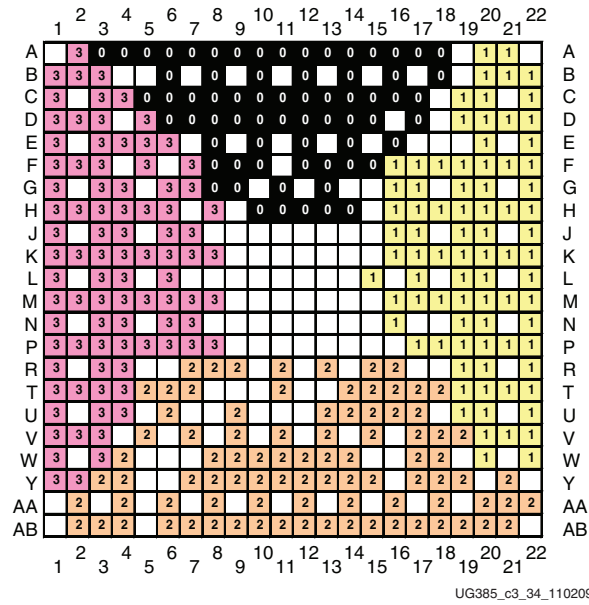
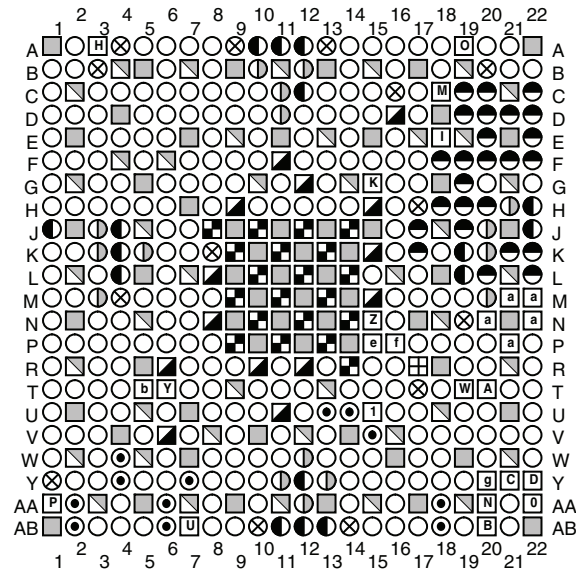


Figure 3-34: FG(G)484 Package—LX100 I/O Bank Diagram

FG(G)484 Package—LX150



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	Ⓟ PROGRAM_B_2	■ GND
	Ⓛ P_GCLK	Ⓚ TCK	Ⓛ VFS
	Ⓜ N_GCLK	Ⓛ TDI	Ⓛ VBATT
	Ⓞ D0 - D15	Ⓞ TDO	Ⓛ VCCAUX
	Ⓛ A0 - A25	Ⓜ TMS	Ⓛ VCCINT
	Ⓛ FCS / FWE / FOE / HDC / LDC	Ⓞ DONE_2	Ⓛ VCCO
	Ⓛ RDWR_B_VREF	Ⓛ SUSPEND	Ⓛ NC
	Ⓛ M1, M0	Ⓛ CMPCS_B_2	
	Ⓛ AWAKE	Ⓛ RFUSE	
	Ⓛ CCLK		
	Ⓛ CSI		
	Ⓛ CSO		
	Ⓛ DIN		
	Ⓛ DOUT_BUSY		
	Ⓛ HSWAPEN		
	Ⓛ INIT		

UG385_c3_35_111909

Figure 3-35: FG(G)484 Package—LX150 Pinout Diagram

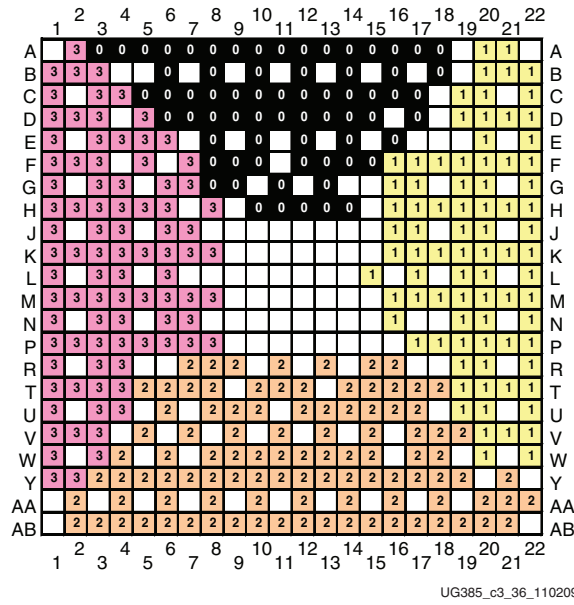
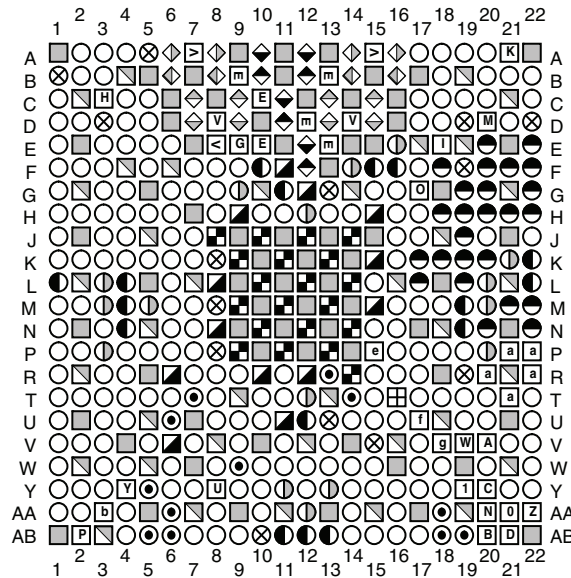


Figure 3-36: FG(G)484 Package—LX150 I/O Bank Diagram

FG(G)484 Package—LX45T, LX100T, and LX150T

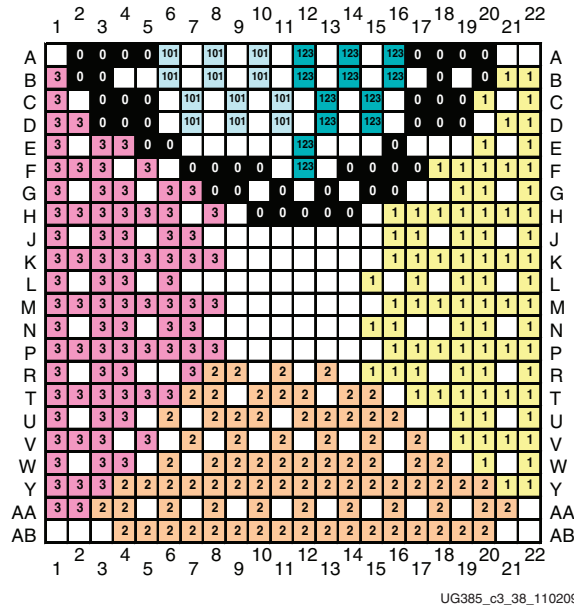


User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN ⓓ INIT ⓓ M1, M0 ⓓ AWAKE	ⓐ MGTAVCC ⓑ MGTAVCCPLL ⓓ MGTAVTTRX ⓐ MGTAVTTRCAL ⓓ MGTAVTTTX ⓓ MGTREFCLK (P) ⓓ MGTREFCLK (N) ⓓ MGTTRREF ⓓ MGTRXP ⓓ MGTRXN ⓓ MGTTXN ⓓ MGTTXP	ⓐ PROGRAM_B_2 ⓑ TCK ⓓ TDI ⓐ TDO ⓓ TMS ⓓ DONE_2 ⓓ SUSPEND ⓓ CMPCS_B_2 ⓓ RFUSE	ⓐ GND ⓑ VFS ⓓ VBATT ⓐ VCCAUX ⓓ VCCINT ⓓ VCCO ⓓ NC

UG385_c3_37_111909

Figure 3-37: FG(G)484 Package—LX45T, LX100T, and LX150T Pinout Diagram

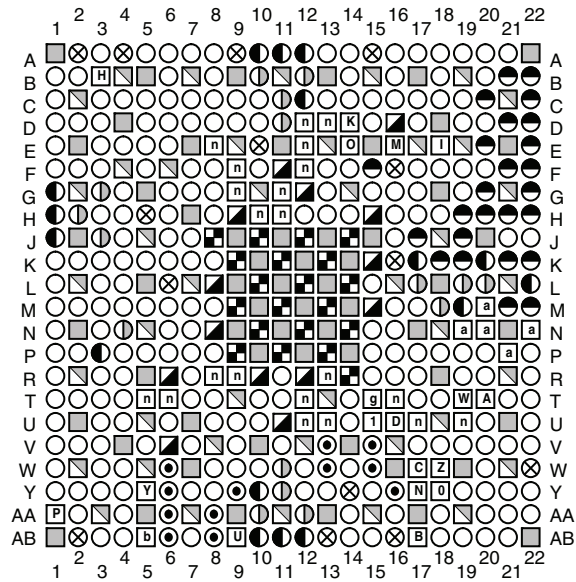
Note: The RFUSE, VBATT, and VFS pins are no connects in the LX45T in the FG(G)484 package.



UG385_c3_38_110209

Figure 3-38: FG(G)484 Package—LX45T, LX100T, and LX150T I/O Bank Diagram

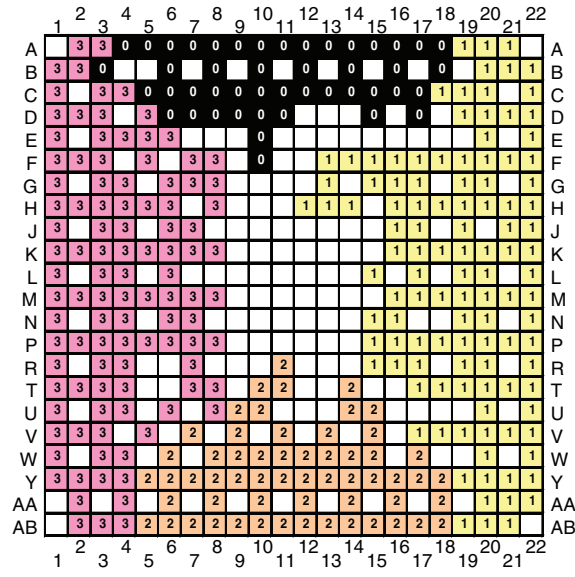
CSG484 Package—LX45



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊔ RDWR_B_VREF	⊞ CCLK ⊞ CSI ⊞ CSO ⊞ DIN ⊞ DOUT_BUSY ⊞ HSWAPEN ⊞ INIT ⊞ M1, M0 ⊞ AWAKE	⊞ PROGRAM_B_2 ⊞ TCK ⊞ TDI ⊞ TDO ⊞ TMS ⊞ DONE_2 ⊞ SUSPEND ⊞ CMPCS_B_2	⊞ GND ⊞ VCCAUX ⊞ VCCINT ⊞ VCCO ⊞ NC

UG385_c3_39_111909

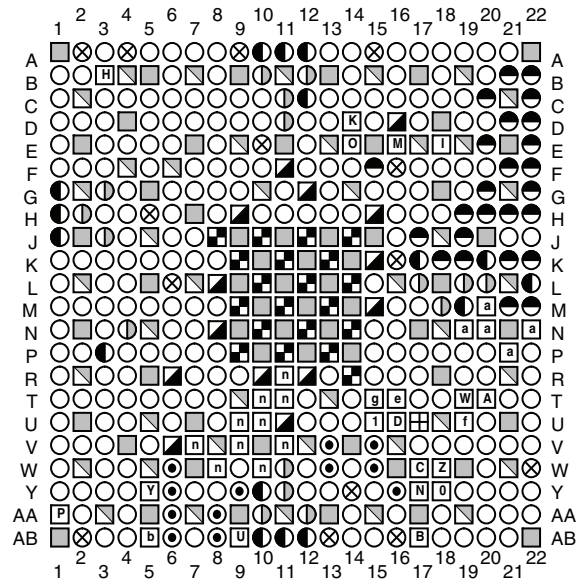
Figure 3-39: CSG484 Package—LX45 Pinout Diagram



UG385_c3_40_110209

Figure 3-40: CSG484 Package—LX45 I/O Bank Diagram

CS(G)484 Package—LX75



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ⊖ A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN Ⓨ INIT Ⓤ M1, M0 Ⓨ AWAKE	ⓐ PROGRAM_B_2 ⓑ TCK Ⓨ TDI ⓐ TDO ⓑ TMS Ⓨ DONE_2 ⓐ SUSPEND ⓑ CMPCS_B_2 Ⓨ RFUSE	ⓐ GND ⓑ VFS Ⓨ VBATT ⓐ VCCAUX ⓑ VCCINT Ⓨ VCCO ⓐ NC

UG385_c3_41_111909

Figure 3-41: CS(G)484 Package—LX75 Pinout Diagram

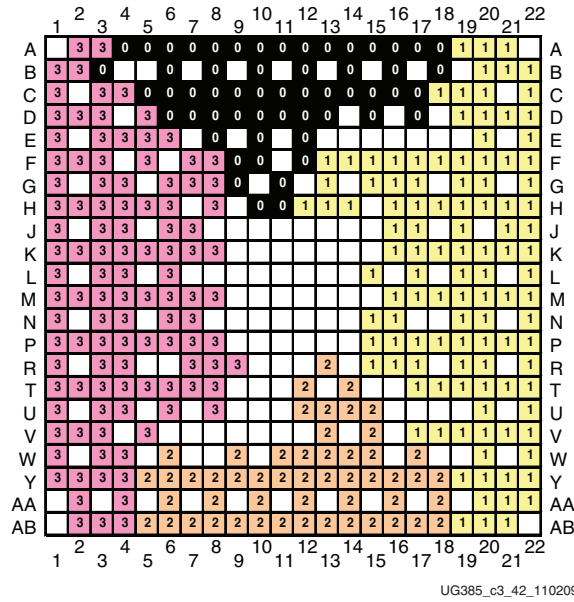
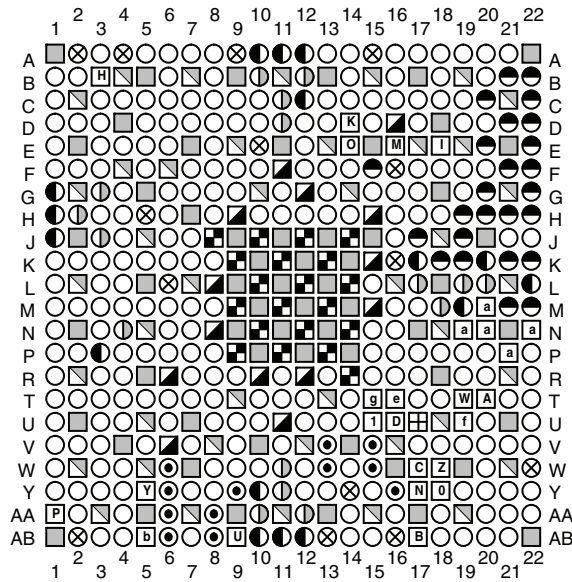


Figure 3-42: CS(G)484 Package—LX75 I/O Bank Diagram

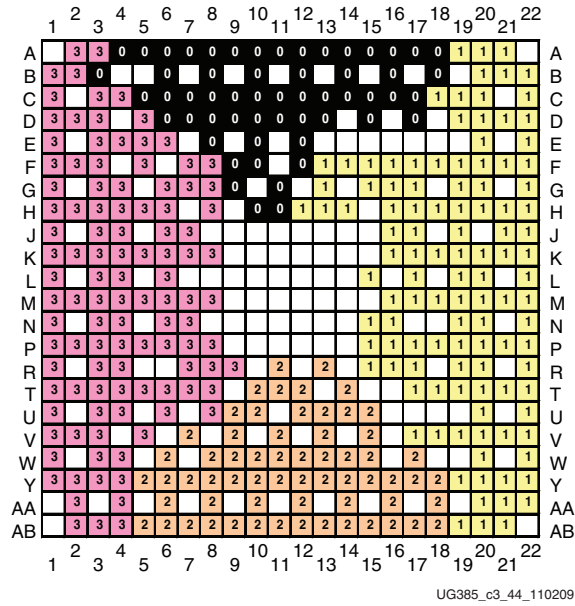
CS(G)484 Package—LX100 and LX150



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	Ⓜ PROGRAM_B_2	■ GND
	Ⓟ P_GCLK	Ⓚ TCK	Ⓛ VFS
	● N_GCLK	Ⓛ TDI	Ⓜ VBATT
	Ⓞ DO - D15	Ⓞ TDO	▣ VCCAUX
	● A0 - A25	Ⓜ TMS	■ VCCINT
	Ⓜ FCS / FWE / FOE / HDC / LDC	Ⓞ DONE_2	▣ VCCO
	Ⓛ RDWR_B_VREF	▣ SUSPEND	Ⓛ NC
	Ⓛ M1, M0	Ⓞ CMPCS_B_2	
	Ⓜ AWAKE	Ⓞ RFUSE	
	Ⓞ CCLK		
	Ⓛ CSI		
	Ⓛ CSO		
	Ⓛ DIN		
	Ⓛ DOUT_BUSY		
	Ⓛ HSWAPEN		
	Ⓛ INIT		

UG385_c3_43_111909

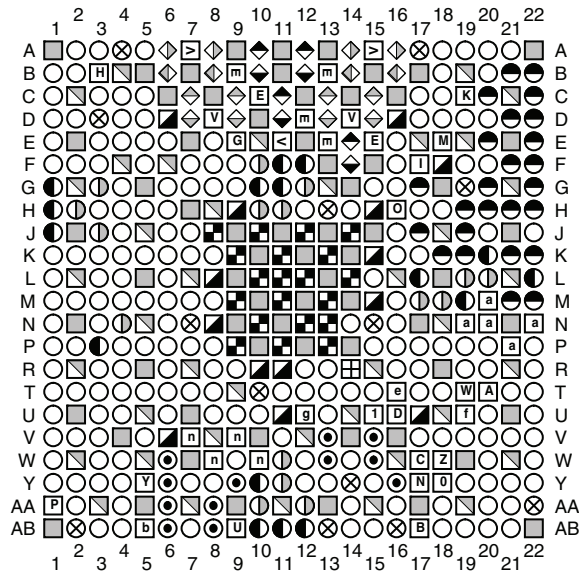
Figure 3-43: CS(G)484 Package—LX100 and LX150 Pinout Diagram



UG385_c3_44_110209

Figure 3-44: CS(G)484 Package—LX100 and LX150 I/O Bank Diagram

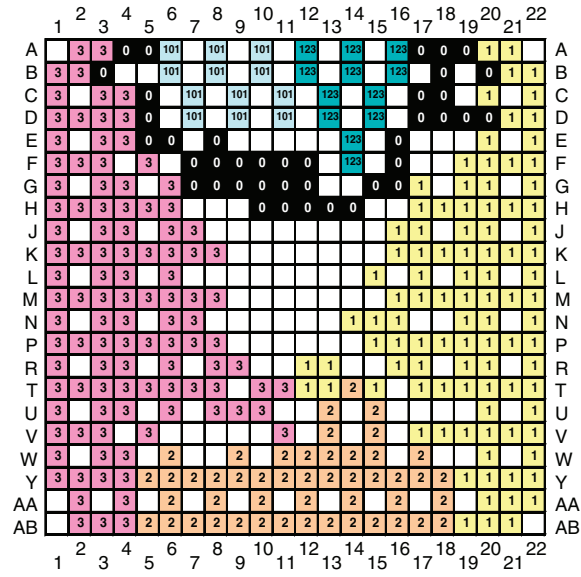
CS(G)484 Package—LX75T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊔ RDWR_B_VREF	⊞ CCLK ⊞ CSI ⊞ CSO ⊞ DIN ⊞ DOUT_BUSY ⊞ HSWAPEN ⊞ INIT ⊞ M1, M0 ⊞ AWAKE	⊞ MGTAVCC ⊞ MGTAVCCPLL ⊞ MGTAVTTRX ⊞ MGTAVTTRCAL ⊞ MGTAVTTTX ⊞ MGTREFCLK (P) ⊞ MGTREFCLK (N) ⊞ MGTTRREF	⊞ MGTRXP ⊞ MGTRXN ⊞ MGTTXN ⊞ MGTTXP ⊞ PROGRAM_B_2 ⊞ TCK ⊞ TDI ⊞ TDO ⊞ TMS ⊞ DONE_2 ⊞ SUSPEND ⊞ CMPCS_B_2 ⊞ RFUSE	⊞ GND ⊞ VFS ⊞ VBATT ⊞ VCCAUX ⊞ VCCINT ⊞ VCCO ⊞ NC

UG385_c3_45_111909

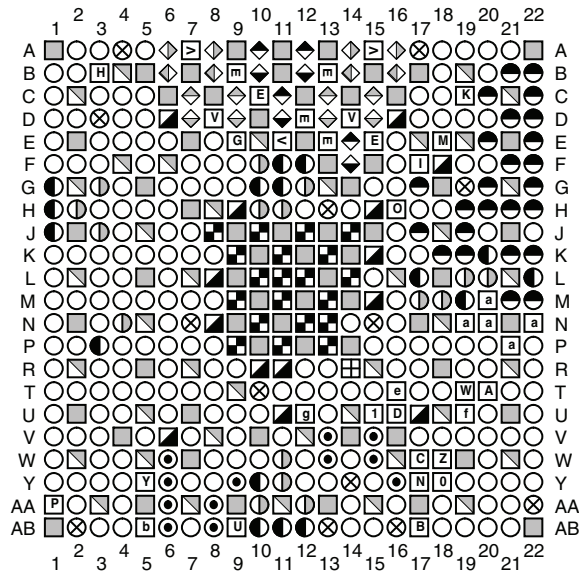
Figure 3-45: CS(G)484 Package—LX75T Pinout Diagram



UG385_c3_46_110209

Figure 3-46: CS(G)484 Package—LX75T I/O Bank Diagram

CS(G)484 Package—LX45T, LX100T, and LX150T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊔ RDWR_B_VREF	⊞ CCLK ⊞ CSI ⊞ CSO ⊞ DIN ⊞ DOUT_BUSY ⊞ HSWAPEN ⊞ INIT ⊞ M1, M0 ⊞ AWAKE	⊞ MGTAVCC ⊞ MGTAVCCPLL ⊞ MGTAVTTRX ⊞ MGTAVTTRCAL ⊞ MGTAVTTTX ⊞ MGTREFCLK (P) ⊞ MGTREFCLK (N) ⊞ MGTTRREF	⊞ MGTRXP ⊞ MGTRXN ⊞ MGTTXN ⊞ MGTTXP ⊞ PROGRAM_B_2 ⊞ TCK ⊞ TDI ⊞ TDO ⊞ TMS ⊞ DONE_2 ⊞ SUSPEND ⊞ CMPCS_B_2 ⊞ RFUSE	⊞ GND ⊞ VFS ⊞ VBATT ⊞ VCCAUX ⊞ VCCINT ⊞ VCCO ⊞ NC

UG385_c3_47_111909

Figure 3-47: CS(G)484 Package—LX45T, LX100T, and LX150T Pinout Diagram

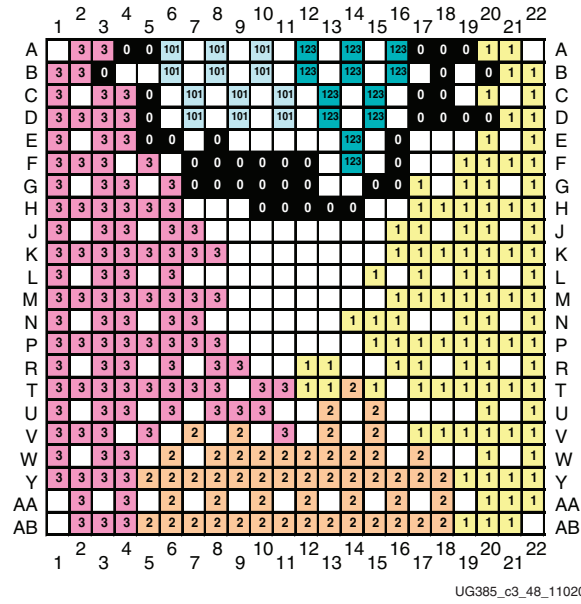
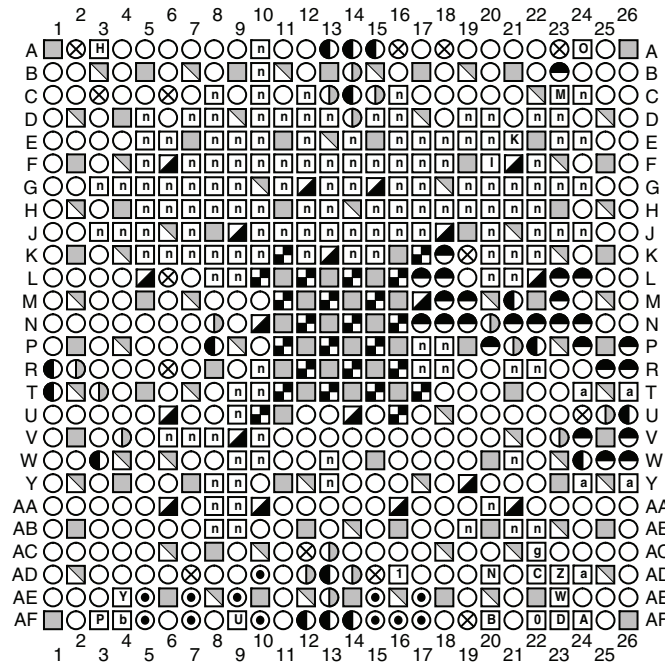


Figure 3-48: CS(G)484 Package—LX45T, LX100T, and LX150T I/O Bank Diagram

FG(G)676 Package—LX45



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	ⓐ PROGRAM_B_2	■ GND
	ⓐ P_GCLK	ⓐ TCK	▣ VCCAUX
	● N_GCLK	ⓐ TDI	▣ VCCINT
	⦿ D0 - D15	ⓐ TDO	▣ VCCO
	● A0 - A25	ⓐ TMS	▣ NC
	ⓐ FCS / FWE / FOE / HDC / LDC	ⓐ DONE_2	
	ⓐ RDWR_B_VREF	ⓐ SUSPEND	
	ⓐ M1, M0	ⓐ CMPCS_B_2	
	ⓐ AWAKE		
	ⓐ CCLK		
	ⓐ CSI		
	ⓐ CSO		
	ⓐ DIN		
	ⓐ DOUT_BUSY		
	ⓐ HSWAPEN		
	ⓐ INIT		
	ⓐ M1, M0		
	ⓐ AWAKE		

UG385_c3_49_111909

Figure 3-49: FG(G)676 Package—LX45 Pinout Diagram

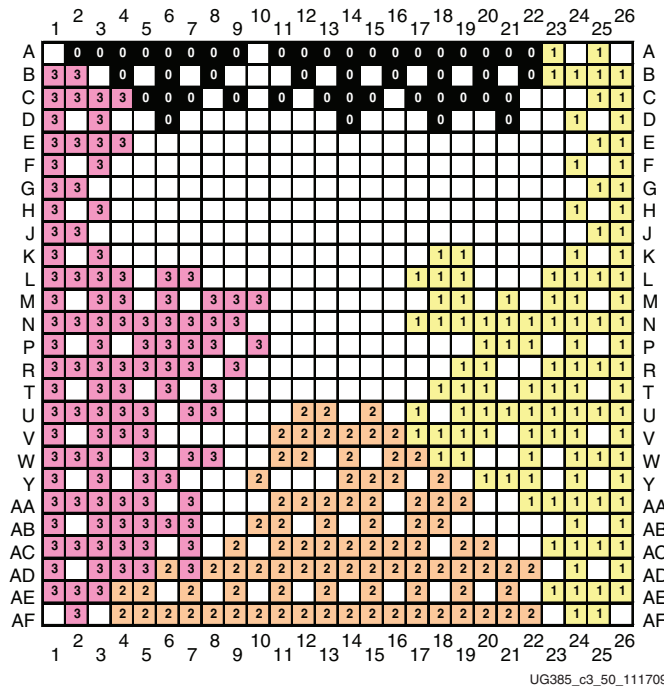
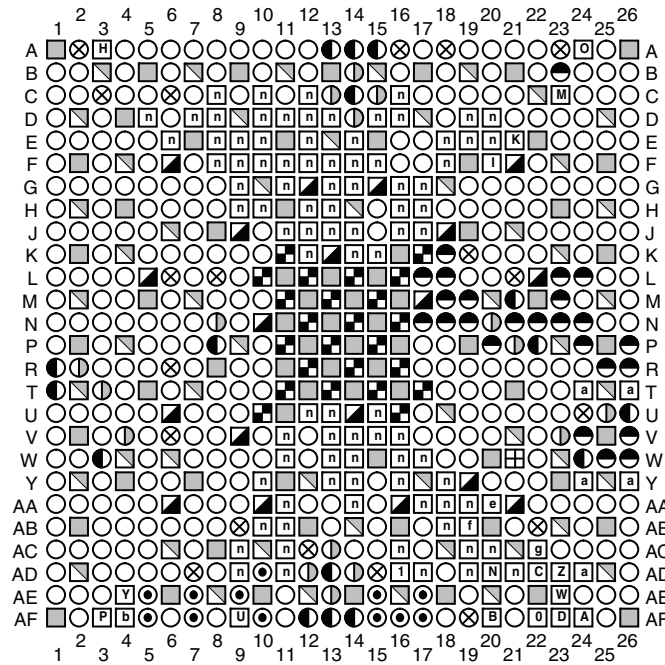


Figure 3-50: FG(G)676 Package—LX45 I/O Bank Diagram

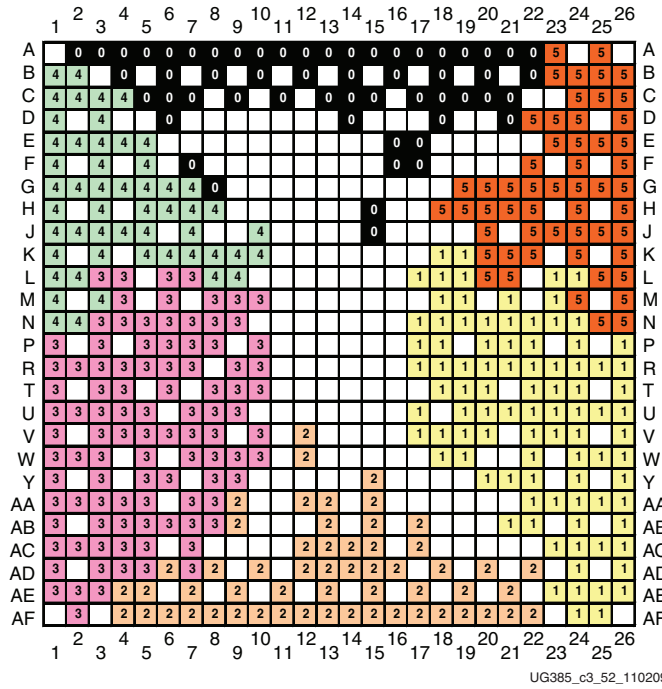
FG(G)676 Package—LX75



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF	ⓐ PROGRAM_B_2	■ GND
	ⓐ P_GCLK	ⓐ TCK	ⓐ VFS
	● N_GCLK	ⓐ TDI	ⓐ VBATT
	ⓐ D0 - D15	ⓐ TDO	ⓐ VCCAUX
	● A0 - A25	ⓐ TMS	ⓐ VCCINT
	ⓐ FCS / FWE / FOE / HDC / LDC	ⓐ DONE_2	ⓐ VCCO
	ⓐ RDWR_B_VREF	ⓐ SUSPEND	ⓐ NC
	ⓐ M1, M0	ⓐ CMPCS_B_2	
	ⓐ AWAKE	ⓐ RFUSE	
	ⓐ CCLK		
	ⓐ CSI		
	ⓐ CSO		
	ⓐ DIN		
	ⓐ DOUT_BUSY		
	ⓐ HSWAPEN		
	ⓐ INIT		

UG385_c3_51_111909

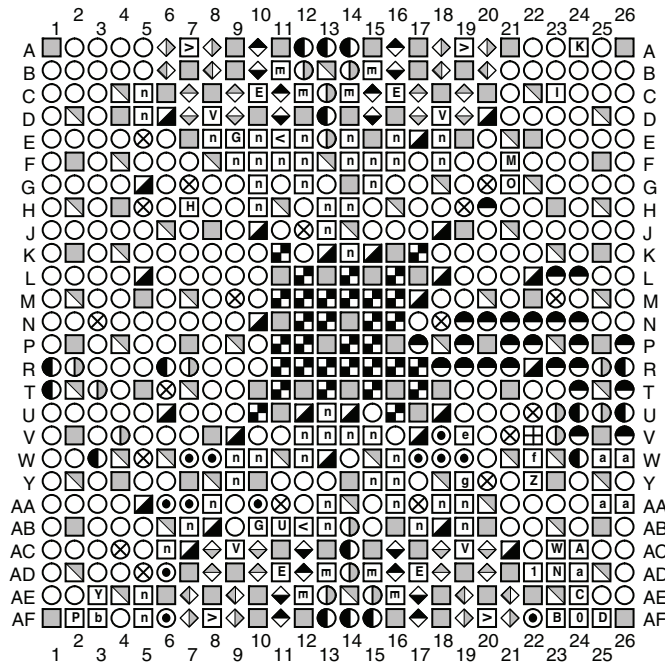
Figure 3-51: FG(G)676 Package—LX75 Pinout Diagram



UG385_c3_52_110209

Figure 3-52: FG(G)676 Package—LX75 I/O Bank Diagram

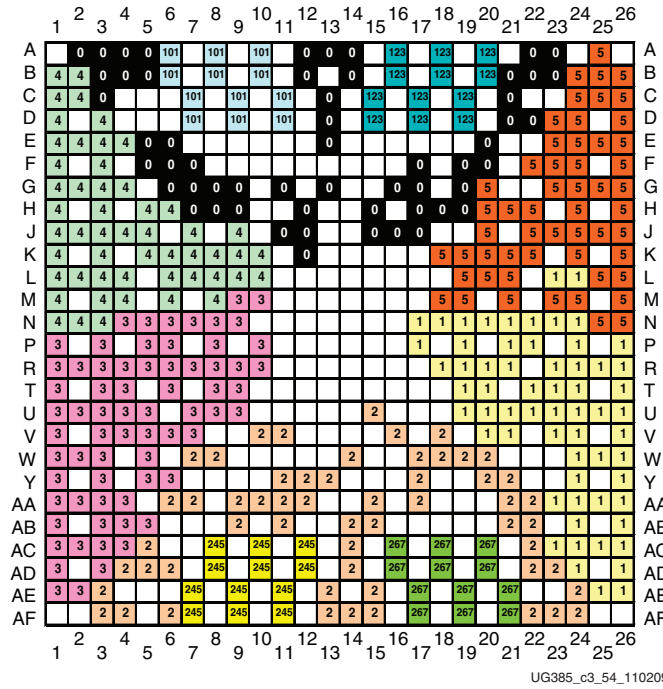
FG(G)676 Package—LX75T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ⊖ A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊡ RDWR_B_VREF	⊞ CCLK ⊞ CSI ⊞ CSO ⊞ DIN ⊞ DOUT_BUSY ⊞ HSWAPEN ⊞ INIT ⊞ M1, M0 ⊞ AWAKE	⊞ MGTAVCC ⊞ MGTAVCCPLL ⊞ MGTAVTTRX ⊞ MGTAVTTRCAL ⊞ MGTAVTTTX ⊞ MGTREFCLK (P) ⊞ MGTREFCLK (N) ⊞ MGTRREF	⊞ MGTRXP ⊞ MGTRXN ⊞ MGTTXN ⊞ MGTTXP ⊞ PROGRAM_B_2 ⊞ TCK ⊞ TDI ⊞ TDO ⊞ TMS ⊞ DONE_2 ⊞ SUSPEND ⊞ CMPCS_B_2 ⊞ RFUSE	⊞ GND ⊞ VFS ⊞ VBATT ⊞ VCCAUX ⊞ VCCINT ⊞ VCCO ⊞ NC

UG385_c3_53_110209

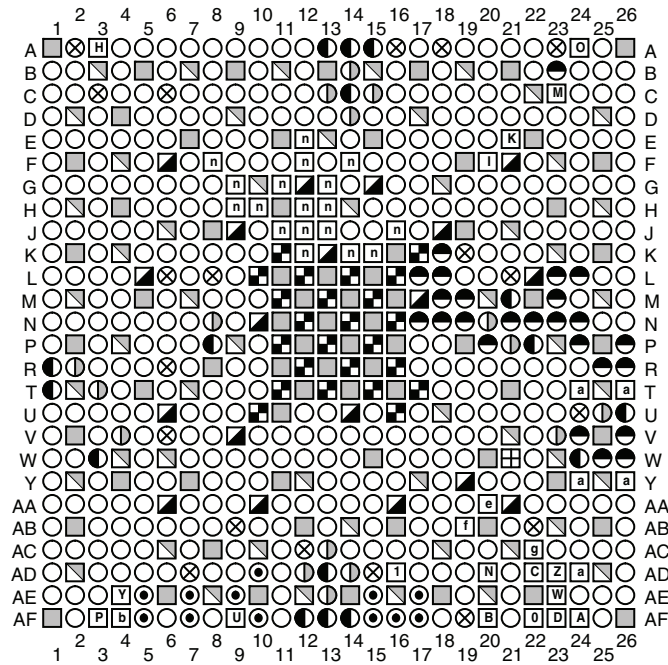
Figure 3-53: FG(G)676 Package—LX75T Pinout Diagram



UG385_c3_54_110209

Figure 3-54: FG(G)676 Package—LX75T I/O Bank Diagram

FG(G)676 Package—LX100



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ⦿ A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN Ⓨ INIT Ⓤ M1, M0 Ⓦ AWAKE	ⓐ PROGRAM_B_2 ⓑ TCK Ⓨ TDI ⓐ TDO ⓑ TMS ⓓ DONE_2 Ⓨ SUSPEND ⓑ CMPCS_B_2 ⓐ RFUSE	ⓐ GND ⓑ VFS Ⓨ VBATT ⓐ VCCAUX ⓑ VCCINT Ⓨ VCCO ⓐ NC

UG385_c3_55_111909

Figure 3-55: FG(G)676 Package—LX100 Pinout Diagram

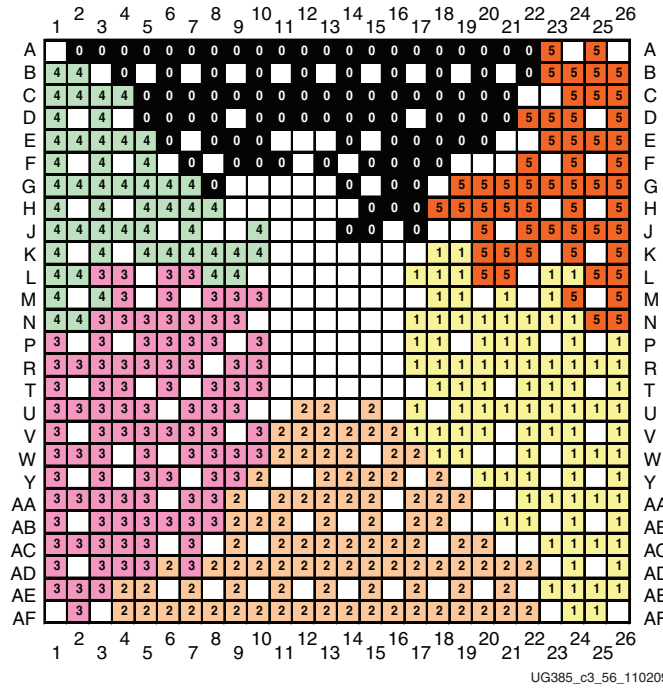
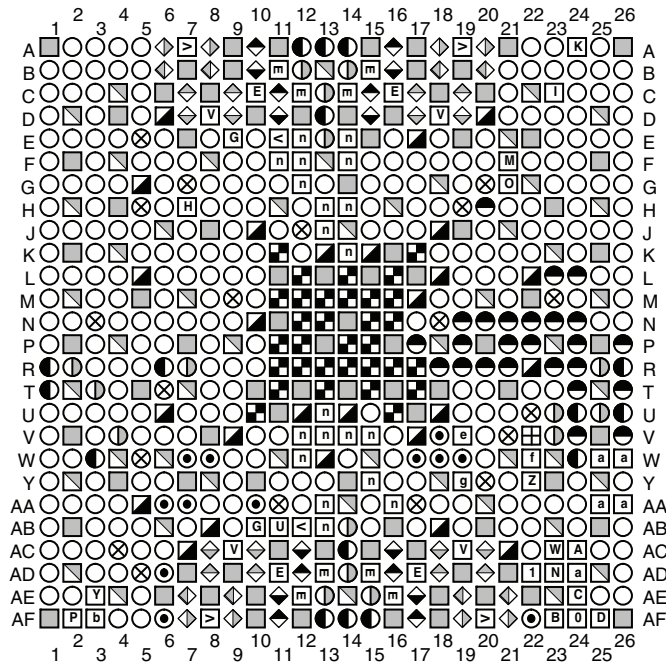


Figure 3-56: FG(G)676 Package—LX100 I/O Bank Diagram

FG(G)676 Package—LX100T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF ⊕ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⊠ FCS / FWE / FOE / HDC / LDC ⊔ RDWR_B_VREF	⊠ MGTAVCC ⊠ MGTAVCCPLL ⊠ MGTAVTTRX ⊠ MGTAVTTRCAL ⊠ MGTAVTTTX ◆ MGTREFCLK (P) ◆ MGTREFCLK (N) ⊠ MGTRREF	⊠ PROGRAM_B_2 ⊠ TCK ⊠ TDI ⊠ TDO ⊠ TMS ⊠ DONE_2 ⊠ SUSPEND ⊠ CMPCS_B_2 ⊠ RFUSE	⊠ GND ⊠ VFS ⊠ VBATT ⊠ VCCAUX ⊠ VCCINT ⊠ VCCO ⊠ NC
	⊠ CCLK ⊠ CSI ⊠ CSO ⊠ DIN ⊠ DOUT_BUSY ⊠ HSWAPEN ⊠ INIT ⊠ M1, M0 ⊠ AWAKE			

UG385_c3_57_111909

Figure 3-57: FG(G)676 Package—LX100T Pinout Diagram

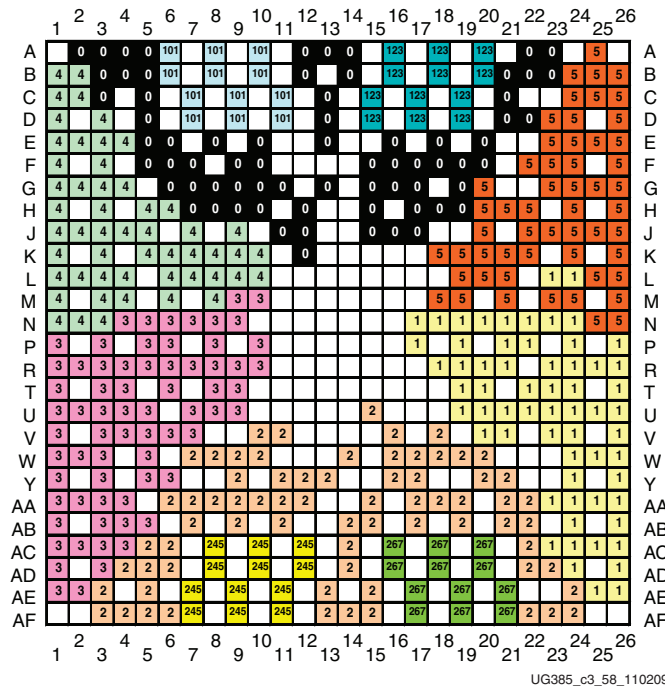
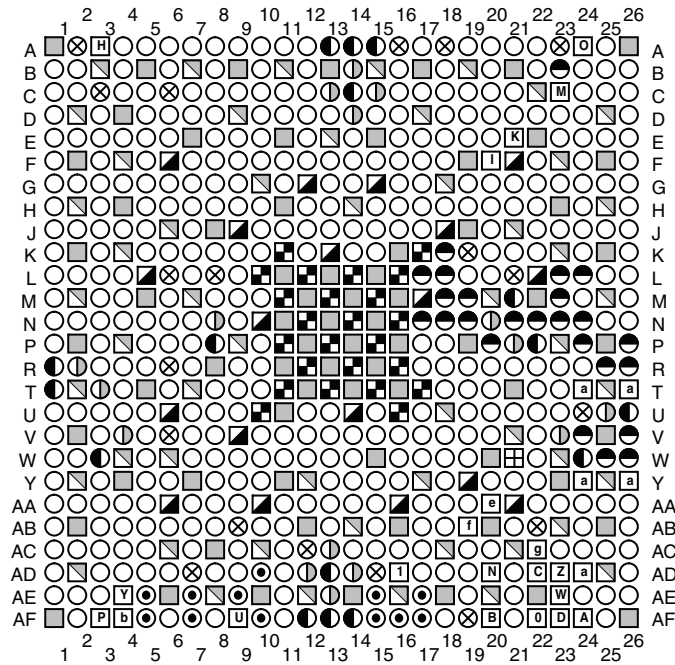


Figure 3-58: FG(G)676 Package—LX100T I/O Bank Diagram

FG(G)676 Package—LX150



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓢ P_GCLK ● N_GCLK ⊙ DO - D15 ● A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓑ HSWAPEN Ⓨ INIT Ⓢ M1, M0 Ⓦ AWAKE	ⓐ PROGRAM_B_2 ⓑ TCK Ⓨ TDI ⓐ TDO ⓑ TMS ⓓ DONE_2 Ⓨ SUSPEND ⓐ CMPCS_B_2 ⓑ RFUSE	■ GND Ⓨ VFS ⓐ VBATT ⓑ VCCAUX Ⓨ VCCINT ⓐ VCCO Ⓨ NC

UG385_c3_59_111909

Figure 3-59: FG(G)676 Package—LX150 Pinout Diagram

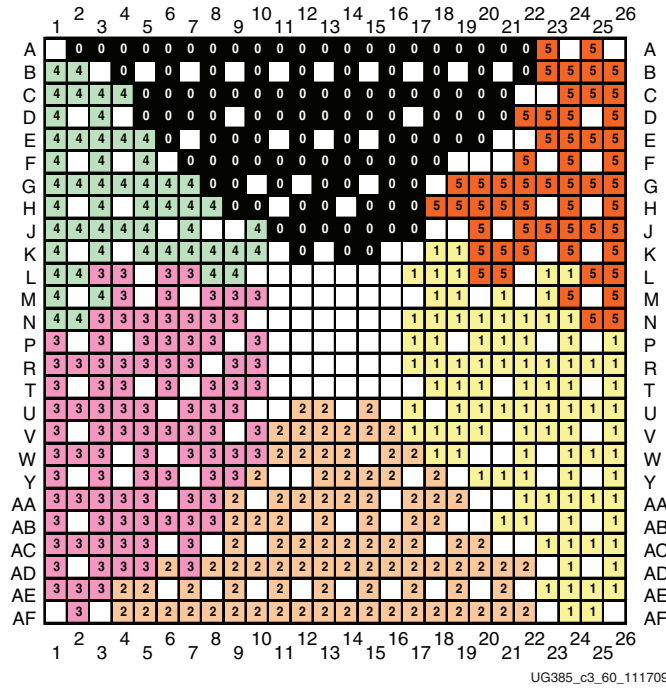
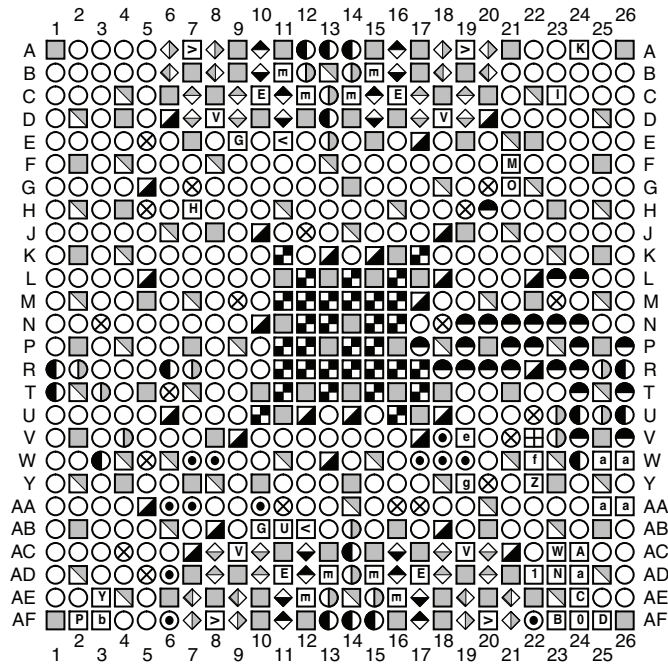


Figure 3-60: FG(G)676 Package—LX150 I/O Bank Diagram

FG(G)676 Package—LX150T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 Ⓜ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	Ⓛ CCLK Ⓛ CSI Ⓛ CSO Ⓛ DIN Ⓛ DOUT_BUSY Ⓛ HSWAPEN Ⓛ INIT Ⓛ M1, M0 Ⓛ AWAKE	Ⓛ MGTAVCC Ⓛ MGTAVCCPLL Ⓛ MGTAVTTRX Ⓛ MGTAVTTRCAL Ⓛ MGTAVTTTX Ⓛ MGTREFCLK (P) Ⓛ MGTREFCLK (N) Ⓛ MGTTRREF	Ⓛ MGTRXP Ⓛ MGTRXN Ⓛ MGTTXN Ⓛ MGTTXP Ⓛ PROGRAM_B_2 Ⓛ TCK Ⓛ TDI Ⓛ TDO Ⓛ TMS Ⓛ DONE_2 Ⓛ SUSPEND Ⓛ CMPCS_B_2 Ⓛ RFUSE	Ⓛ GND Ⓛ VFS Ⓛ VBATT Ⓛ VCCAUX Ⓛ VCCINT Ⓛ VCCO Ⓛ NC

UG385_c3_61_111909

Figure 3-61: FG(G)676 Package—LX150T Pinout Diagram

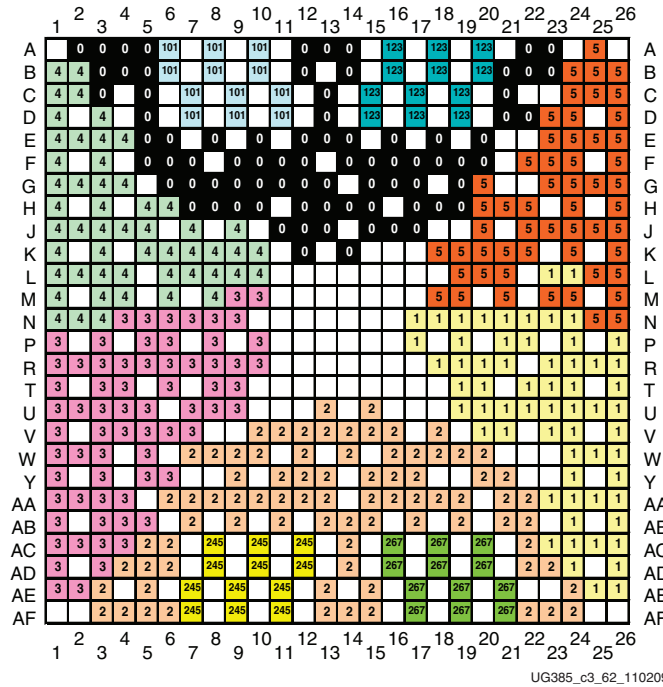
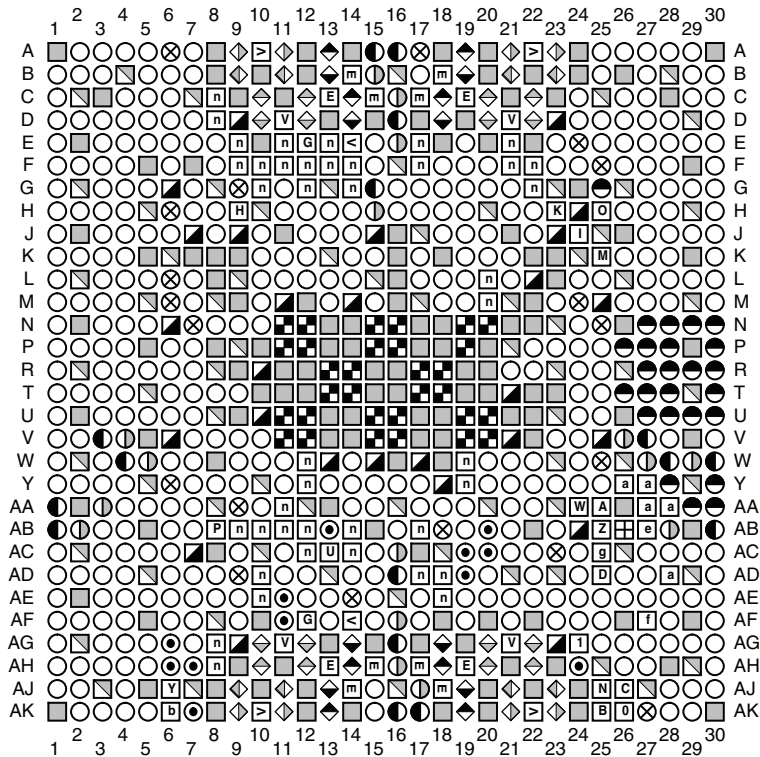


Figure 3-62: FG(G)676 Package—LX150T I/O Bank Diagram

FG(G)900 Package—LX100T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊗ VREF Ⓜ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ MGTA VCC Ⓜ MGTA VCCPLL Ⓤ MGTA VTRTX ⓐ MGTA VTTRCAL ⓐ MGTA VTTTX ◆ MGTR EFLCK (P) ◆ MGTR EFLCK (N) ⓐ MGTR REF	ⓐ PROGRAM_B_2 ⓐ TCK ⓐ TDI ⓐ TDO ⓐ TMS ⓐ DONE_2 ⓐ SUSPEND ⓐ CMPCS_B_2 ⓐ RFUSE	■ GND ⓐ VFS ⓐ VBATT ⓐ VCCAUX ⓐ VCCINT ⓐ VCCO ⓐ NC
	ⓐ CCLK ⓐ CSI ⓐ CSO ⓐ DIN ⓐ DOUT_BUSY ⓐ HSWAPEN ⓐ INIT ⓐ M1, M0 ⓐ AWAKE			

UG385_c3_63_111909

Figure 3-63: FG(G)900 Package—LX100T Pinout Diagram

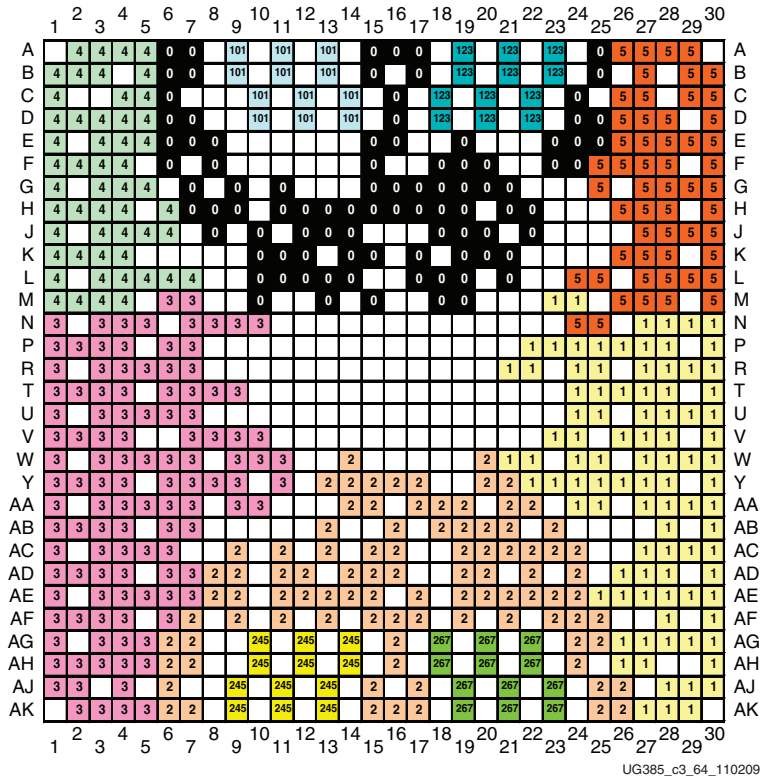
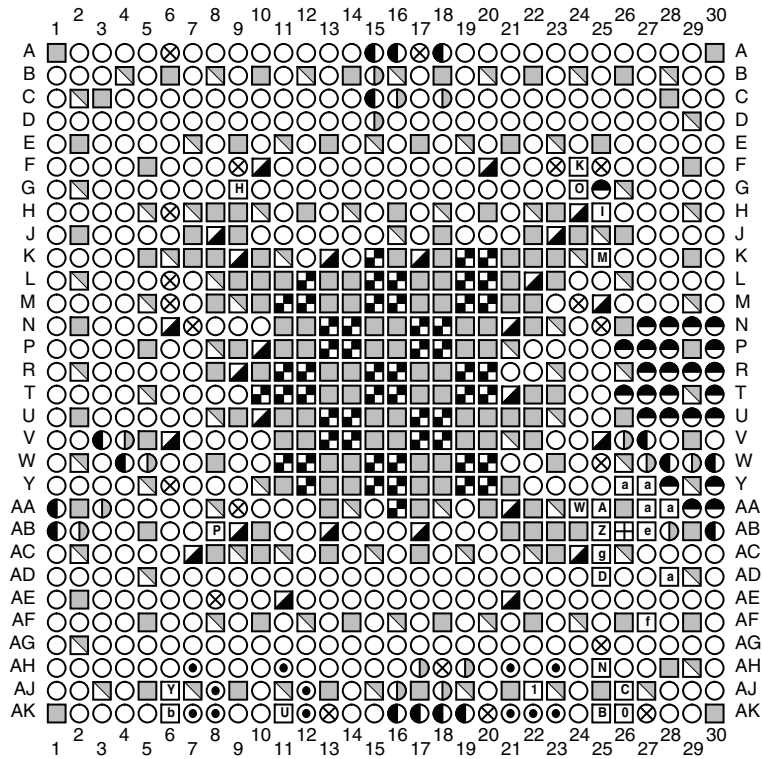


Figure 3-64: FG(G)900 Package—LX100T I/O Bank Diagram

FG(G)900 Package—LX150



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓢ P_GCLK ● N_GCLK ⦿ D0 - D15 ⦿ A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	ⓐ CCLK ⓑ CSI ⓓ CSO Ⓨ DIN ⓐ DOUT_BUSY ⓐ HSWAPEN Ⓨ INIT ⓐ M1, M0 Ⓨ AWAKE	ⓐ PROGRAM_B_2 ⓐ TCK ⓐ TDI ⓐ TDO ⓐ TMS ⓐ DONE_2 ⓐ SUSPEND ⓐ CMPCS_B_2 ⓐ RFUSE	ⓐ GND ⓐ VFS ⓐ VBATT ⓐ VCCAUX ⓐ VCCINT ⓐ VCCO ⓐ NC

UG385_c3_65_012810

Figure 3-65: FG(G)900 Package—LX150 Pinout Diagram

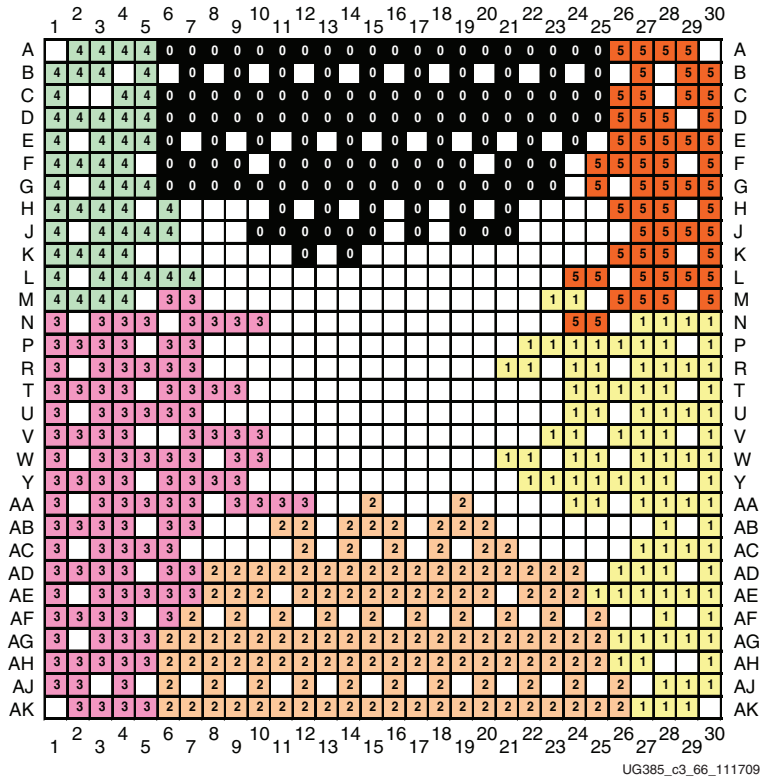
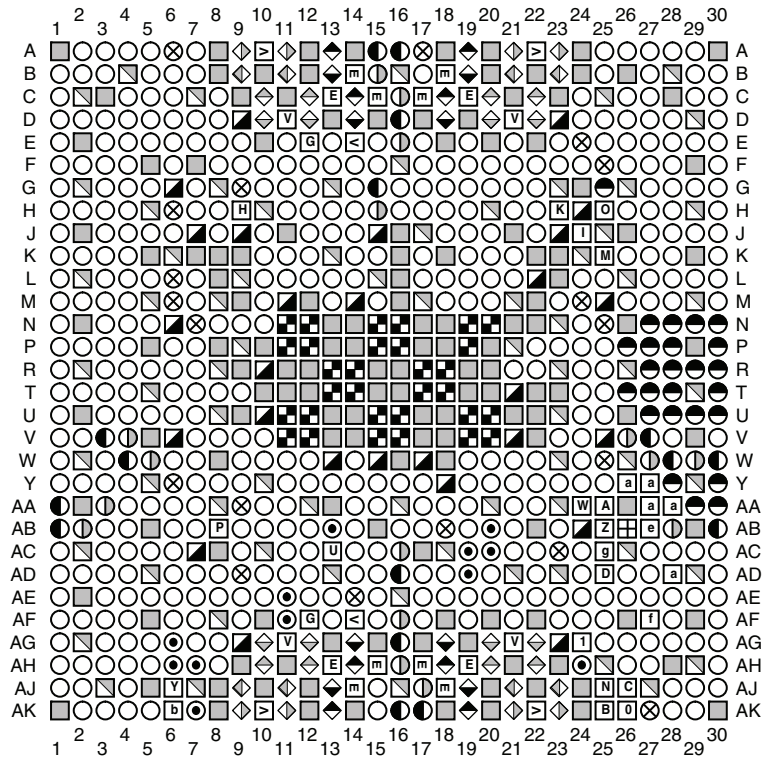


Figure 3-66: FG(G)900 Package—LX150 I/O Bank Diagram

FG(G)900 Package—LX150T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_#	⊗ VREF Ⓟ P_GCLK ● N_GCLK ⊙ D0 - D15 ● A0 - A25 ⓐ FCS / FWE / FOE / HDC / LDC Ⓤ RDWR_B_VREF	Ⓛ CCLK Ⓛ CSI Ⓛ CSO Ⓛ DIN Ⓛ DOUT_BUSY Ⓛ HSWAPEN Ⓛ INIT Ⓛ M1, M0 Ⓛ AWAKE	Ⓛ MGTAVCC Ⓛ MGTAVCCPLL Ⓛ MGTAVTTRX Ⓛ MGTAVTTRCAL Ⓛ MGTAVTTTX Ⓛ MGTREFCLK (P) Ⓛ MGTREFCLK (N) Ⓛ MGTRREF	Ⓛ MGTRXP Ⓛ MGTRXN Ⓛ MGTTXN Ⓛ MGTTXP Ⓛ PROGRAM_B_2 Ⓛ TCK Ⓛ TDI Ⓛ TDO Ⓛ TMS Ⓛ DONE_2 Ⓛ SUSPEND Ⓛ CMPCS_B_2 Ⓛ RFUSE	Ⓛ GND Ⓛ VFS Ⓛ VBATT Ⓛ VCCAUX Ⓛ VCCINT Ⓛ VCCO Ⓛ NC

UG385_c3_67_111909

Figure 3-67: FG(G)900 Package—LX150T Pinout Diagram

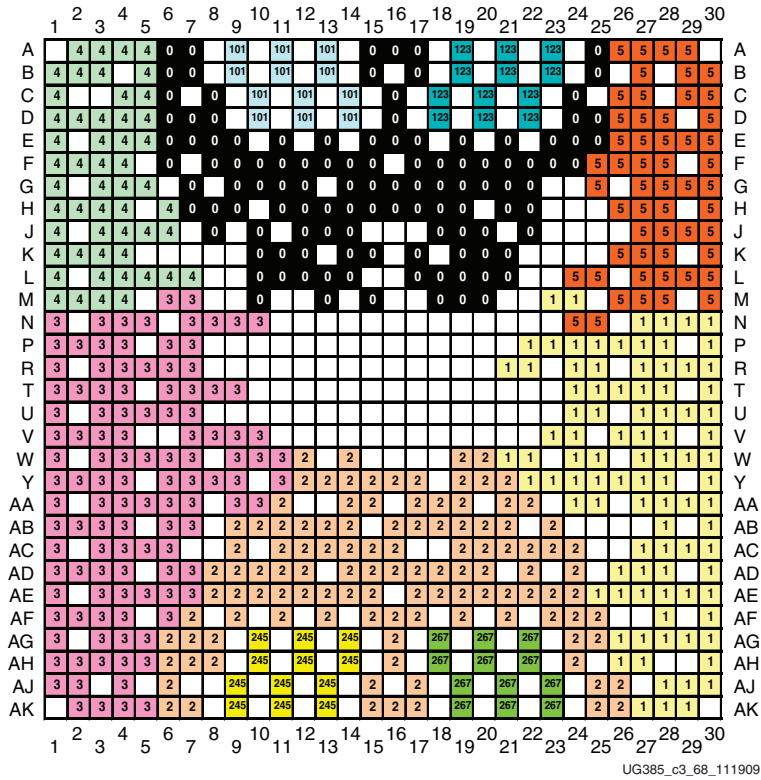


Figure 3-68: FG(G)900 Package—LX150T I/O Bank Diagram

Mechanical Drawings

Summary

This chapter provides mechanical drawings of the following Spartan-6 FPGA packages:

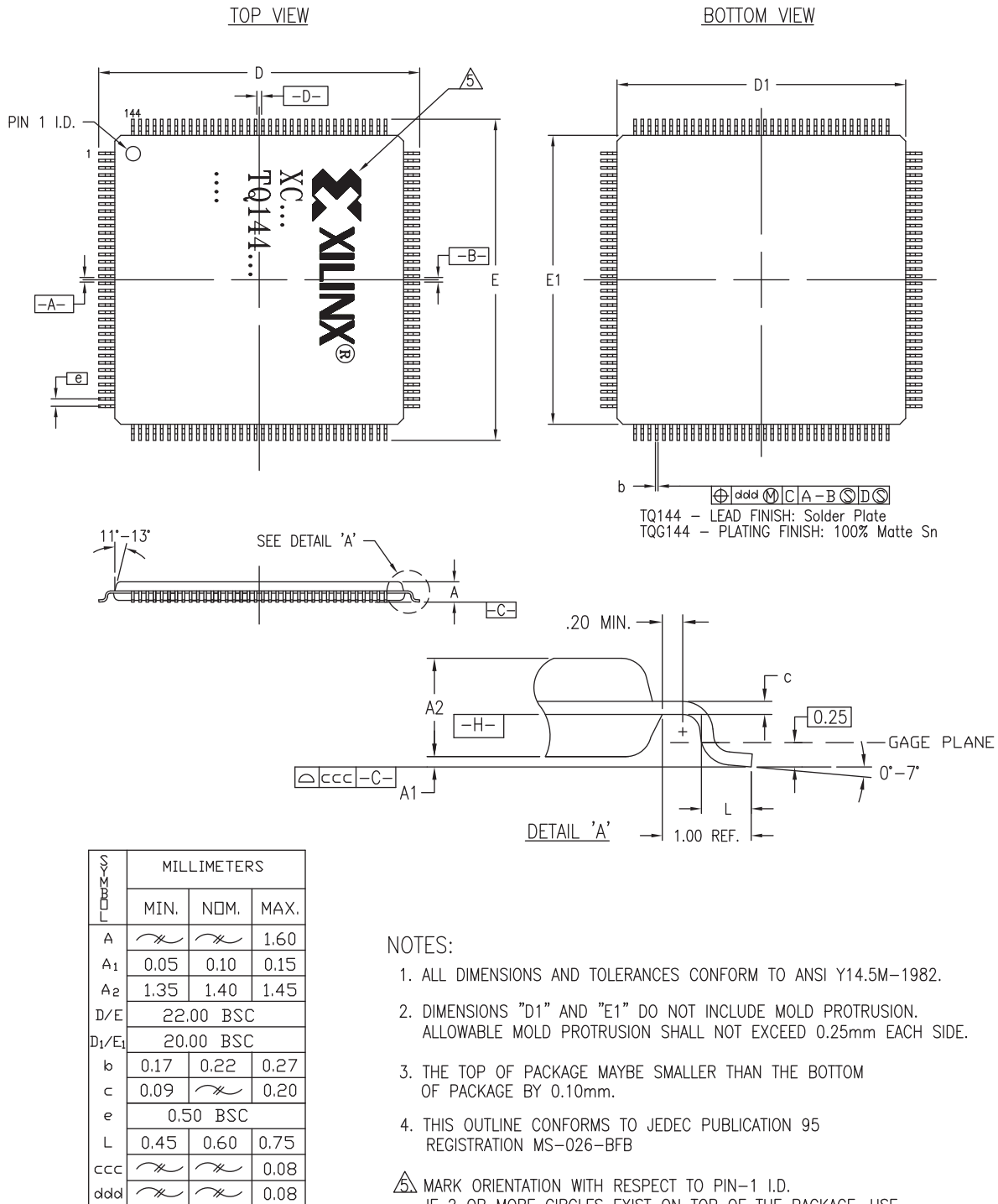
- [TQG144 Thin Quad Flat-Pack Package Specifications \(0.5 mm Pitch\)](#), page 334
- [CPG196 Chip-Scale BGA Package Specifications \(0.5 mm Pitch\)](#), page 335
- [CSG225 Chip-Scale BGA Package Specifications \(0.8 mm Pitch\)](#), page 336
- [FT\(G\)256 Fine-Pitch Thin BGA Package Specifications \(1.00 mm Pitch\)](#), page 337
- [CSG324 Chip-Scale BGA Package Specifications \(0.8 mm Pitch\)](#), page 338
- [FG\(G\)484 Fine-Pitch BGA Package Specifications \(1.00 mm Pitch\)](#), page 339
 - [FG\(G\)484 Fine-Pitch BGA Package - Corner Gate Mold \(CGM\)](#), page 339
 - [FG\(G\)484 Fine-Pitch BGA Package - Pin Gate Mold \(PGM\)](#), page 340
- [CS\(G\)484 Chip-Scale BGA Package Specifications \(0.8 mm Pitch\)](#), page 341
- [FG\(G\)676 Fine-Pitch BGA Package Specifications \(1.00 mm Pitch\)](#), page 342
 - [FG\(G\)676 Fine-Pitch BGA Package - Corner Gate Mold \(CGM\)](#), page 342
 - [FG\(G\)676 Fine-Pitch BGA Package - Pin Gate Mold \(PGM\)](#), page 343
- [FG\(G\)900 Chip-Scale BGA Package Specifications \(1.00 mm Pitch\)](#), page 344

Material Declaration Data Sheets (MDDS) are available for each package listed at:

<http://www.xilinx.com/support/documentation/spartan-6.htm#131532>

[UG393](#), *Spartan-6 FPGA PCB Design and Pin Planning Guide* includes recommendations for board layout, PCB design rules, and pin planning for these Spartan-6 FPGA packages.

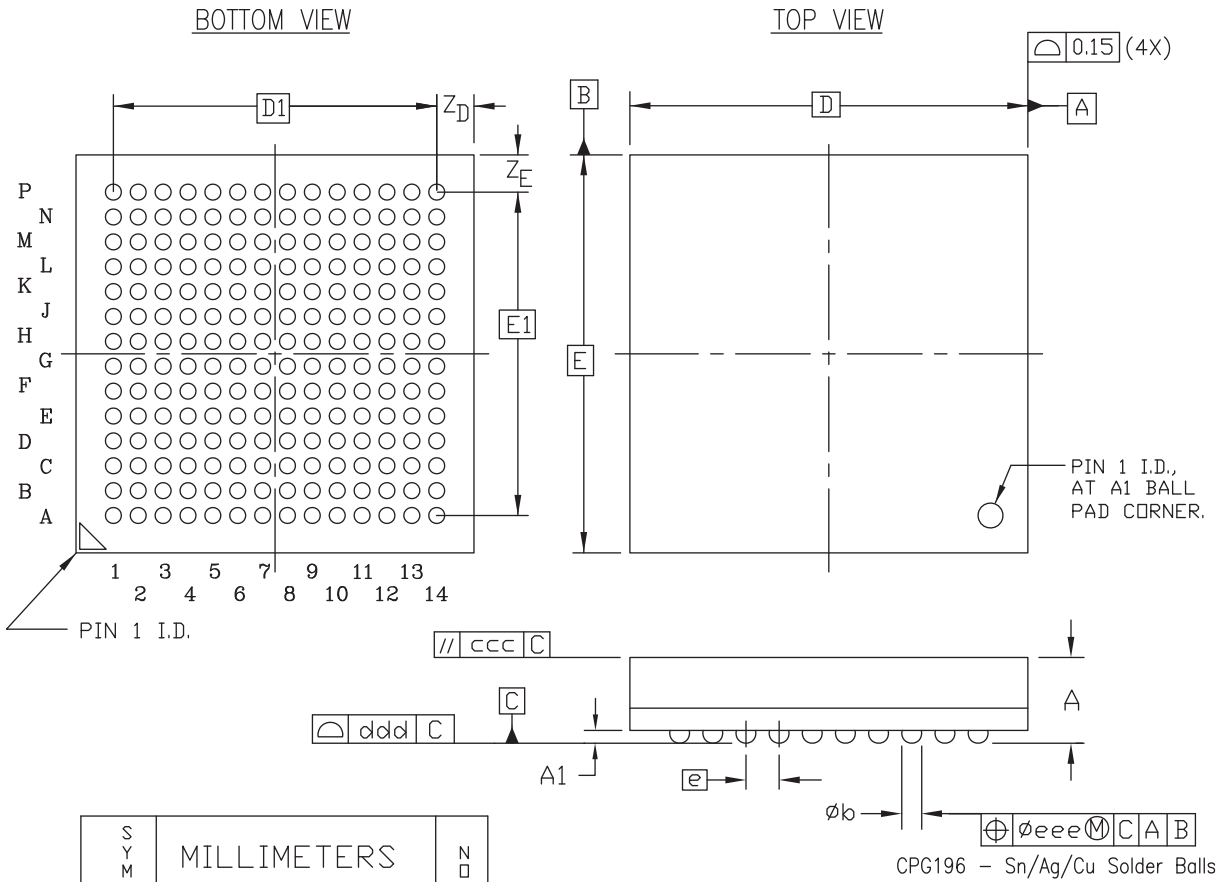
TQG144 Thin Quad Flat-Pack Package Specifications (0.5 mm Pitch)



ug385_c4_01_100509

Figure 4-1: TQG144 Thin Quad Flat-Pack Package

CPG196 Chip-Scale BGA Package Specifications (0.5 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	$\cancel{\text{---}}$	1.00	1.10	2
A ₁	0.15	0.20	0.25	
D/E	7.90	8.00	8.10	
D ₁ /E ₁	6.50 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.10	
ddd	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.08	
eee	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.15	
Z _D /Z _E	0.60	0.75	0.90	
M	14			

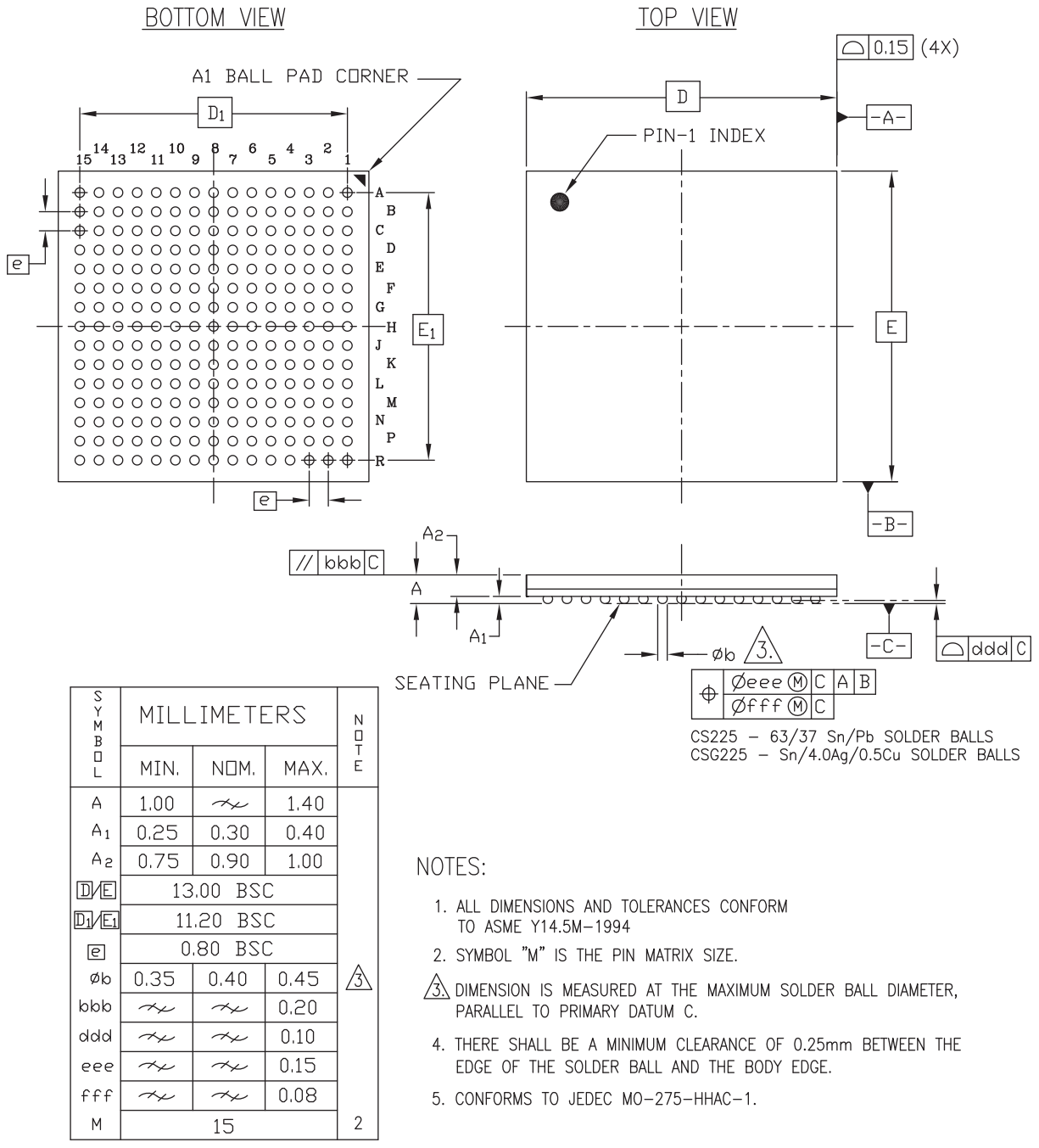
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-275

ug385_c4_02_100709

Figure 4-2: CPG196 Chip-Scale BGA Package

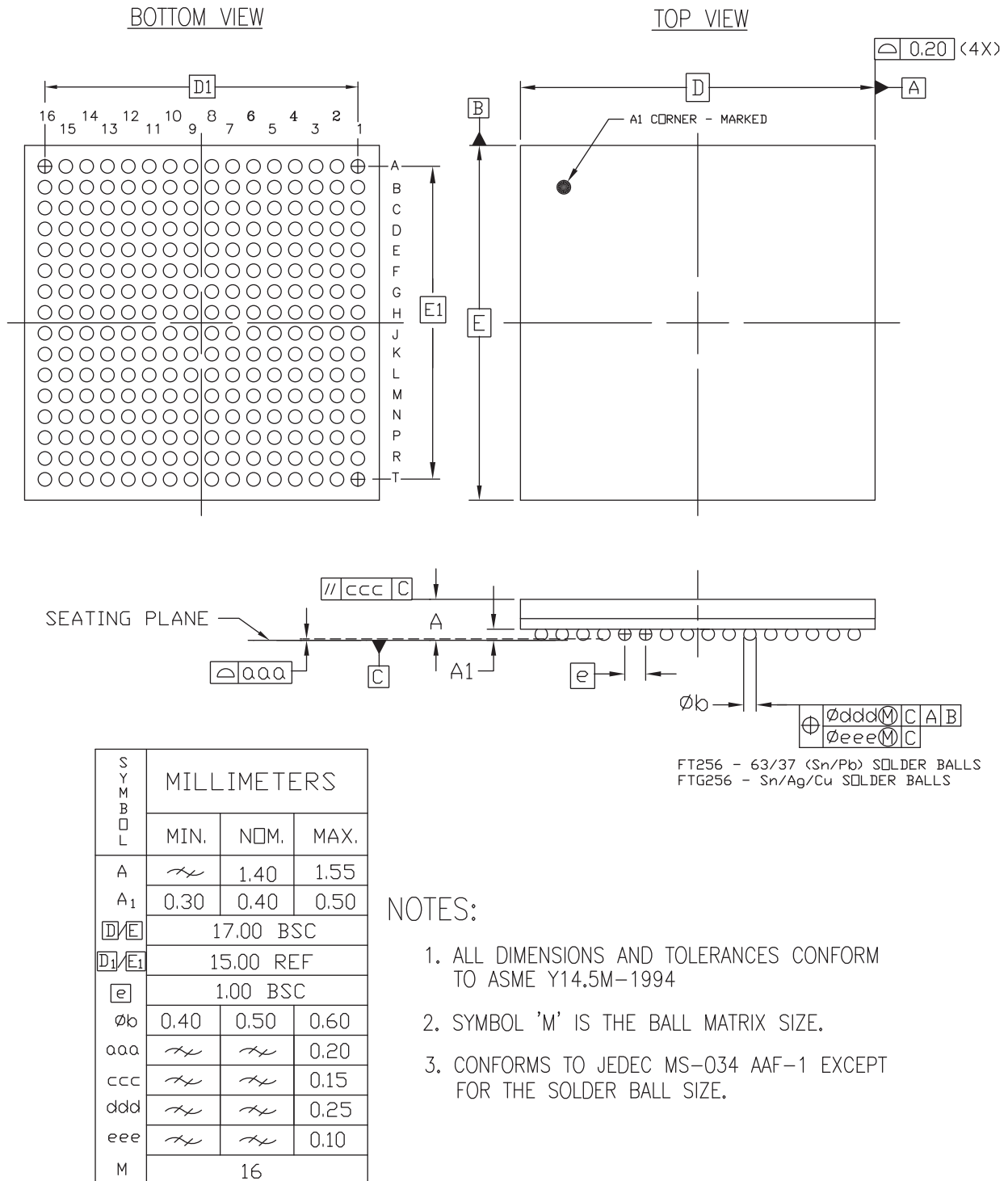
CSG225 Chip-Scale BGA Package Specifications (0.8 mm Pitch)



UG385_c4_03_110509

Figure 4-3: CSG225 Chip-Scale BGA Package

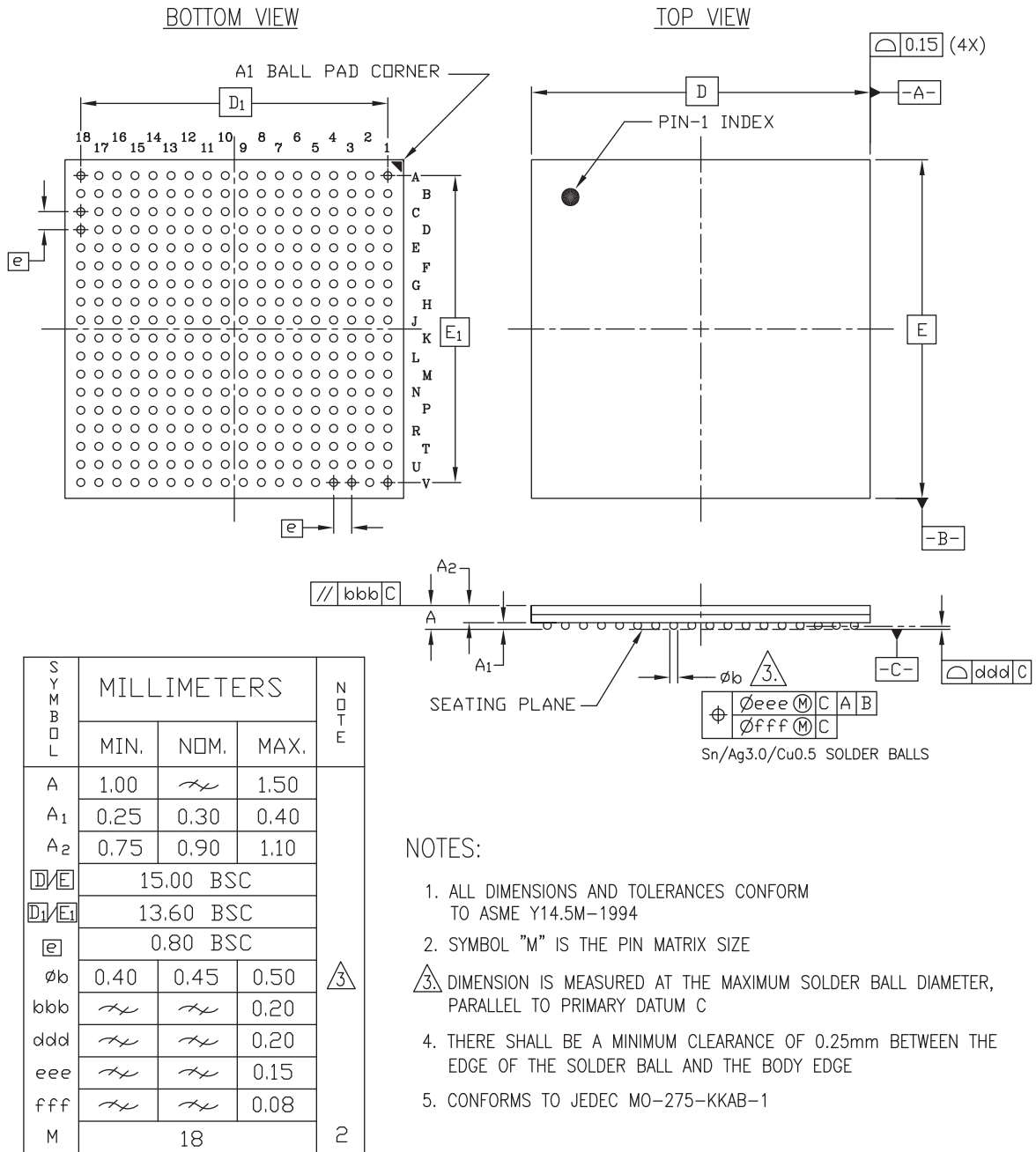
FT(G)256 Fine-Pitch Thin BGA Package Specifications (1.00 mm Pitch)



ug385_e4_04_021411

Figure 4-4: FT(G)256 Fine-Pitch Thin BGA Package

CSG324 Chip-Scale BGA Package Specifications (0.8 mm Pitch)

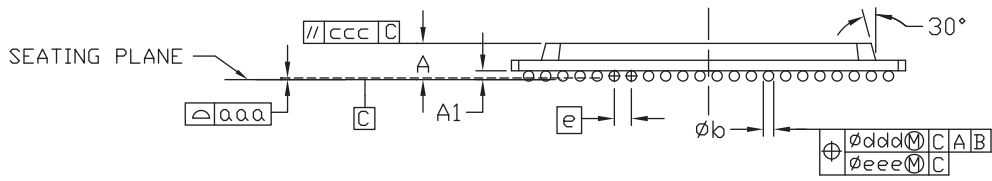
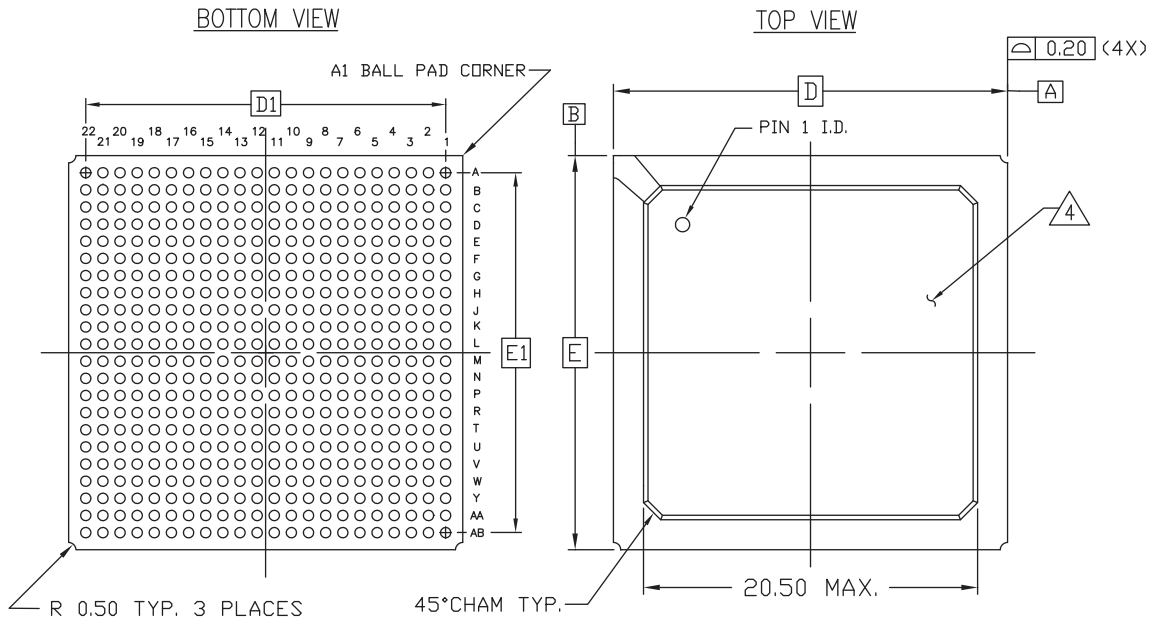


ug385_c4_05_110509

Figure 4-5: CSG324 Chip-Scale BGA Package

FG(G)484 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

FG(G)484
 △CGM



FG484 - Pb/Sn SOLDER BALLS
 FGG484 - Sn/Ag/Cu

SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.60	3
A ₁	0.35	0.50	0.60	
D/E	23.00 BSC			2
D ₁ /E ₁	21.00 REF			
e	1.00 BSC			
φ _b	0.50	0.60	0.70	
aaa	↯	↯	0.20	
ccc	↯	↯	0.35	
ddd	↯	↯	0.30	
eee	↯	↯	0.10	
M	22			

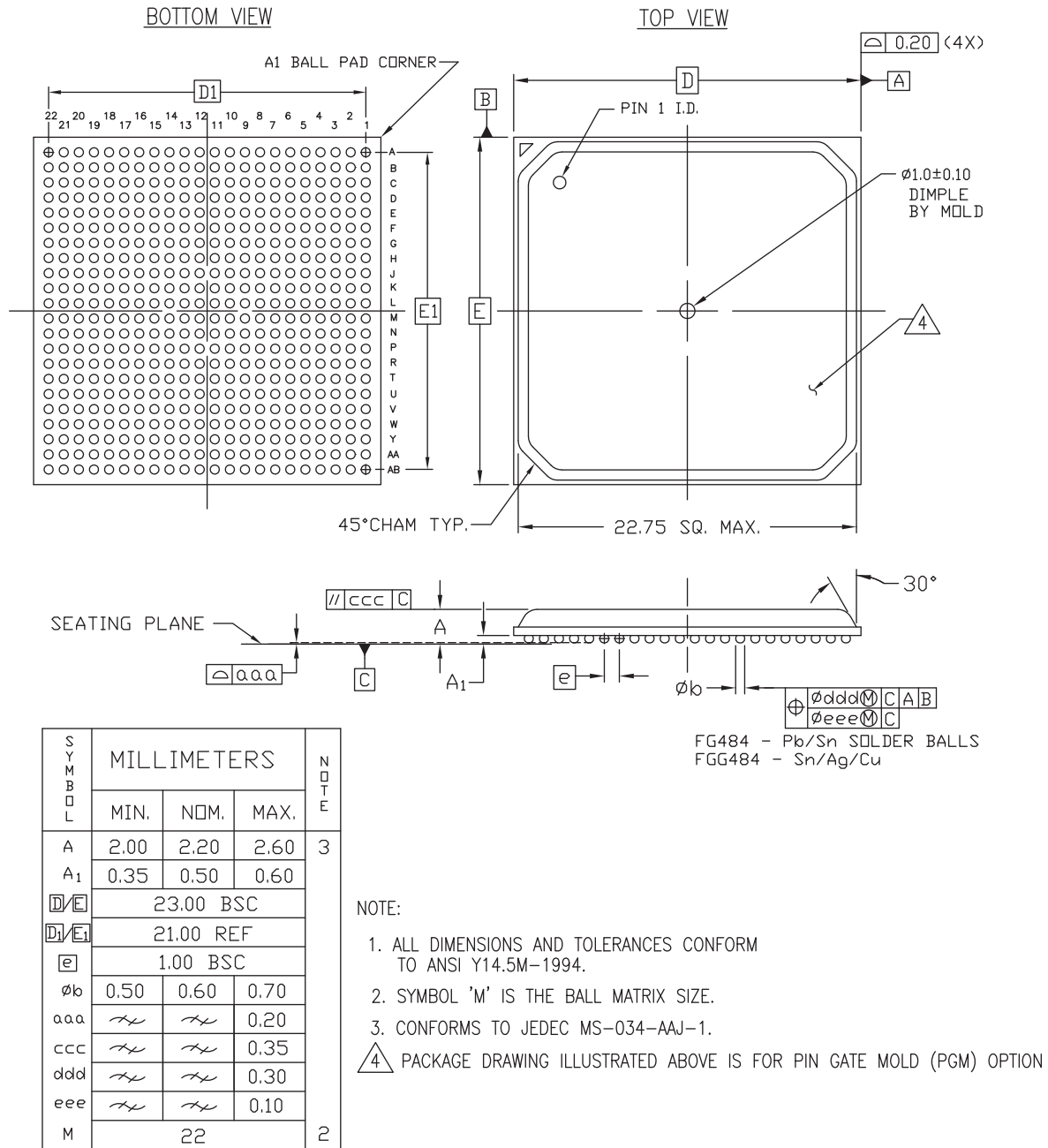
- NOTE:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
 2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
 3. CONFORMS TO JEDEC MS-034-AAJ-1.
 - △ PACKAGE DRAWING ILLUSTRATED ABOVE IS FOR CORNER GATE MOLD (CGM)
 5. SEE NEXT PAGE FOR PIN GATE MOLD (PGM) PACKAGE OPTION

ug385_c4_06_050514

Figure 4-5: FG(G)484 Fine-Pitch BGA Package - Corner Gate Mold (CGM)

FG(G)484

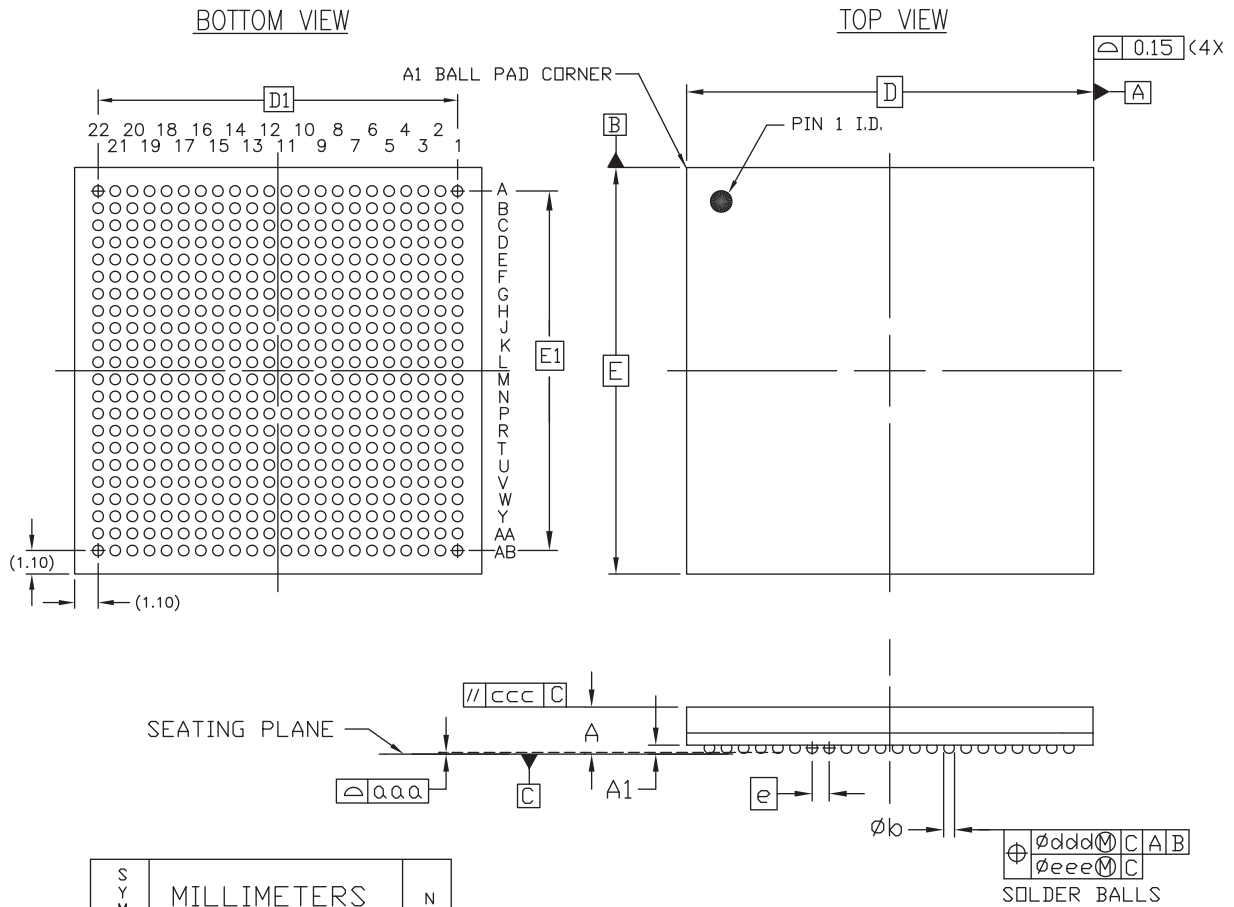
△ PGM



ug385_c4_16_050514

Figure 4-6: FG(G)484 Fine-Pitch BGA Package - Pin Gate Mold (PGM)

CS(G)484 Chip-Scale BGA Package Specifications (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.57	1.67	1.80	2
A ₁	0.30	0.38	0.45	
$\frac{D}{E}$	19.00 BSC			
$\frac{D_1}{E_1}$	16.80 BSC			
$\frac{E}{E_1}$	0.80 BSC			
ϕb	0.40	0.50	0.55	
aaa	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.20	
ccc	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.20	
ddd	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.15	
eee	$\cancel{\text{---}}$	$\cancel{\text{---}}$	0.08	
M	22			

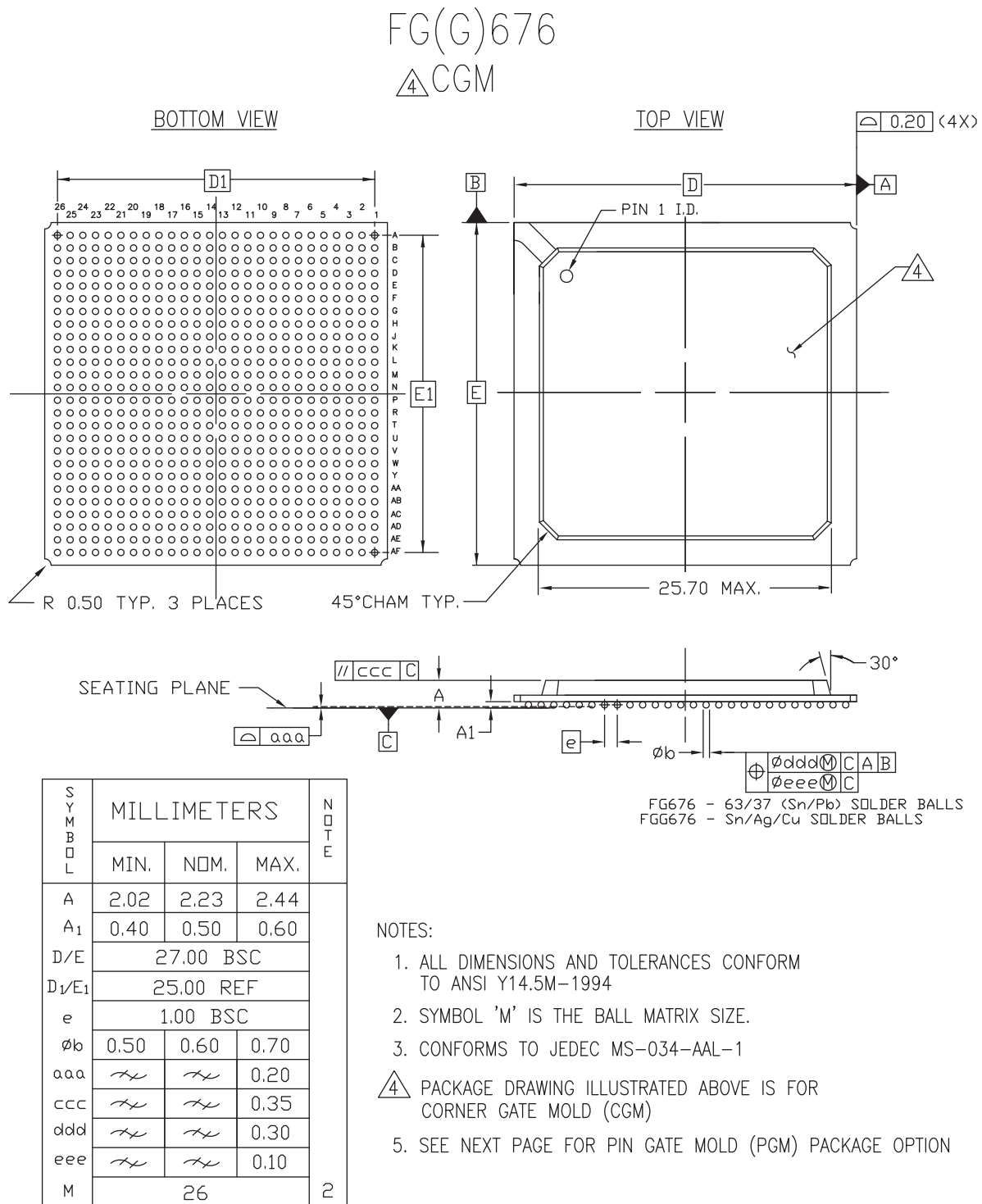
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO-275-PPAA-2.

ug385_c4_07_061809

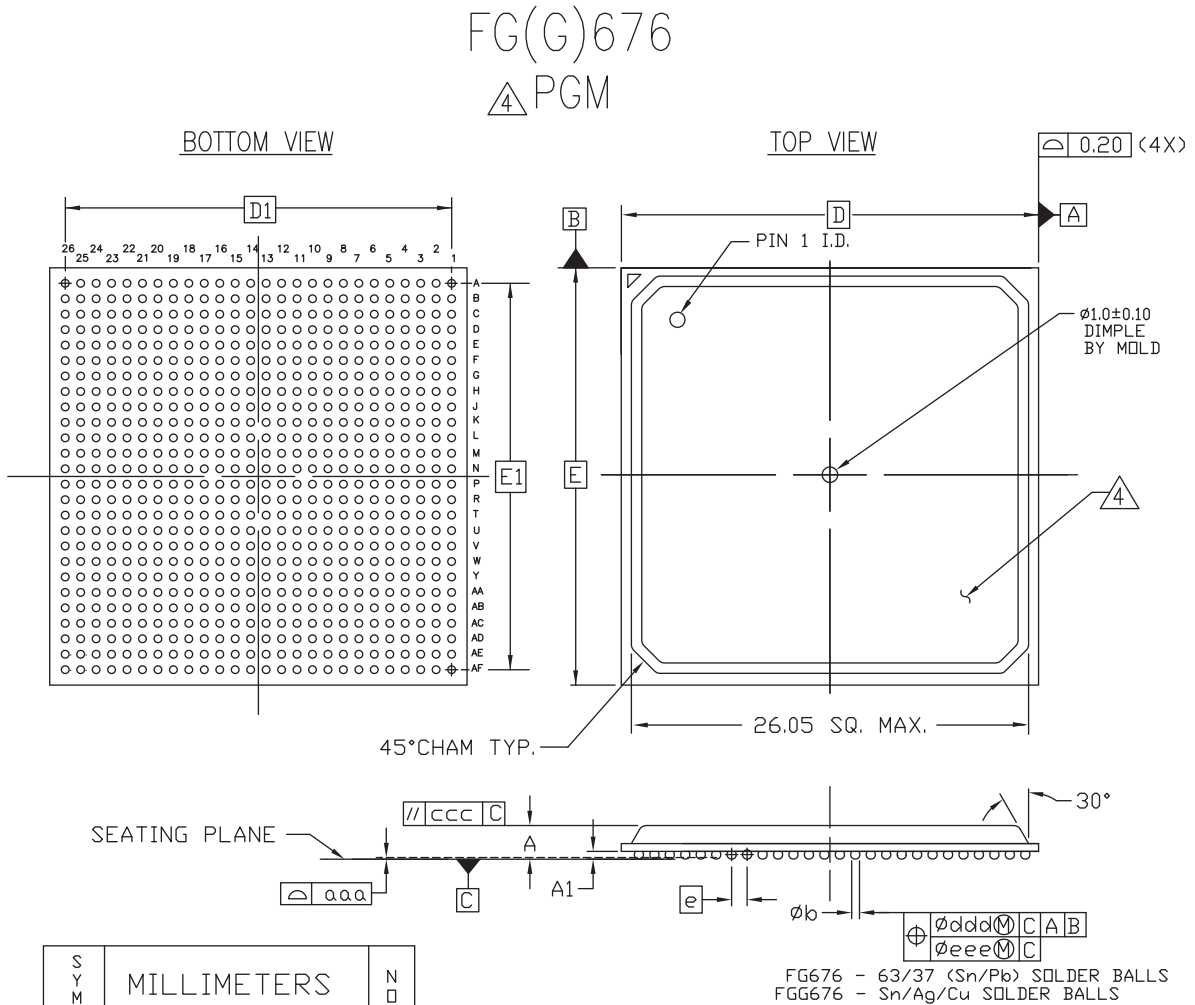
Figure 4-7: CS(G)484 Chip-Scale BGA Package

FG(G)676 Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug385_c4_08_050514

Figure 4-8: FG(G)676 Fine-Pitch BGA Package - Corner Gate Mold (CGM)



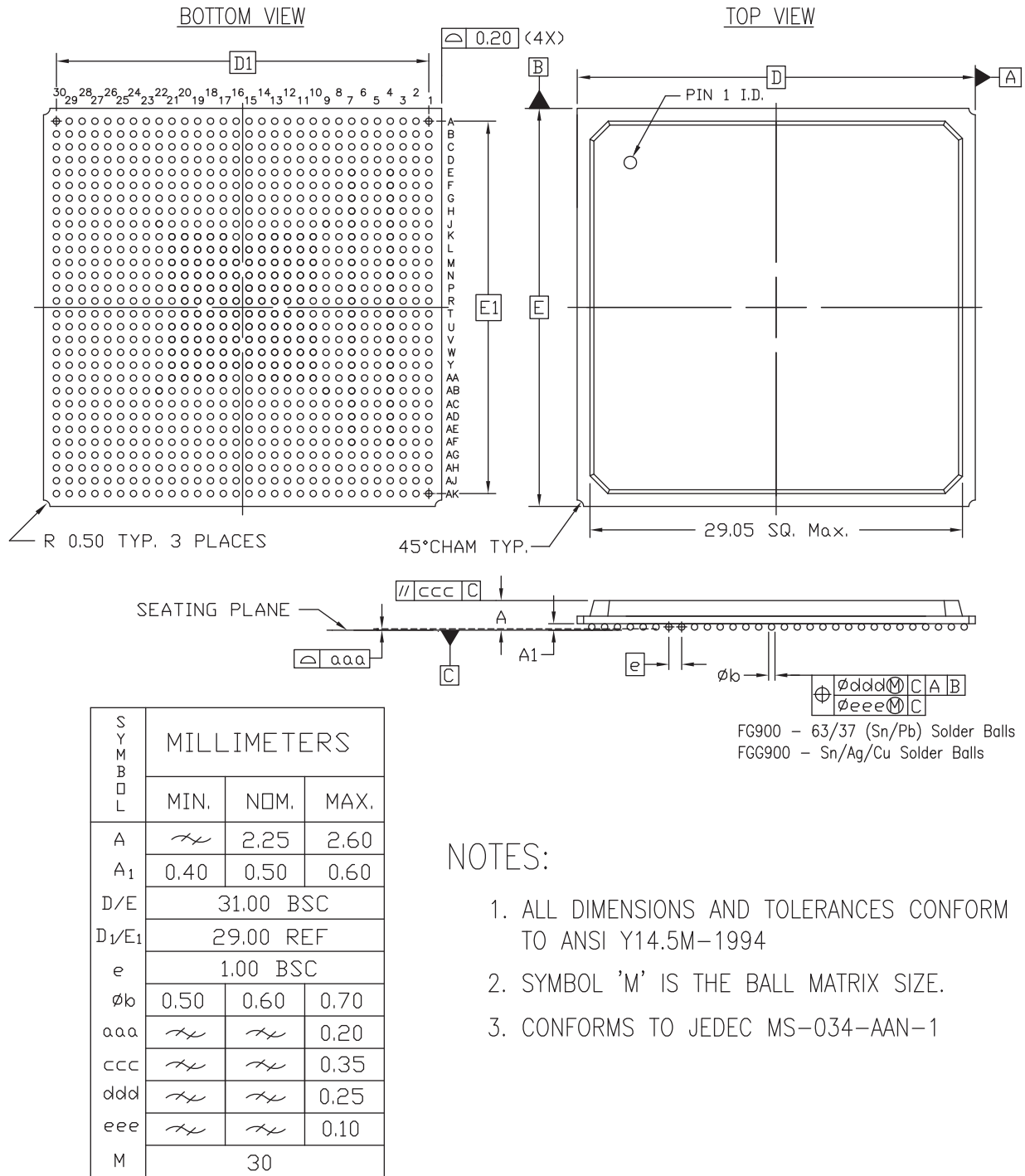
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
 2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
 3. CONFORMS TO JEDEC MS-034-AAL-1
- △ PACKAGE DRAWING ILLUSTRATED ABOVE IS FOR PIN GATE MOLD (PGM) OPTION

ug385_c4_19_050514

Figure 4-9: FG(G)676 Fine-Pitch BGA Package - Pin Gate Mold (PGM)

FG(G)900 Chip-Scale BGA Package Specifications (1.00 mm Pitch)



ug385_c4_09_111809

Figure 4-10: FG(G)900 Chip-Scale BGA Package

Thermal Specifications

Summary

This chapter provides thermal data associated with Spartan-6 FPGA packages. The following topics are discussed:

- [Introduction](#)
- [Cavity-Up Plastic BGA Packages](#)
- [Support for Compact Thermal Models \(CTM\)](#)
- [Soldering Guidelines](#)
- [References](#)

Introduction

Spartan-6 devices are offered in a wide variety of packages. The suite of packages is used to address the various power requirements of the Spartan-6 devices. All Spartan-6 devices are implemented in the 45 nm process technology

All Spartan-6 devices feature versatile SelectIO™ resources that support a variety of I/O standards. They also include DSPs and other traditional features and blocks (such as block RAM) contained in earlier Spartan and Virtex® products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 45 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured Spartan-6 FPGA design that exploits the internal logic speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Spartan-6 devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Table 5-1 shows the thermal resistance data for Spartan-6 devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

Note: The data in Table 5-1 is for device/package comparison purposes only. Do not apply directly to your system design. Attempts to recreate this data are only valid using the steady-state measurement technique outlined in JESD51-2a, JESD51-6, and JESD51-8.

- Thermal data is available on the Xilinx website at:
<http://www.xilinx.com/cgi-bin/thermal/thermal.pl>.
- Compact package thermal models for these products are available on the Xilinx support download center (under the Device Model tab) at:
<http://www.xilinx.com/support/download/index.htm>

Table 5-1: Thermal Resistance Data—All Devices

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
CPG196	8 x 8	LX4	58.5	18.6	8.8	49.9	46.7	44.9
		LX9	58.5	18.6	8.8	49.9	46.7	44.9
		LX16	36.9	17.1	7.8	31.5	29.3	28.2
TQG144	20 x 20	LX4	38.4	26.7	12.5	33.1	31.5	30.6
		LX9	38.4	26.7	12.5	33.1	31.5	30.6
CSG225	13 x 13	LX4	32.2	17.4	10.6	26.7	25.1	24.2
		LX9	32.2	17.4	10.6	26.7	25.1	24.2
		LX16	30.6	15.6	9.4	27.1	23.5	22.7
FT(G)256	17 x 17	LX9	31.9	22.7	10.0	26.9	25.3	24.4
		LX16	30.2	20.1	8.6	25.2	23.6	22.8
		LX25	26.8	16.6	6.8	21.9	20.3	19.5
CSG324	15 x 15	LX9	30.5	18.0	10.6	26.2	24.7	23.9
		LX16	27.8	13.7	8.9	22.5	21.1	20.0
		LX25	26.2	12.5	7.1	20.9	19.4	18.6
		LX25T	26.2	12.5	7.1	20.9	19.4	18.6
		LX45	22.6	8.8	5.3	17.3	15.9	15.1
		LX45T	22.6	8.8	5.3	17.3	15.9	15.1

Table 5-1: Thermal Resistance Data—All Devices (Cont'd)

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FG(G)484	23 x 23	LX25	21.0	13.4	8.1	17.2	15.9	15.2
		LX25T	21.0	13.4	8.1	17.2	15.9	15.2
		LX45	19.1	10.0	6.0	14.3	13.0	12.4
		LX45T	19.1	10.0	6.0	14.3	13.0	12.4
		LX75	17.2	8.0	4.7	12.5	11.3	10.6
		LX75T	17.2	8.0	4.7	12.5	11.3	10.6
		LX100	16.4	7.0	4.2	11.7	10.5	9.8
		LX100T	16.4	7.0	4.2	11.7	10.5	9.8
		LX150	15.8	6.3	3.7	11.1	9.9	9.3
		LX150T	15.8	6.3	3.7	11.1	9.9	9.3
CS(G)484	19 x 19	LX45	20.3	9.1	4.7	15.5	14.4	13.8
		LX45T	20.3	9.1	4.7	15.5	14.4	13.8
		LX75	18.5	7.4	3.6	13.7	12.4	11.7
		LX75T	18.5	7.4	3.6	13.7	12.4	11.7
		LX100	17.6	6.5	2.9	12.9	11.6	11.0
		LX100T	17.6	6.5	2.9	12.9	11.6	11.0
		LX150	17.0	5.9	2.7	12.2	10.9	10.3
		LX150T	17.0	5.9	2.7	12.2	10.9	10.3
FG(G)676	27 x 27	LX45	17.6	9.6	5.9	14.5	12.2	11.6
		LX75	15.9	7.5	4.5	11.6	10.5	9.9
		LX75T	15.9	7.5	4.5	11.6	10.5	9.9
		LX100	15.0	6.6	4.0	11.0	9.6	9.1
		LX100T	15.0	6.6	4.0	11.0	9.6	9.1
		LX150	14.4	6.0	3.5	10.2	9.7	8.5
		LX150T	14.4	6.0	3.5	10.2	9.7	8.5
		LX150T	14.4	6.0	3.5	10.2	9.7	8.5
FG(G)900	31 x 31	LX100T	15.0	7.3	4.4	10.8	9.7	9.1
		LX150	14.2	6.5	3.8	10.0	8.9	8.5
		LX150T	14.2	6.5	3.8	10.0	8.9	8.5

Package Strategy

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields.

The substrate is made of a multilayer BT (bismaleimide triazene) epoxy-based material. Power and ground pins are grouped together and the signal pins are assigned in the perimeter format for ease of routing on to the board. The package is offered in a die up format and contains a wirebonded device that is covered with a mold compound.

Package Construction

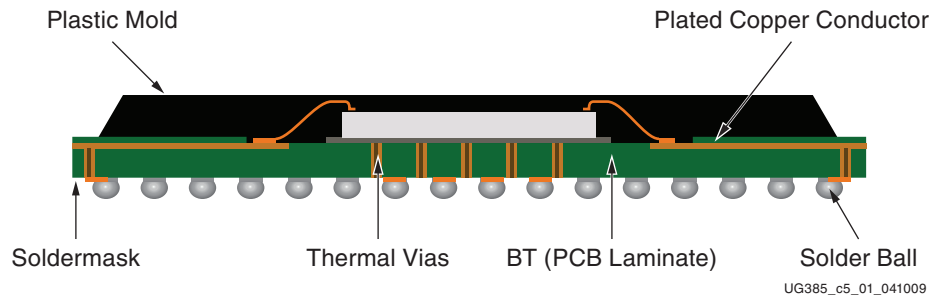


Figure 5-1: Cavity-Up Ball Grid Array Package

As shown in the cross section of [Figure 5-1](#), the BGA package contains a wire bonded die on a single-core printed circuit board with an overmold. Beneath the die are the thermal vias which can dissipate the heat through a portion of the solder ball array and ultimately into the power and ground planes of the system circuit board. This thermal management technique provides better thermal dissipation than a standard PQFP package. Metal planes also distribute the heat across the entire package, enabling a 15–20% decrease in thermal resistance to the case.

Key Features/Advantages of Cavity-Up BGA Packages

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Chip Scale Packages

Chip Scale (CSP) packages meet the demands of miniaturization while offering improved performance. Applications for CSP packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption/dissipation must be low. By employing Spartan-6 FPGA CSP packages, system designers can dramatically reduce board real estate. Xilinx CSP packages are rigid BT-based substrates (see [Figure 5-2](#)).

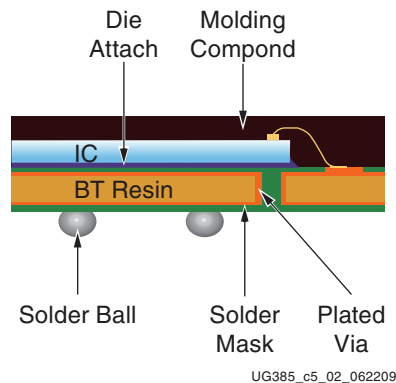


Figure 5-2: Rigid BT-Based Substrate CSP Packages

Key Features/Advantages of CSP Packages

- An extremely small form factor which significantly reduces board real estate for such applications as portable and wireless designs and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light-weight package

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for Spartan-6 devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for Spartan-6 FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all Spartan-6 devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-3.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center at: <http://www.xilinx.com/support/download/index.htm>.

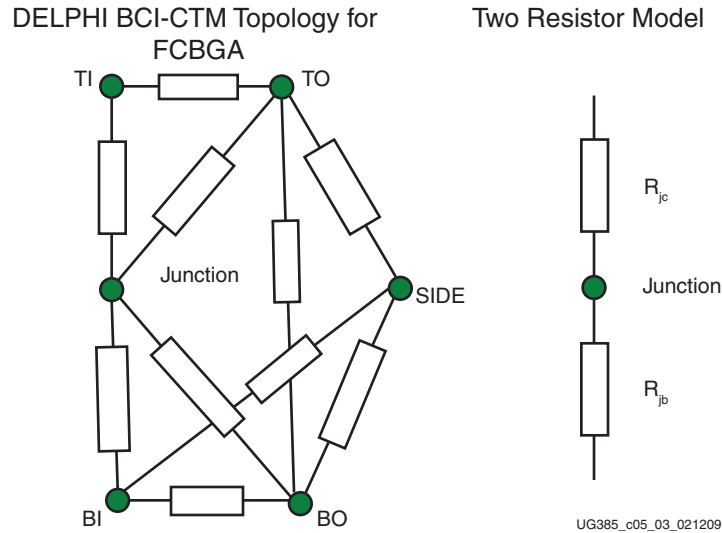


Figure 5-3: Thermal Model Topologies

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepack (version 4.2 and above) format.

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

Note: Xilinx recommends that customers qualify their custom PCB assembly processes using package samples. [UG112: Device Package User Guide](#) contains further details on recommended assembly procedures.

The primary phases of the reflow process are:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

In a Pb-free soldering system, the sequences are the same. However, for the Pb-free soldering system, higher reflow temperature is applied. The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 220°C for standard packages and 245–260°C for Pb-free packages (package size dependent). For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package

moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

Figure 5-4 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

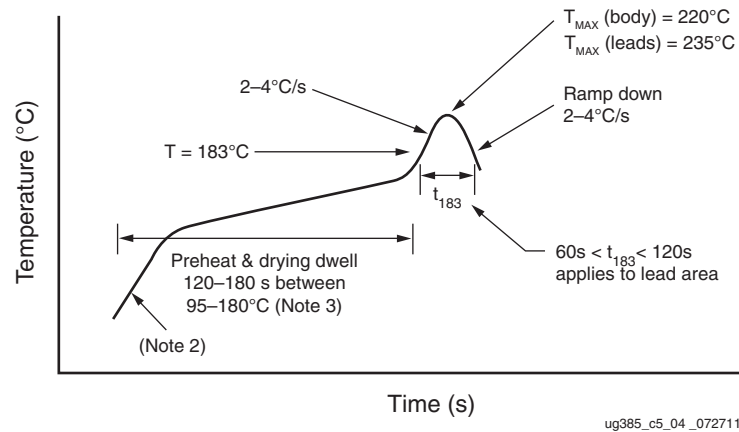


Figure 5-4: Typical Conditions for IR Reflow Soldering of Sn/Pb Solder

Notes for Figure 5-4:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2–4°C/s
3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses a matte Sn lead finish for lead-frame packages and SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (245°C–260°C) required by Pb-free soldering processes.

Lead frame packages (TQG) from Xilinx are backwards compatible, that is the component can be soldered with Sn/Pb solder using a Sn/Pb soldering process. Lead-frame packages from Xilinx use a matte Sn plating on the leads which is compatible with Pb-free and Sn/Pb soldering alloys.

Xilinx does not recommend soldering BGA packages (CPG, CSG, FTG, FGG) with SnPb solder using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs

using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

[Table 5-2](#) and [Figure 5-5](#) provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders ([Figure 5-5](#)). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C and above. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to [Table 5-2](#) for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-2: Pb-Free Reflow Soldering Guidelines

Profile Feature	Convection, IR/Convection
Ramp-up rate	3°C/s maximum
Preheat Temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak Temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, components mixture)
Peak Temperature (body)	245°C–260°C, package body size dependent (reference Table 5-3)
Ramp-down Rate	6°C/s maximum
Time 25°C to Peak Temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

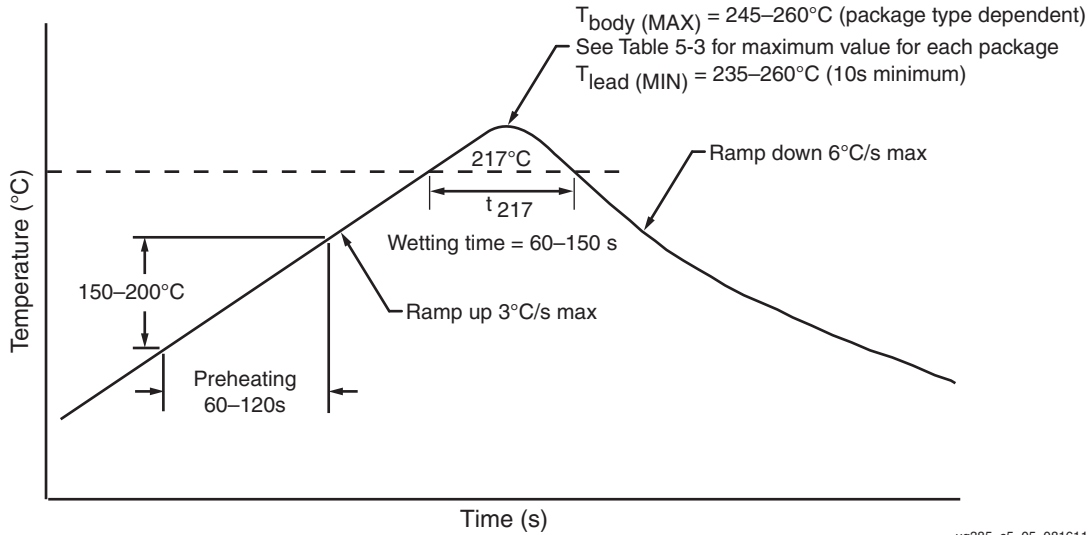


Figure 5-5: Typical Conditions for Pb-Free Reflow Soldering

Table 5-3: Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages (Based on J-STD-020 Standard)

Package		Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
Lead Frame			
TQFP	TQG144	260°C	3
BGA			
BGA	FTG256	260°C	3
	FGG484	250°C	3
	FGG676		
	FGG900		
Chip Scale	CPG196	260°C	3
	CSG225		
	CSG324		
	CSG484		

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board ($<10^\circ\text{C}$) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than 1°C/s during the preheating and soaking stages, in combination with a heating rate of not more than 3°C/s throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually

between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

References

The following Xilinx links are to additional information on topics outlined in this chapter.

- [UG394](#), *Spartan-6 FPGA Power Management User Guide* contains more information on power analysis and optimization.
- [UG112](#), *Device Package User Guide* contains general information on Xilinx packaging.
- More information on Xilinx Pb-free solutions is available at:
http://www.xilinx.com/system_resources/lead_free/index.htm.
- [XAPP427](#): *Implementation and Solder Reflow Guidelines for Pb-Free Packages* provides further information on the Pb-free reflow process.

The following websites contain additional information on heat management and contact information.

- <http://www.wakefield.com>
- <http://www.aavidthermalloy.com>
- <http://www.qats.com>

Refer to the following websites for interface material sources:

- Henkel Electronics: <http://www.henkel.com/electronics.htm>
- Bergquist Company: <http://www.bergquistcompany.com>
- AOS Thermal Compound: <http://www.aosco.com>
- Chomerics: <http://www.chomerics.com>
- Kester: <http://www.kester.com>

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor Graphics Flotherm:
<http://www.mentor.com/products/mechanical/flomerics>
- ANSYS Icepak:
<http://www.ansys.com/Products/Simulation+Technology/Fluid+Dynamics/ANSYS+Icepak>

Package Marking

The Spartan-6 devices in the TQ, CS, and FG packages have package top-markings similar to the example shown in Figure 6-1 and explained in Table 6-1. In BGA packages, the ball A1 indicator is in the top-left corner. In the TQG144 packages, the pin P1 indicator is in the bottom left of the mark.

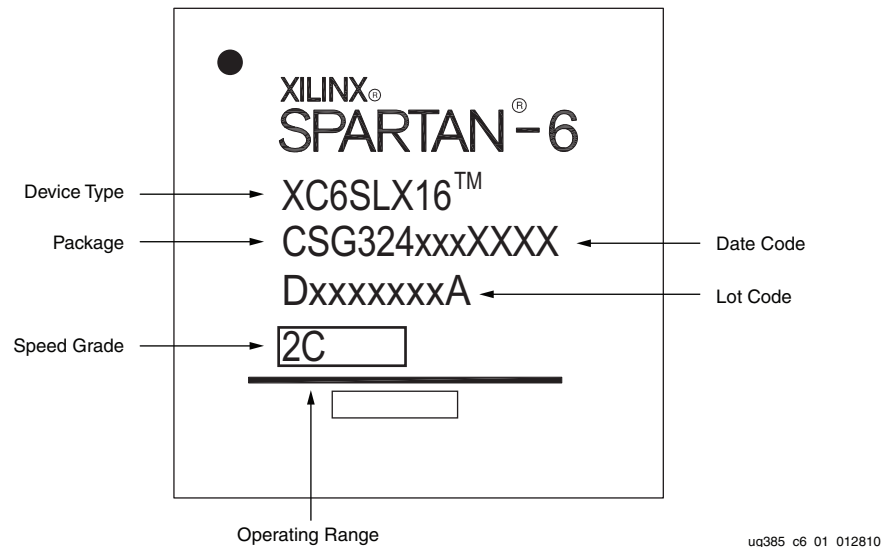


Figure 6-1: Spartan-6 Device Package Marking

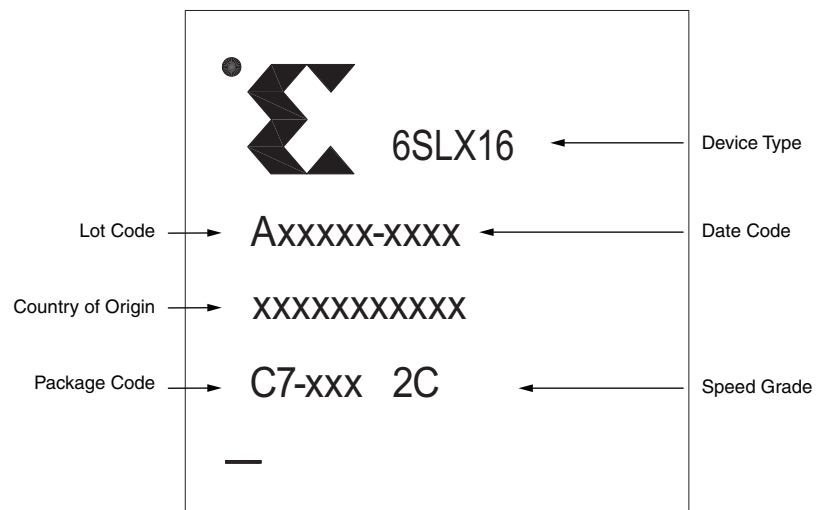
Table 6-1: Xilinx Device Marking Definition—Example

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Spartan-6 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A G in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree .
3rd Line	Ten alphanumeric characters for Assembly and Lot information. The last digit is usually an A or an M.

Table 6-1: Xilinx Device Marking Definition—Example (Cont'd)

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	L1C	The <i>L1C</i> indicates a lower-power (1.0V core voltage) device with a -1L speed grade.
	2C-xxxx	The <i>xxxx</i> indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	2C-ES	An <i>ES</i> , when present, indicates an Engineering Sample.

The Spartan-6 devices in the CPG196 package have package top-markings similar to the example shown in Figure 6-2 and explained in Table 6-2. The package markings are abbreviated.



ug385_c6_02_100510

Figure 6-2: Spartan-6 Device CPG196 Package Marking

Table 6-2: Xilinx CPG196 Device Marking Definition—Example

Item	Definition	
1st Line	Xilinx Logo, Device type. Abbreviated without the leading XC.	
2nd Line	Lot code and date code (abbreviated).	
3rd Line	Country of Origin	
4th Line	Package code (C7 = CPG196), circuit design revision, the location code for the wafer fab, the geometry code, and the device speed grade and temperature (in this example: 2C). Other variations for the 4th line:	
	<i>L1C</i>	An <i>L1C</i> indicates a lower-power (1.0V core voltage) device with a -1L speed grade.
	2C ES	An <i>ES</i> , when present, indicates an Engineering Sample.

Density Migration

Introduction

Spartan-6 FPGA pinouts are 100% compatible across density in the same package and within the same set of LX or LXT devices. Designs implemented in a given device/package combination can be migrated up or down in density without changing a board layout. The guidelines in this chapter facilitate migration between Spartan-6 devices. For general information on pin planning, see the I/O Pin and Clock Planning chapter in [UG393, *Spartan-6 FPGA PCB Design and Pin Planning Guide*](#).

Compatibility

A common layout for multiple devices using the same package is the goal of pinout compatibility. Generally, the only difference between densities is the number or placement of No Connects (NCs) within the package. In Spartan-6 FPGAs, all pins maintain their same names from one density to the next. However, there are some unique situations where pin names change because of differences in functionality from one density to the next, as explained in the [Special Cases](#) section.

All Spartan-6 LX devices are pinout compatible in the same package, and all Spartan-6 LXT devices are pinout compatible in the same package. The Spartan-6 LX and Spartan-6 LXT devices are not pinout compatible in the same package due to the additional GTP transceiver pins in the LXT family. Although many of the other pins are in the same location, there can be significant differences between LX and LXT devices, and migration between devices requires a different board layout.

Package compatibility refers only to changing densities within a common package. No compatibility between packages, even between packages with the same amount of pins, such as the FG(G)484 and the CS(G)484, is implied. However, a design using one package can be implemented in another package with a similar quality of results, since the pin locations are similar. The Spartan-6 LX devices and LXT devices use the same package designators for common packages, such as FG(G)484, even though the pinouts are different. There is no difference in pinout between the Pb-free packages and the leaded equivalent, such as the FGG484 and the FG484.

The Spartan-6 FPGA pinouts are optimized for the unique Spartan-6 FPGA architecture. No compatibility is implied between the Spartan-6 FPGA pinouts and any other FPGA family.

The Spartan-6 FPGA pinout compatibility is summarized in [Table 7-1](#).

Table 7-1: Pinout Compatibility Summary

Device	Device	Compatible?
Any LX device, any package	Any LX device, any package	Yes
Any LXT device, any package	Any LXT device, any package	Yes
LX device	LXT device	No
Any device and package, Pb-free	Same device and package, Pb-equivalent	Yes
Any package	Different package	No
Spartan-6 FPGA	Other FPGAs	No

No Connects

The primary difference between densities in the same package is the number or location of the No Connects (NCs). To make a board layout compatible, refer to [Chapter 2, Pinout Tables](#) and prohibit the use of any pin where a potential target density is shown in the NC column.

Typically, the largest device in a package has zero No Connects and smaller devices add NCs as the size limits the amount of I/O available. In the Spartan-6 family, there are instances where a larger density has fewer I/O than the smaller device in the same package. Referring to [Table 1-4, page 16](#) for example, the I/O available is less than for a smaller device for the LX25 and LX45 in the CSG324, the LX75 in the FG(G)484, and the LX75T in the CS(G)484 and FG(G)484. In these instances, the available I/O count in banks 0 and 2 (top and bottom) is reduced in the larger device. The I/O count per bank is shown in [Table 1-5, page 17](#).

No Connects can be in different locations in one density versus another. To create a compatible pinout across densities, all the potential NCs should be prohibited, which can result in fewer usable I/O than the number available in the device with the fewest I/O. For example, in the CS(G)484 package, out of the 338 I/O in the two largest devices (LX100 and LX150), the LX75 has 10 NCs (328 I/O) and the LX45 has 18 NCs (320 I/O). Since the NCs are on different pins, all 28 NCs are used to create a 310 I/O pinout that can be migrated between the LX45 and LX75.

No Connects are almost always on single-purpose pins. Dual-purpose pins, including memory controller pins and configuration pins, are used consistently across all densities in a package. The only exception is the CSG225 package, because the LX4 does not include the memory controllers and does not support parallel configuration.

Table 7-2 and Table 7-3 show the number of I/Os to produce compatibility across various density ranges in a package. For all the ranges not noted, the pinout of the lowest I/O count device is compatible with the rest of the range. A design can simply be implemented in the device with the lowest I/O count and restricted to the same pinout if migrated to a device with more I/O.

Table 7-2: I/O Count for Compatibility Across Density Ranges in LX the Family

Package	I/O Count	LX4	LX9	LX16	LX25	LX45	LX75	LX100	LX150	
TQG144	Total I/O	102	102							
	Compatible I/O	102								
CPG196	Total I/O	106	106	106						
	Compatible I/O	106								
CSG225	Total I/O	132	160	160						
	Compatible I/O	132								
		160								
FT(G)256	Total I/O		186	186	186					
	Compatible I/O		186							
CSG324	Total I/O		200	232	226	218				
	Compatible I/O	200								
		226								
		218								
CS(G)484	Total I/O					320	328	338	338	
	Compatible I/O	310 ⁽¹⁾								
						328		338		
FG(G)484	Total I/O				266	316	280	326	338	
	Compatible I/O	254 ⁽¹⁾								
		226 ⁽¹⁾								
		270 ⁽¹⁾								
						280		326		
FG(G)676	Total I/O					358	408	480	498	
	Compatible I/O	324 ⁽¹⁾								
						408		480		
FG(G)900	Total I/O								576	

Notes:

1. The compatible number of I/O is less than the number of I/O in the device with the lowest I/O count because NCs do not completely align with each other.

Table 7-3: I/O Count for Compatibility Across Density Ranges in the LXT Family

Package	I/O Count	LX25T ⁽¹⁾	LX45T	LX75T	LX100T	LX150T	
CSG324	Total I/O	190	190				
	Compatible I/O	190					
CS(G)484	Total I/O		296	292	296	296	
	Compatible I/O	292					
						296	
FG(G)484	Total I/O	250	296	268	296	296	
	Compatible I/O	250					
		226 ⁽²⁾					
				268			
FG(G)676	Total I/O			348	376	396	
	Compatible I/O				348		
						376	
FG(G)900	Total I/O				498	540	
	Compatible I/O					498	

Notes:

1. The LX25T devices have NCs in place of one GTPA1_DUAL available in the larger devices.
2. The compatible number of I/O is less than the number of I/O in the device with the lowest I/O count because the NCs do not completely align with each other.

Special Cases

MCBs and Parallel Configuration in the LX4

The LX4 device does not support Memory Controller Blocks (MCBs) or parallel configuration modes. The same is true of all devices in the TQG144 and CPG196 packages, but in the CSG225 package the larger devices support these functions. Therefore, the names of several I/O on the LX4 are different than the LX9 and LX16 in the CSG225 because the dual function name is not included in the pin name. For example, pin B14 is IO_L1P_A25_1 in the LX9 and LX16 but IO_L1P_1 in the LX4. This name change does not affect its compatibility as an I/O pin.

GTP Transceiver Connections in the LX25T

The LX25T device, available in the CSG324 and FG(G)484 packages, has two GTP transceiver ports. The other LXT devices in these packages have four GTP transceiver ports. The two additional ports are left as No Connects in the LX25T in the CSG324 and FG(G)484 packages. Therefore, the LX25T has more NCs than is implied by the I/O count. For example, although the LX25T and LX45T have the same I/O count in the CSG324 package, the LX25T has 17 NCs while the LX45T has none.

Encryption Pins

The LX75, LX100, LX150, LX75T, LX100T, and LX150T include three pins used for the bitstream encryption function— V_{FS} , R_{FUSE} , and V_{BATT} . This function is not available in the smaller devices. To maintain compatibility with the larger devices, these pins are left as NCs in the smaller devices. For example, in packages that support both the LX45 or LX45T and the LX75 or LX75T, the LX45 and LX45T will have three NCs in addition to any NCs in place of I/O pins. In the larger devices, these encryption pins should be tied High or Low. However, they can be left floating for ease of migration. In the smaller devices, the encryption pins can be treated as standard NCs, however, to allow for migration, avoid routing active signals through these NC pins. If there is a potential to add encryption and migrate the design to a larger device, connect the pins in the smaller devices as they would be used for encryption.

MCBs and I/O Banks in the FG(G)676 and FG(G)900

The MCB associated I/O pins have a similar relative layout across multiple packages. A board layout for one package can be similar for a different package.

The larger Spartan-6 devices (LX75/T, LX100/T, and LX150/T) have four MCBs in the larger packages, the FG(G)676 and FG(G)900. To support the extra MCBs, the two side banks 1 and 3 are split in half, with a bank 4 added to the top left and a bank 5 added to the top right (Figure 7-1).

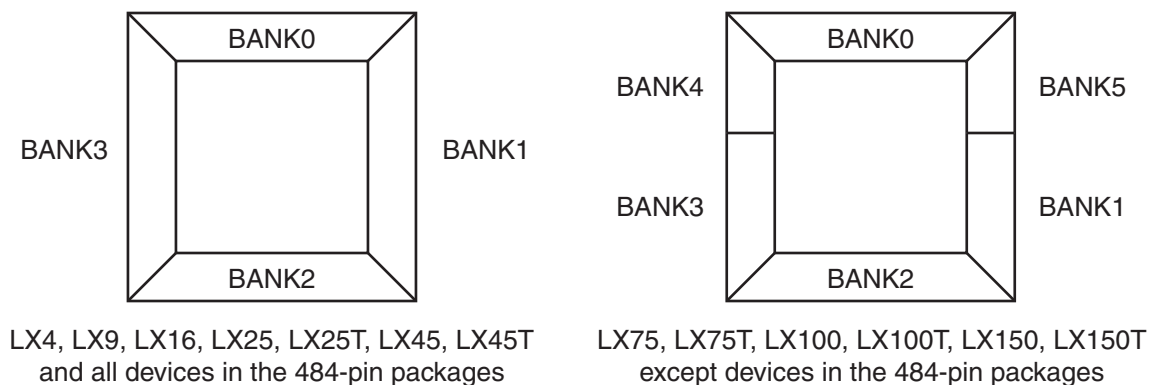


Figure 7-1: Spartan-6 FPGA I/O Bank Migration

In the LX devices, when migrating from the LX45 to the LX75 in the FG(G)676 package, the pinout designations change for some of the pins from bank 3 to bank 4, and for others from bank 1 to bank 5. In addition, many of these pins also add dual-purpose MCB names. For an FG(G)676 design to migrate (in either direction) between the LX45 and the LX75 or larger, restrict MCB use to banks 1 and 3. Treat bank 4 as an extension of bank 3, and treat bank 5 as an extension of bank 1, using the same V_{CC0} and optional V_{REF} voltages. Calculate SSO requirements independently for the 4-bank and 6-bank implementations. Also follow all I/O design rules for both implementations, including the restriction of two differential I/O standards per bank.

When the LX75 and LX75T and larger devices are packaged in the 484-pin packages, only four banks are provided in the pinout. The device designs in this package should be for a 4-bank device, not a 6-bank device. Limiting to four banks allows migration between the LX45 and LX45T or smaller devices and the LX75 and LX75T and larger devices in the 484-pin packages.

GTP Transceiver Banks

The GTP transceivers have a similar relative layout of their associated I/O and power pins across multiple packages. An effective board layout for one package can be used for a different package.

The MGTREFCLK pins in the FG(G)484 package have the P side toward the outside of the package, while in all other packages and all other I/O the N side is toward the outside of the package.

LX25 and LX25T Migration

The pinouts for the LX25 and LX25T are compatible with the other Spartan-6 devices in the same packages. However, there are two unique characteristics to consider when migrating from the LX25 to other Spartan-6 LX devices or when migrating from the LX25T to other Spartan-6 LXT devices.

- The LX25 and LX25T do not support BPI configuration. For more details, see [UG380](#), *Spartan-6 FPGA Configuration User Guide*.
- 12 pins in bank 1 and bank 3 of the LX25 and LX25T are associated with different BUFIO2 clocking regions for the other devices in the same package. This difference affects package migration when using the FT(G)256, CSG324, and FG(G)484 packages. For more information, see the notes in [Table 2-6](#) through [Table 2-10](#), and refer to the *Clock Inputs* section in [UG382](#), *Spartan-6 FPGA Clocking Resources User Guide*.

Pin Names and Physical Pad Locations

In general, the same pin name will have the same location on the device across different packages. For example, the HSWAPEN pin is always in the top-left corner of the device and the I/O name is consistently IO_L1P_0. Pins with dual-purpose names, such as the MCB and configuration pins, always refer to the same specific pad location on the device. As a design migrates between densities in a package, these pins will connect to the same general area of the device, allowing the pinout to be maintained. However, some pins may connect to a different area of the device, either because of the different size of the FPGA array or because of different pad-to-package connections. When possible, when migrating between densities, allow the software to change the pin locations to optimize for the new target device.

Migrating Between Packages

Although general layout will be consistent between packages, there is no direct compatibility, even between the CS(G)484 and FG(G)484, to facilitate migration between packages. Pin names are generally maintained across packages, so a function locked to a particular pin name in one package should use the same I/O pad when migrated to a different package. However, some associations between pin names and physical pad locations can change. Either create new constraints for the new package, or use the software tools to verify that the same pad is being used.

PlanAhead Software Tool

The PinAhead environment with the PlanAhead™ tool provides an interface to analyze the design and device I/O requirements and to define an I/O pinout configuration that satisfies the needs of both the PCB and FPGA designers. The PlanAhead software enables the creation of I/O port signals and can import an I/O port list in CSV, UCF, or HDL format. Using this tool allows for early and intelligent pinout definition and can eliminate some of the unnecessary pinout related changes that typically happen later in the design.

The graphical tools make it easier to analyze possible pinouts across different options. The PinAhead environment consists of a split workspace showing both the package and device views. There are other views that provide additional I/O information: the clock region view, package pins view, and the I/O ports view. The package pins view table is categorized by I/O banks allowing easy cross selection and highlighting of I/O banks in both the device and package views. This clearly shows the relationship of the physical pin location and the I/O pad location on the device, which simplifies optimal I/O bank selection. Pin information for each pin in the I/O bank is displayed in the package pins view. For more information on the PlanAhead tool, see <http://www.xilinx.com/tools/planahead.htm>.

