CY7C4221 / CY7C4231

1 K / 2 K × 9 Synchronous FIFOs

Features

- High-speed, low-power, first-in first-out (FIFO) memories
  - 1 K × 9 (CY7C4221)
  - 2 K × 9 (CY7C4231)
- High-speed 66.7 MHz operation (15 ns read/write cycle time)
- Low power (I_{CC} = 35 mA)
- Fully asynchronous and simultaneous read and write operation
- Empty, Full, and Programmable Almost Empty and Almost Full status flags
- TTL-compatible
- Output Enable ($\overline{OE}$) pin to three-state the output bus
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- Width-expansion capability
- Space saving 7 mm × 7 mm 32-pin TQFP and 32-pin PLCC packages available
- Pin-compatible and functionally equivalent to IDT72221 & 72231
- Pb-free packages available

Functional Description

The CY7C42X1 are high-speed, low-power FIFO memories with clocked read and write interfaces. All are nine bits wide. The CY7C42X1 are pin-compatible to IDT722X1. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read-enable pins (REN1, REN2). In addition, the CY7C42X1 has an output enable pin ($\overline{OE}$). The Read (RCLK) and Write (WCLK) clocks can be tied together for single-clock operation or the two clocks can run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.The CY7C42X1 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty – 7 and Full – 7.

The flags are synchronous, they change state relative to either the Read clock (RCLK) or the Write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

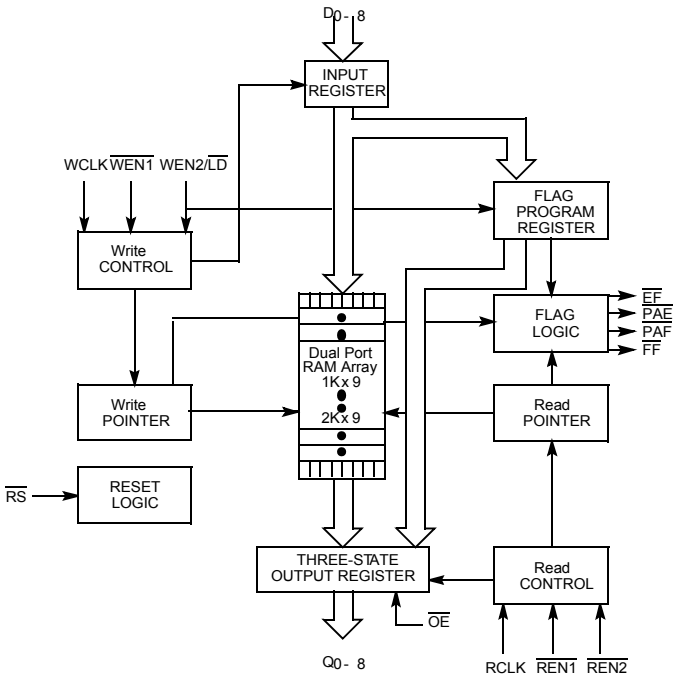
All configurations are fabricated using advanced 0.65 μ N-Well CMOS technology. Input ESD protection is greater than 2001 V, and latch up is prevented by the use of guard rings.

Selection Guide

Description		-15	Unit
Maximum frequency		66.7	MHz
Maximum access time		10	ns
Minimum cycle time		15	ns
Minimum data or enable setup		4	ns
Minimum data or enable hold		1	ns
Maximum flag delay		10	ns
Active power supply current	Commercial	35	ICC1
	Industrial	40	

	CY7C4221	CY7C4231
Density	1 K × 9	2 K × 9

Logic Block Diagram



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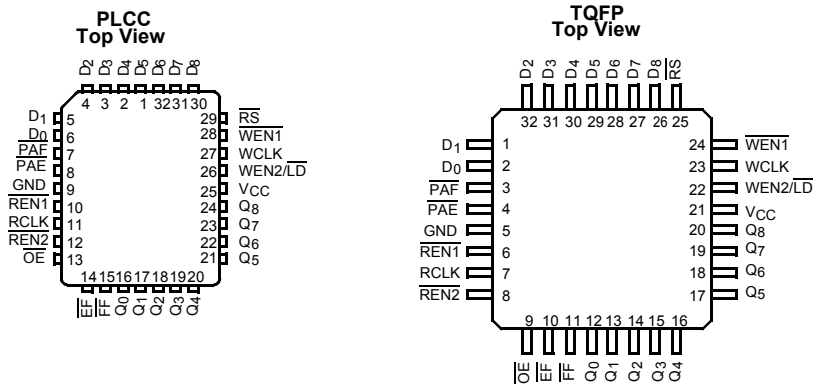
Pin Configuration

Figure 1. Pin Diagram



Pin Definitions

Pin	Name	I/O	Description
$D_{0–8}$	Data Inputs	I	Data inputs for 9-bit bus.
$Q_{0–8}$	Data Outputs	O	Data outputs for 9-bit bus.
WEN1	Write Enable 1	I	The only write enable to have programmable flags when device is configured. Data is written on a LOW-to-HIGH transition of WCLK when WEN1 is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when WEN1 is LOW and WEN2/LD and FF are HIGH.
WEN2/LD Dual Mode Pin	Write Enable 2	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data is not written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
	Load	I	
REN1, REN2	Read Enable Inputs	I	Enables device for read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when WEN1 is LOW, WEN2/LD is HIGH, and the FIFO is not Full. When LD is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when REN1 and REN2 are LOW and the FIFO is not Empty. When WEN2/LD is LOW, RCLK reads data out of the programmable flag-offset register.
EF	Empty Flag	O	When EF is LOW, the FIFO is empty. EF is synchronized to RCLK.
FF	Full Flag	O	When FF is LOW, the FIFO is full. FF is synchronized to WCLK.
PAE	Programmable Almost Empty	O	When PAE is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
PAF	Programmable Almost Full	O	When PAF is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
RS	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power up.
OE	Output Enable	I	When OE is LOW, the FIFO's data outputs drive the bus to which they are connected. If OE is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

Architecture

The CY7C42X1 consists of an array of 1K or 2K words of nine bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN1, REN2, WEN1, WEN2, RS), and flags (EF, PAE, PAF, FF).

Resetting the FIFO

During powerup, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs ($Q_{0–8}$) go LOW t_{RSF} after the rising edge of $\overline{RS}$. For the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while RS is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the $D_{0–8}$ pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW, data in the FIFO memory is presented on the $Q_{0–8}$ outputs. New data is presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the $Q_{0–8}$ outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register is available to the $Q_{0–8}$ outputs after t_{OE}.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its $Q_{0–8}$ outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$). If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$). This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2 / Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

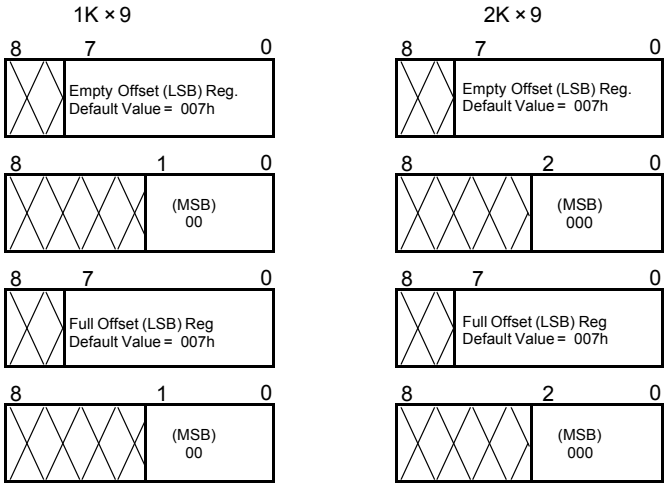
When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. Figure 2 on page 6 shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK Read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

Figure 2. Offset Register Location and Default Values



Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in Table 1 or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n + 1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAF}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4221 (1K – m) or CY7C4231 (2K – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 1. Writing the Offset Registers

LD	WEN	WCLK [1]	Selection
0	0	↑	Empty offset (LSB) Empty offset (MSB) Full offset (LSB) Full offset (MSB)
0	1	↑	No operation
1	0	↑	Write into FIFO
1	1	↑	No operation

Table 2. Status Flags

Number of Words in FIFO		$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
CY7C4221	CY7C4231				
0	0	H	H	L	L
1 to n[2]	1 to n[2]	H	H	L	H
(n + 1) to 512	(n + 1) to 1024	H	H	H	H
513 to (1024 – (m + 1))	1025 to (2048 – (m + 1))	H	H	H	H
(1024 – m)[3] to 1023	(2048 – m)[3] to 2047	H	L	H	H
1024	2048	L	L	H	H

Notes
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n = 7 default value).
3. m = Full Offset (m = 7 default value).

Width Expansion Configuration

Word width may be increased by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. Figure 3 demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See Figure 3). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C42X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

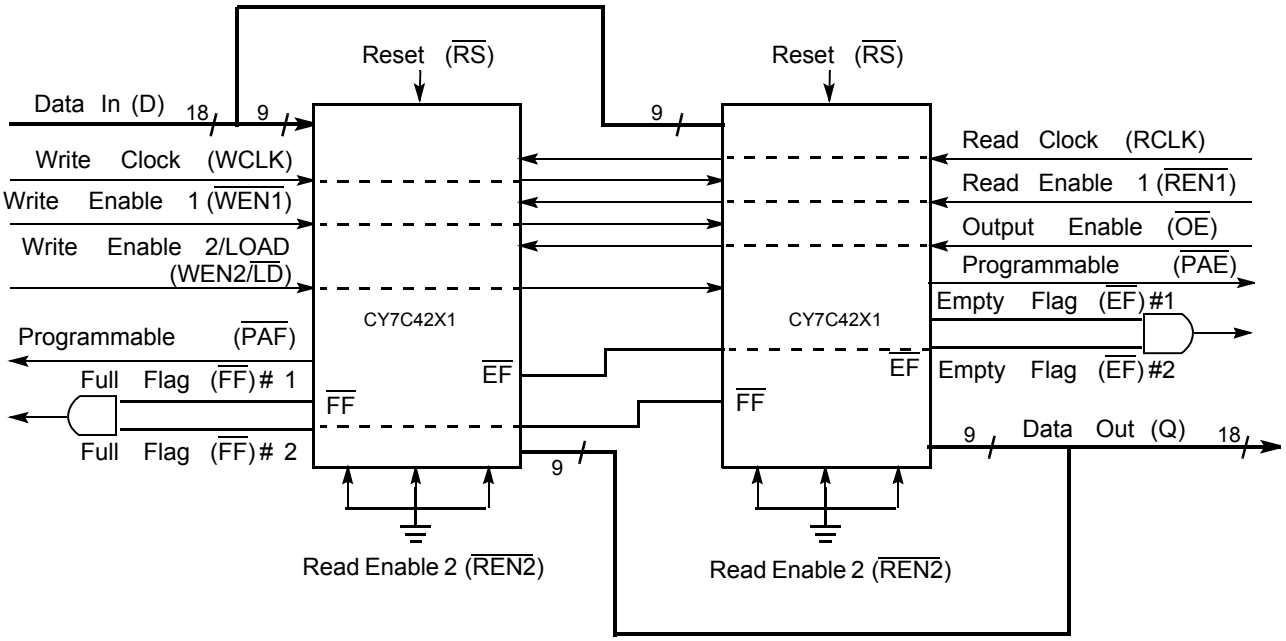
Full Flag

The Full Flag ($\overline{FF}$) goes LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of WEN1 and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK - it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) goes LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK - it is exclusively updated by each rising edge of RCLK.

Figure 3. Block Diagram of 1024 × 9, 2048 × 9 Synchronous FIFO Memory Used in a Width Expansion Configuration



Maximum Ratings

Exceeding maximum ratings[4] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.5 V to +7.0 V

DC voltage applied to outputs in High Z state ..... –0.5 V to +7.0 V

DC input voltage ..... –3.0 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial [5]	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-15		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –2.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage			2.2	V_{CC}	V
V_{IL}	Input LOW voltage			–3.0	0.8	V
I_{IX}	Input leakage current	V_{CC} = Max		–10	+10	µA
I_{OS}[6]	Output short circuit current	V_{CC} = Max, V_{OUT} = GND		–90	–	mA
I_{OZL}	Output OFF, High Z current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	mA
I_{OZH}						
I_{CC1}[7]	Active power supply current		Commercial	–	35	mA
			Industrial	–	40	mA
I_{CC2}[8]	Average standby current		Commercial	–	10	mA
			Industrial	–	15	mA

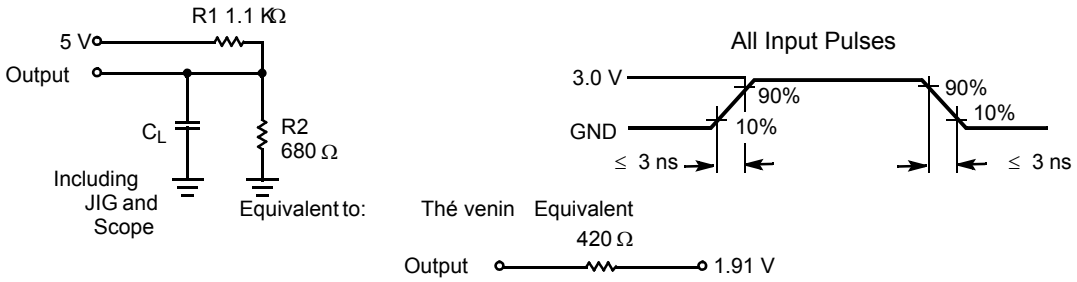
Capacitance

Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output capacitance		7	pF

Notes
4. The voltage on any input or I/O pin cannot exceed the power pin during powerup.
5. T_A is the “instant on” case temperature.
6. Test no more than one output at a time for not more than one second.
7. Outputs open. Tested at frequency = 20 MHz.
8. All inputs = V_{CC} – 0.2 V, except WCLK and RCLK, which are switching at 20 MHz.
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [10, 11]



Switching Characteristics

Over the Operating Range

Parameter	Description	-15		Unit
		Min	Max	
t_S	Clock Cycle Frequency	–	66.7	MHz
t_A	Data Access Time	2	10	ns
t_{CLK}	Clock Cycle Time	15	–	ns
t_{CLKH}	Clock HIGH Time	6	–	ns
t_{CLKL}	Clock LOW Time	6	–	ns
t_{DS}	Data Setup Time	4	–	ns
t_{DH}	Data Hold Time	1	–	ns
t_{ENS}	Enable Setup Time	4	–	ns
t_{ENH}	Enable Hold Time	1	–	ns
t_{RS}	Reset Pulse Width [12]	15	–	ns
t_{RSS}	Reset Setup Time	10	–	ns
t_{RSR}	Reset Recovery Time	10	–	ns
t_{RSF}	Reset to Flag and Output Time	–	15	ns
t_{OLZ}	Output Enable to Output in Low Z [13]	0	–	ns
t_{OE}	Output Enable to Output Valid	3	8	ns
t_{OHZ}	Output Enable to Output in High Z [13]	3	8	ns
t_{WFF}	Write Clock to Full Flag	–	10	ns
t_{REF}	Read Clock to Empty Flag	–	10	ns
t_{PAF}	Clock to Programmable Almost-Full Flag	–	10	ns
t_{PAE}	Clock to Programmable Almost-Full Flag	–	10	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	6	–	ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	15	–	ns

Notes
10. C_L = 30 pF for all AC parameters except for t_{OHZ}.
11. C_L = 5 pF for t_{OHZ}.
12. Pulse widths less than minimum values are not allowed.
13. Values guaranteed by design, not currently tested.

Switching Waveforms

Figure 5. Write Cycle Timing

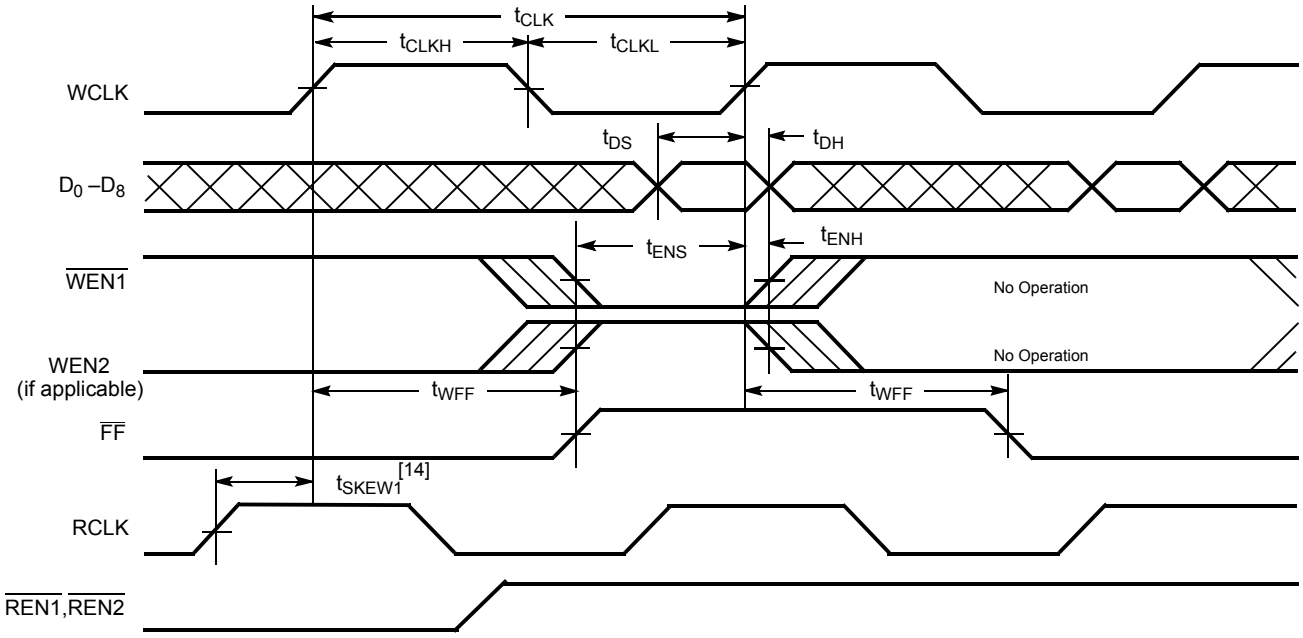
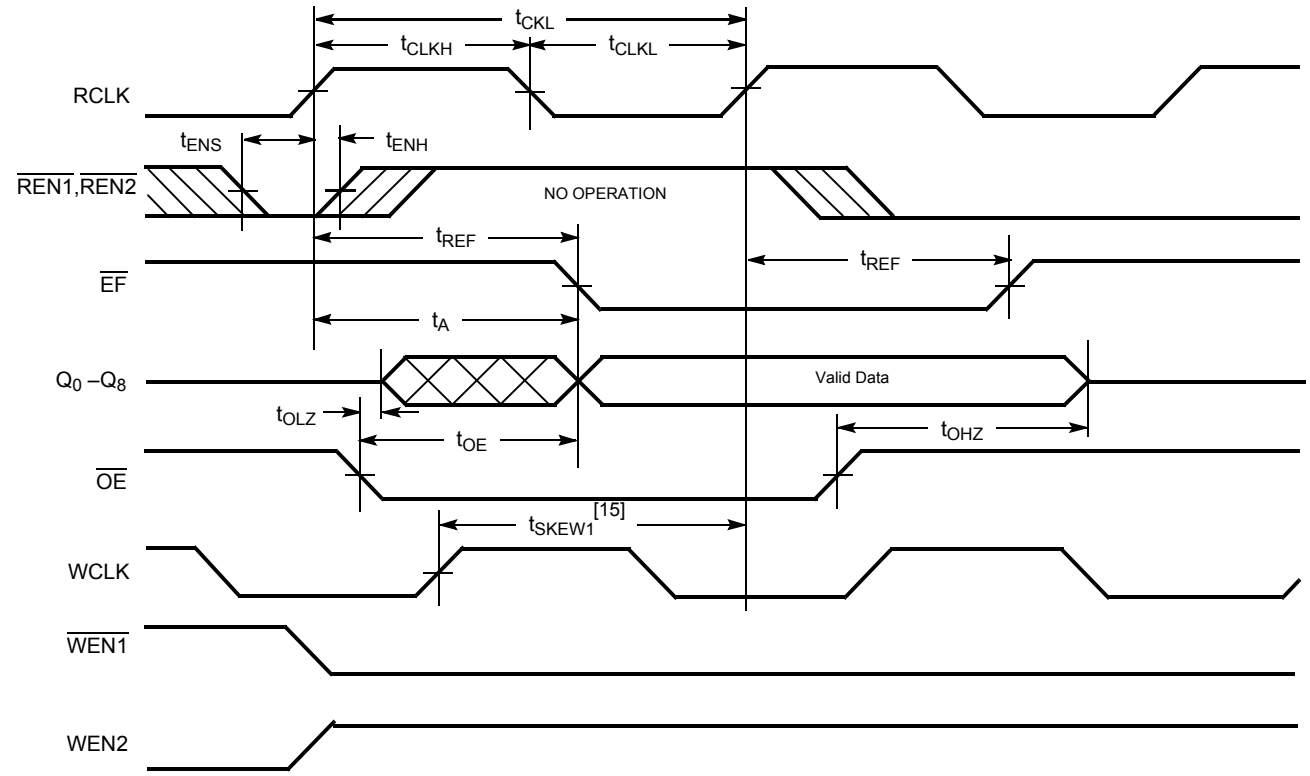


Figure 6. Read Cycle Timing



Notes

14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK rising edge.
15. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ goes HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then EF may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Figure 7. Reset Timing [16]

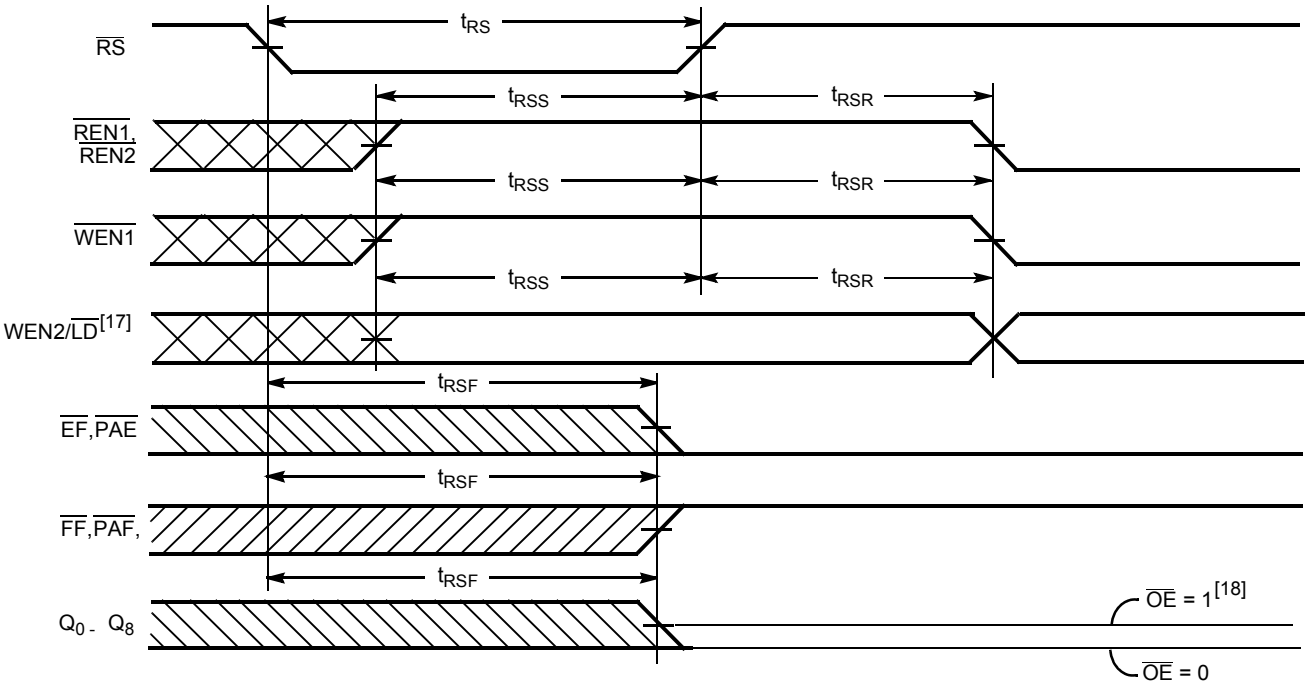
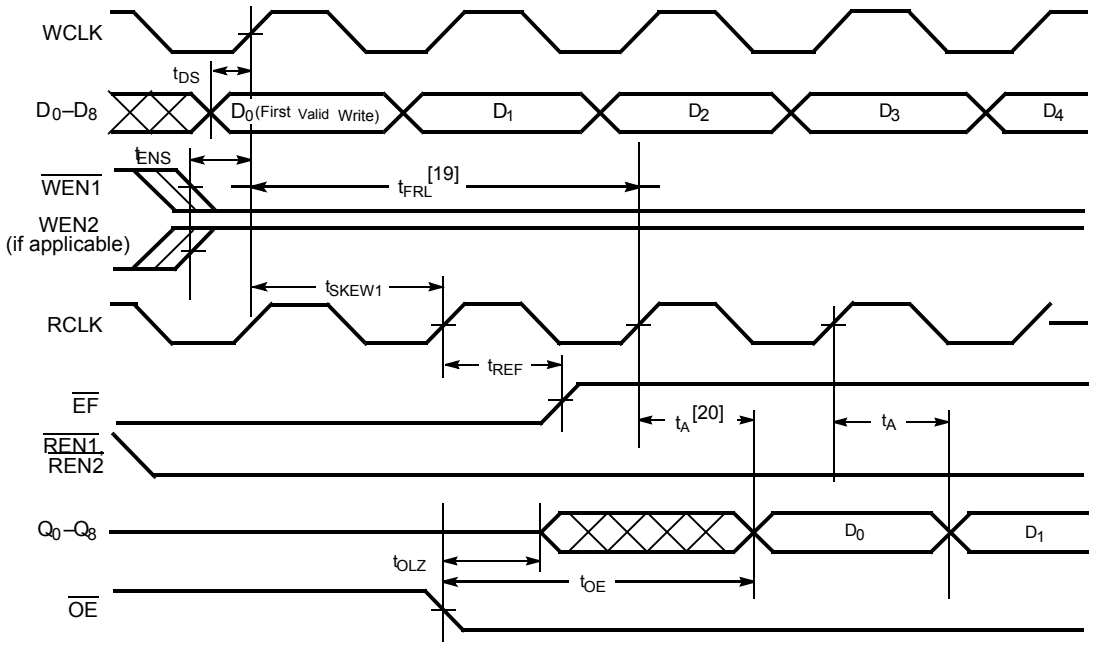


Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

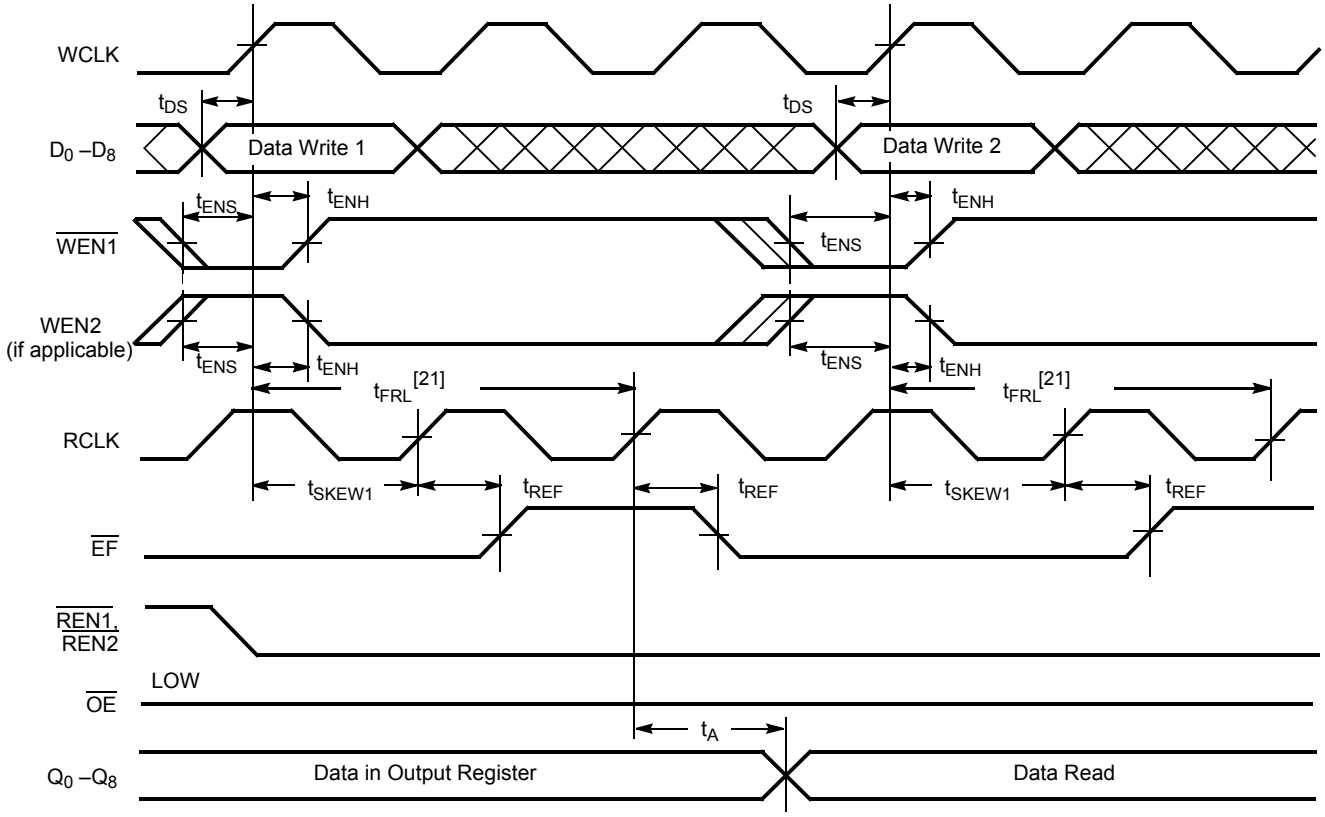


Notes

16. The clocks (RCLK, WCLK) can be free-running during reset.
17. Holding WEN2/LD HIGH during reset makes the pin act as a second enable pin. Holding WEN2/LD LOW during reset makes the pin act as a load enable for the programmable flag offset registers.
18. After reset, the outputs are LOW if OE = 0 and three-state if OE = 1.
19. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(maximum)} = t_{CLK} + t_{SKEW1}$. When t_{SKEW1} < minimum specification, $t_{FRL(maximum)}$ = either $2 \times t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary (EF = LOW).
20. The first word is available the cycle after EF goes HIGH, always.

Switching Waveforms (continued)

Figure 9. Empty Flag Timing

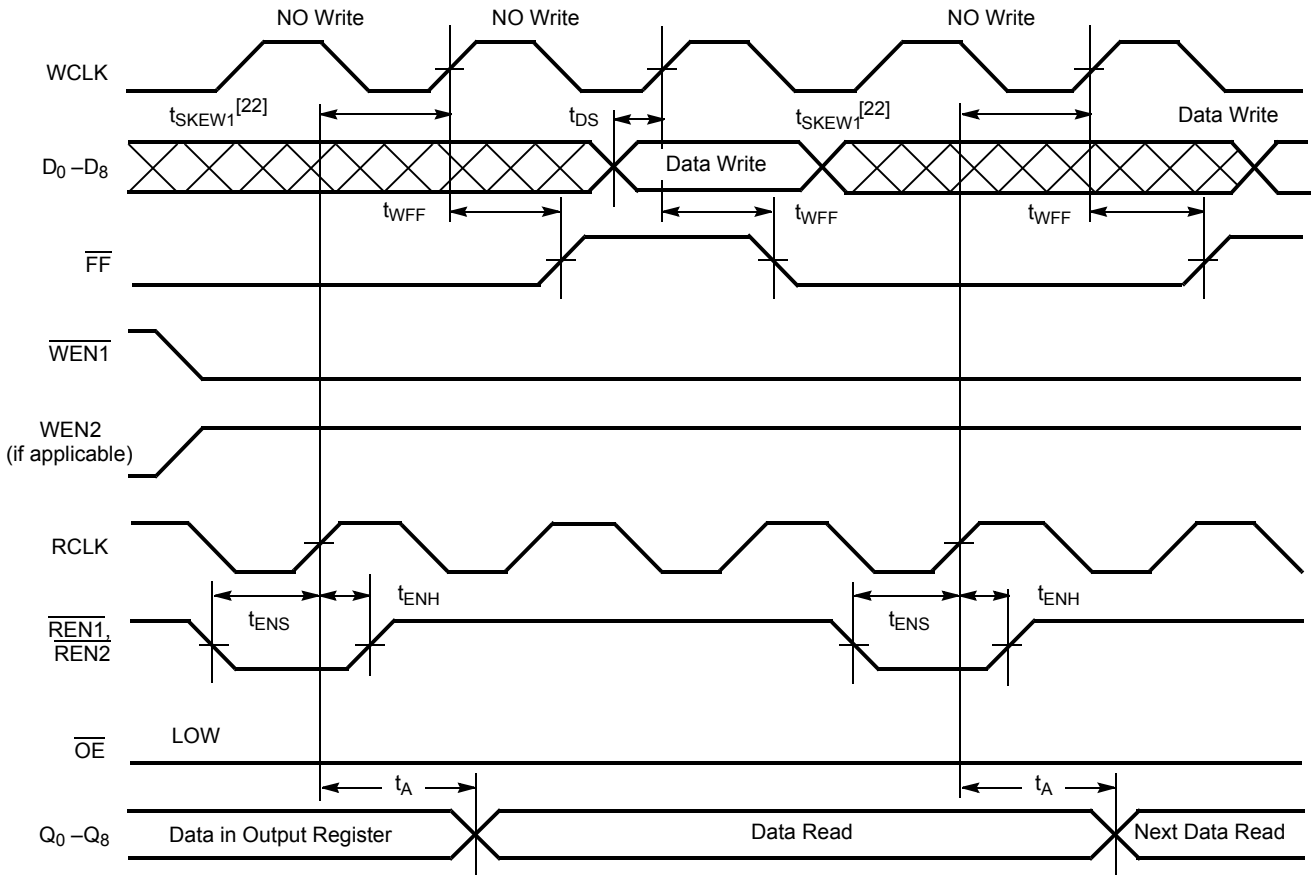


Note

21. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(maximum)} = t_{CLK} + t_{SKEW1}$. When t_{SKEW1} < minimum specification, $t_{FRL(maximum)}$ = either 2 × $t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary (EF = LOW).

Switching Waveforms (continued)

Figure 10. Full Flag Timing



Note

22. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

Figure 11. Programmable Almost Empty Flag Timing

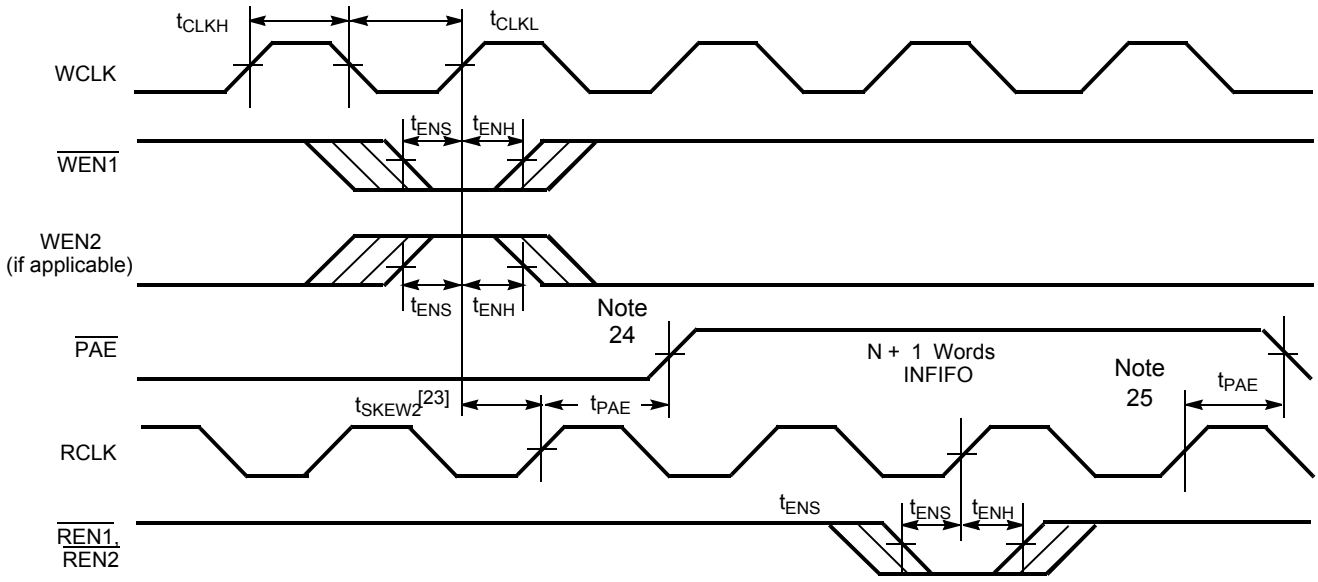
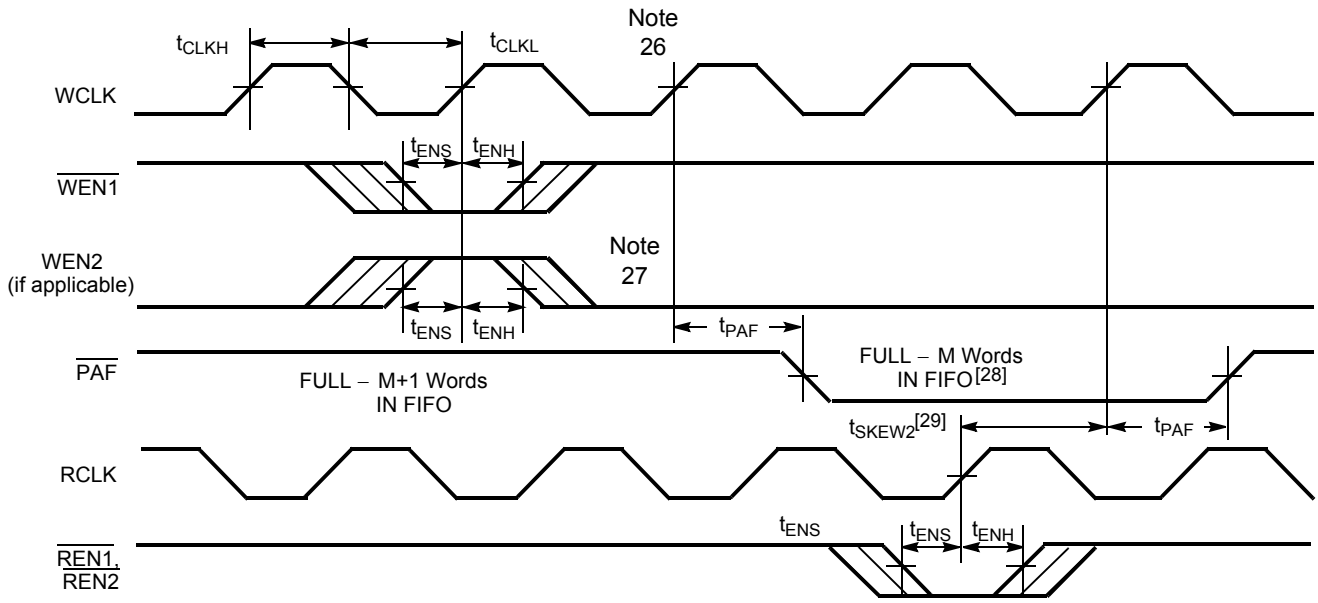


Figure 12. Programmable Almost Full Flag Timing



Notes

23. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
24. PAE offset = n.
25. If a read is performed on this rising edge of the read clock, there are Empty + (n – 1) words in the FIFO when $\overline{PAE}$ goes LOW.
26. If a write is performed on this rising edge of the write clock, there are Full – (m – 1) words of the FIFO when $\overline{PAF}$ goes LOW.
27. PAF offset = m.
28. 1024 – m words for CY7C4221, 2048 – m words for CY7C4231.
29. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

Figure 13. Write Programmable Registers

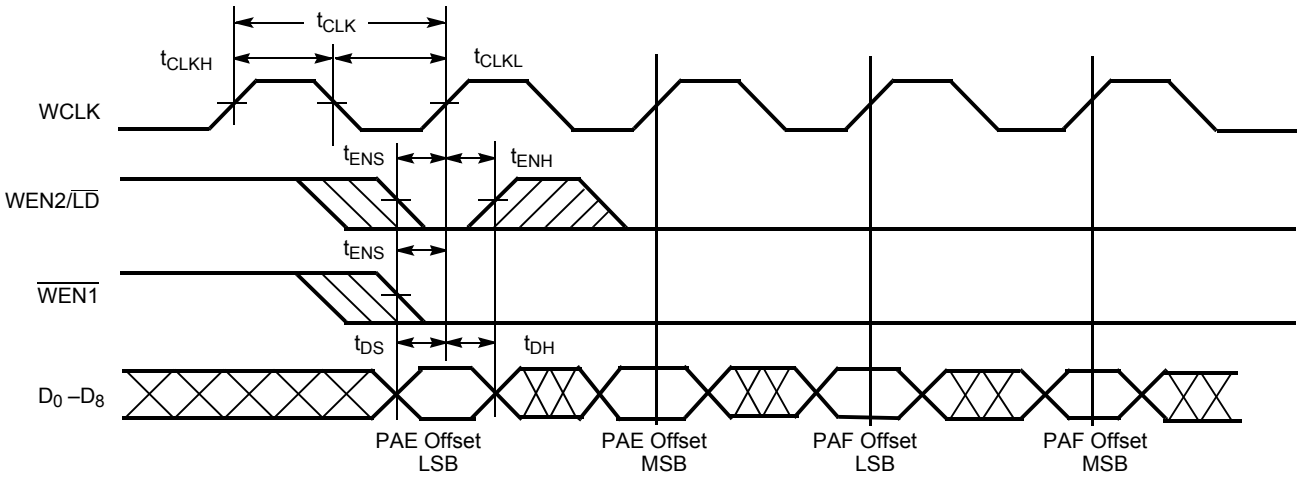
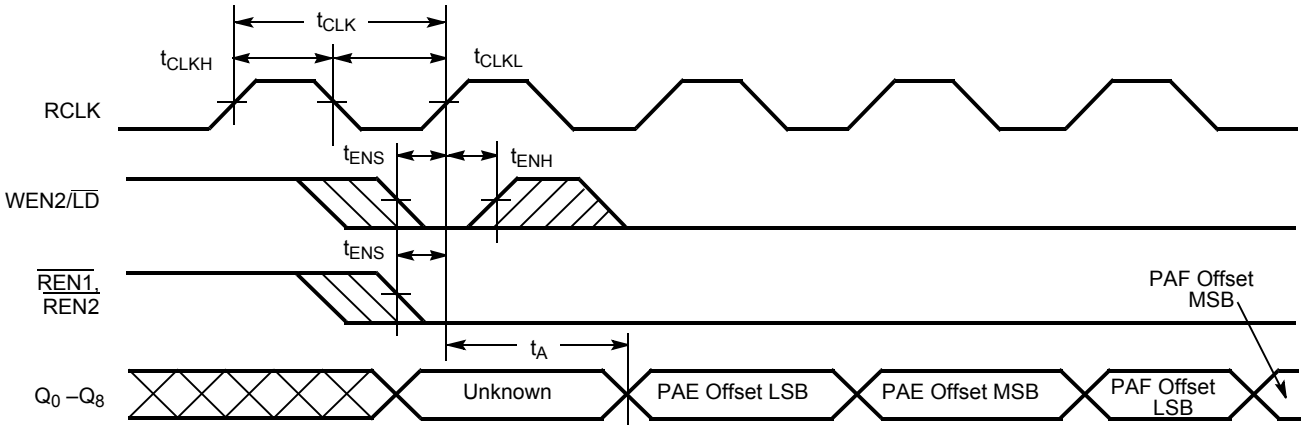
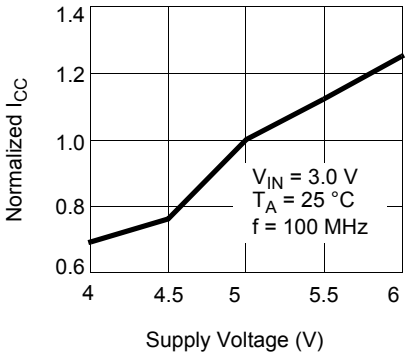


Figure 14. Read Programmable Registers

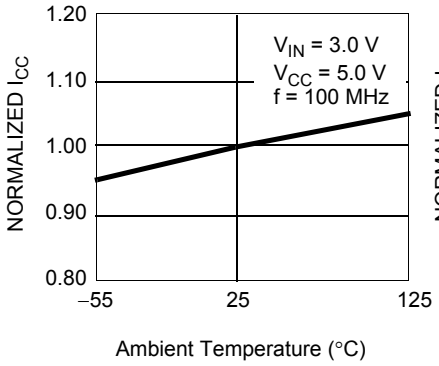


Typical AC and DC Characteristics

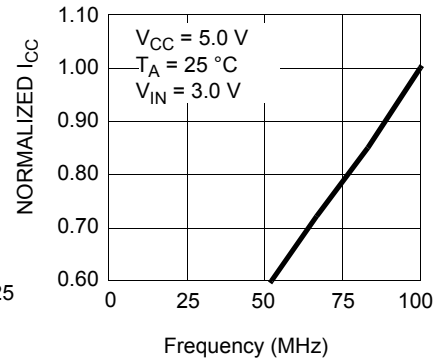
Normalized Supply Current vs. Supply Voltage



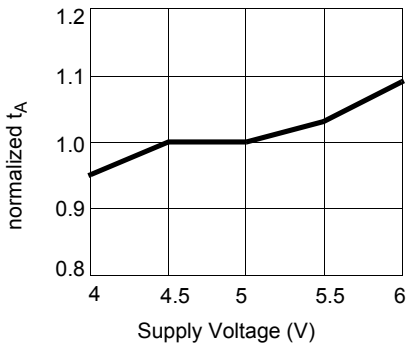
Normalized Supply Current vs. Ambient Temperature



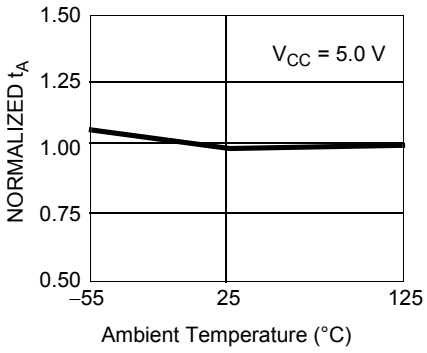
Normalized Supply Current vs. Frequency



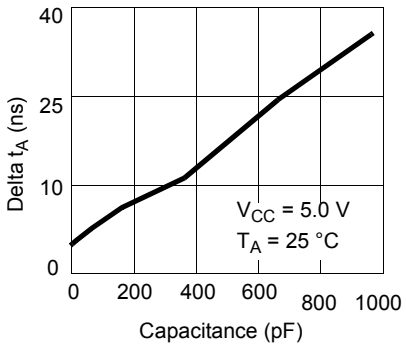
Normalized t_A vs. Supply Voltage



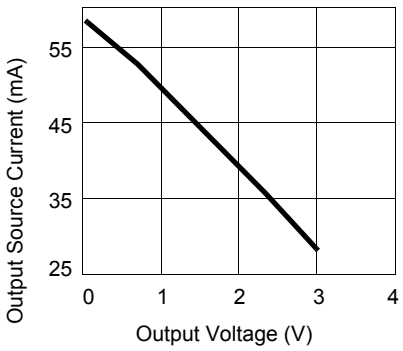
Normalized t_A vs. Ambient Temperature



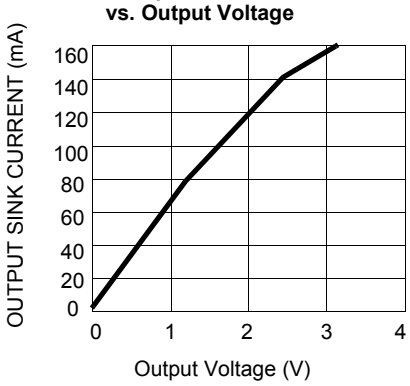
Typical t_A Change vs. Output Loading



Output Source Current vs. Output Voltage



Output Sink Current vs. Output Voltage



Ordering Information

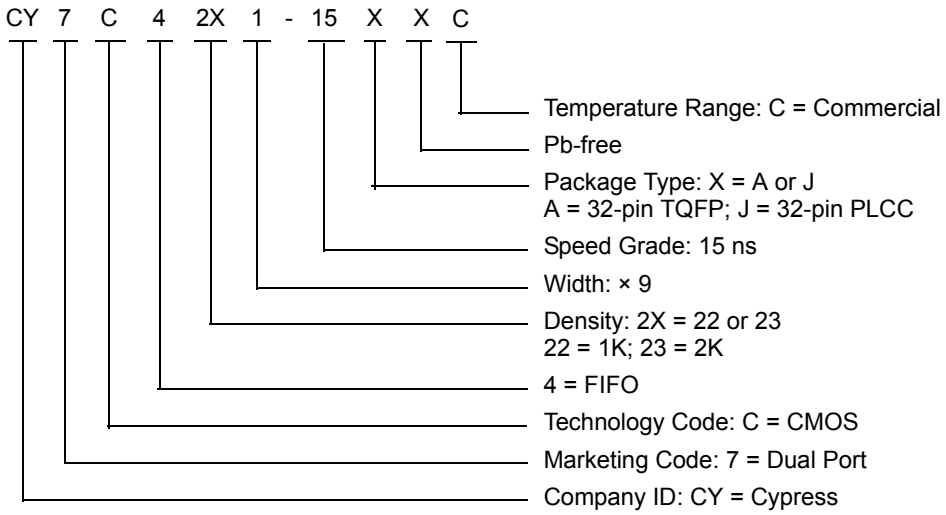
1 K × 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4221-15AXC	51-85063	32-pin Thin Quad Flat Pack (7 × 7 × 1.0 mm) Pb-free	Commercial
	CY7C4221-15JXC	51-85002	32-pin Plastic Leaded Chip Carrier (0.453 × 0.553 inches) Pb-free	

2 K × 9 Synchronous FIFO

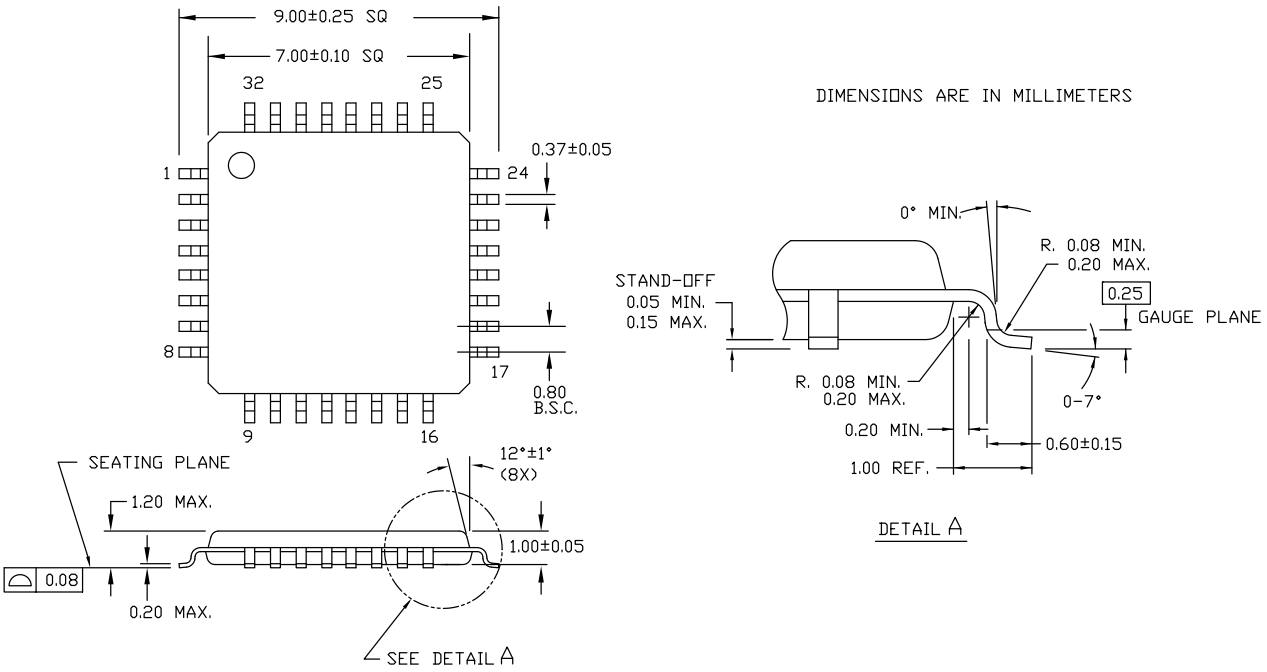
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4231-15AXC	51-85063	32-pin Thin Quad Flat Pack (7 × 7 × 1.0 mm) Pb-free	Commercial
	CY7C4231-15JXC	51-85002	32-pin Plastic Leaded Chip Carrier (0.453 × 0.553 inches) Pb-free	

Ordering Code Definitions



Package Diagrams

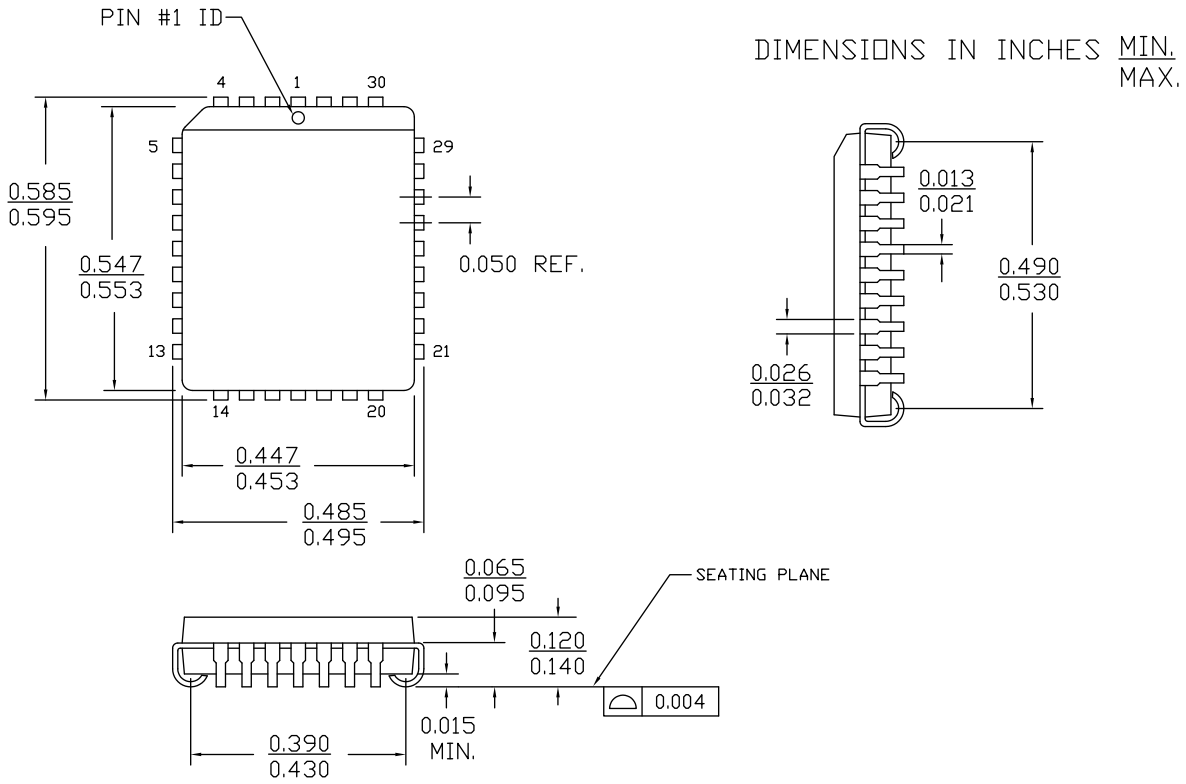
Figure 15. 32-pin TQFP (7 × 7 × 1.0 mm) A3210, 51-85063



51-85063 *D

Package Diagrams (continued)

Figure 16. 32-pin PLCC (0.453 × 0.553 Inches) J32, 51-85002



51-85002 *D

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{EF}$	empty flag
ESD	electrostatic discharge
$\overline{FF}$	full flag
FIFO	first-in first-out
LSB	least significant bit
MSB	most significant bit
$\overline{OE}$	output enable
PLCC	plastic leaded chip carrier
RCLK	read clock
$\overline{RS}$	reset
TQFP	thin quad flat pack
TTL	transistor-transistor logic
WCLK	write clock

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watts

Document History Page

Document Title: CY7C4221 / CY7C4231, 1 K / 2 K × 9 Synchronous FIFOs Document Number: 38-06016				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	106477	09/10/01	SZV	Change from Spec number: 38-00419 to 38-06016
*A	110725	03/20/02	FSG	Change Input Leakage current I_{IX} unit from mA to μA (typo)
*B	122268	12/26/02	RBI	Power up requirements added to Maximum Ratings Information
*C	386306	See ECN	ESH	Added Pb-free logo to top of front page Added CY7C4421-10JXC, CY7C4201-15AXC. CY7C4201-15JXC, CY7C4211-10AXI, CY7C4211-15AXC, CY7C4211-15JXC, CY7C4221-15AXC, CY7C4221-15JXC, CY7C4231-15JXC, CY7C4231-15AXC, CY7C4241-10AXC, CY7C4241-15AXC, CY7C4241-15JXC, CY7C4251-10JXC, CY7C4251-10AXI, CY7C4251-15AXC, CY7C4251-15JXC
*D	2863896	01/22/10	VKN / PYRS	Removed inactive/pruned parts from the Ordering Information table Added Table of Contents Updated TQFP package diagram
*E	2896378	03/19/2010	RAME	Removed inactive parts from Ordering information and updated package diagram.
*F	3091024	12/22/10	ADMU	Modified PAE and PAF flags information Added Ordering Code Definition, Acronym, and Document Conventions.
*G	3372970	09/15/2011	ADMU	Updated title to read “CY7C4221 / CY7C4231, 1 K / 2 K × 9 Synchronous FIFOs”. Updated Features (Removed CY7C4421, CY7C4201, CY7C4211, CY7C4241, CY7C4251 information). Updated Selection Guide (Removed CY7C4421, CY7C4201, CY7C4211, CY7C4241, CY7C4251 information). Updated Figure 2 and Table 2 in Programming (Removed CY7C4421, CY7C4201, CY7C4211, CY7C4241, CY7C4251 information). Updated Figure 3 in Width Expansion Configuration (Removed CY7C4421, CY7C4201, CY7C4211, CY7C4241, CY7C4251 information). Updated Electrical Characteristics (Removed -10 and -25 speed bin information). Updated Switching Characteristics (Removed -10 and -25 speed bin information). Updated Typical AC and DC Characteristics. Updated Package Diagrams. Updated in new template.

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