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Advantages of the Virtex-5 FPGA 6-Input LUT Architecture

By: Andrew Percey

The innovative Virtex™-5 architecture, which is based on a real 6-input LUT with dual-LUT capability, provides substantial resource utilization advantages over competing architectures. This white paper details those advantages, focusing on comparisons between the 65 nm high-end FPGA offerings of Xilinx (Virtex-5 FPGAs) and Altera (Stratix III FPGAs).

Introduction to the Architectures

Figure 1 shows the fundamental architecture of the Xilinx Virtex-5 FPGA: the 6-input LUT with associated logic. Figure 2 shows the fundamental architecture of the Altera Stratix III FPGA: the Adaptive Logic Module (or ALM).

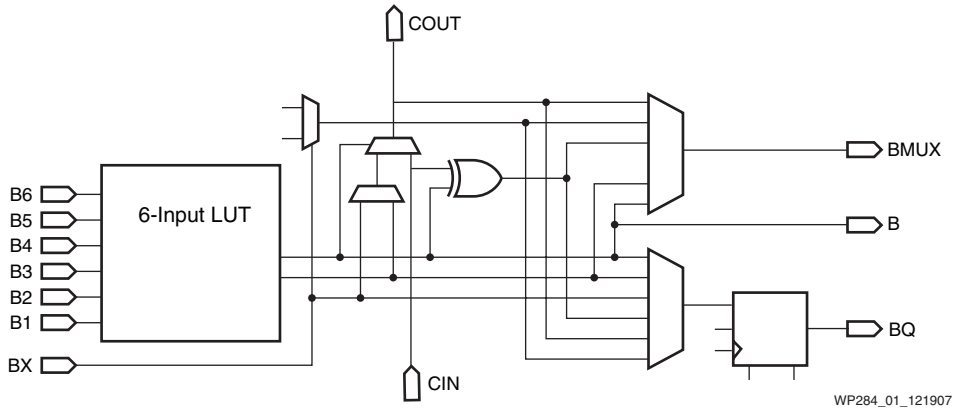

Figure 1: **Virtex-5 FPGA 6-Input LUT Architecture**

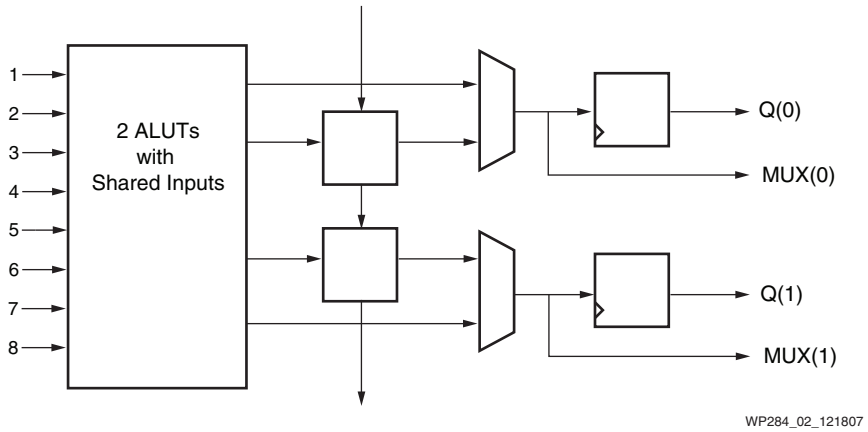

Figure 2: **Stratix III ALM Architecture**

The Xilinx 6-input LUT is a look-up table with a total of 64 bits of logic programming space and 6 independent inputs. It is able to implement any function of 6 inputs and numerous combinations of one or two smaller functions. The 6-input LUT also includes associated carry logic, MUXs, and a flip-flop. In some portions of the logic, the 6-input LUT can additionally be used as 64 bits of RAM or 32 bits of shift register. For more information, see UG190: *Virtex-5 User Guide*.

The Altera ALM includes two Adaptive LUTs (ALUTs) with a total of 64 bits of logic programming space and 8 shared inputs. It is also able to implement any function of 6 inputs and numerous combinations of one or two smaller functions. The ALM also includes associated adders, MUXs, and flip-flops.

Because the 6-input LUT and the ALM are the fundamental logic building blocks of these FPGA architectures and are very similar to each other, they represent the best comparison points.

At the expense of additional silicon area, the ALM provides incremental flexibility beyond the functionality of the 6-input LUT and associated logic. However, because

the ALM is larger and costlier to build, there are fewer ALMs relative to 6-input LUTs in devices with comparable part numbering. The resulting effect on the total logic capacity of specific devices is the metric that matters most (see Table 1).

Every customer design has a unique mixture of functions, ranging from one input to six or more inputs, varying amounts of input signal sharing, and varying requirements for arithmetic logic and flip-flops. And while the Virtex-5 FPGA 6-input LUT and Stratix III ALM architectures have similar logic capacity, the underlying implementations have many differences. Therefore, the most accurate and useful way to compare device utilization (logic capacity) of these two architectures is to perform fair benchmarking with a suite of customer designs.

Creating and Analyzing Fair Benchmarks

Creating a useful and fair FPGA benchmarking suite requires:

- A large number of customer designs that represent various target markets
- Unaltered RTL code, to avoid tweaks that might favor a certain architecture
- Use of the tool sets recommended by each FPGA vendor
- Use of appropriate constraints for each FPGA vendor's tool set

The Xilinx benchmark suite of designs used to generate the results in this white paper meets all of these requirements.

The 97 designs represent the main markets for high-end FPGAs (which includes both Virtex-5 and Stratix III devices). About 40% of the designs are Telecom designs, another 40% are DSP designs, and the rest are composed of industrial, data processing, and processor designs. Most represent FPGA designs currently used in production by customers. A few are ASIC designs.

All the designs in the suite are RTL-based (VHDL and Verilog). Several include Xilinx CORE Generator™ software EDIF netlists to implement FIFOs and memories. The equivalent functions were created for Stratix III using the Quartus II MegaWizard tool. No alterations were made to the RTL code to favor either FPGA architecture.

The utilization benchmarks were based on the latest versions of the Xilinx ISE software and the Altera Quartus II software, using Synplify Pro netlists. The appropriate switches were used for each tool set to minimize design area.

By carefully following this process, the benchmark results achieved in this white paper are both accurate and representative of real customer designs.

Figure 3 shows the device utilization comparison between the 6-input LUT and ALM architectures across the benchmark suite defined above. The *y* axis shows the ratio of 6-input LUTs to ALMs required to implement each design. The *x* axis is the suite of benchmark designs, ordered from the lowest to highest 6-input LUT/ALM ratio.

The results have a range from 0.3 to 3.2, a standard deviation of 0.45, and an average (geometric mean) of 1.2. Across this representative suite of customer designs, using accurate and fair synthesis practices with both the Xilinx and Altera tools to minimize design area, it takes an average of 1.2 6-input LUTs to implement the same logic as a single ALM.

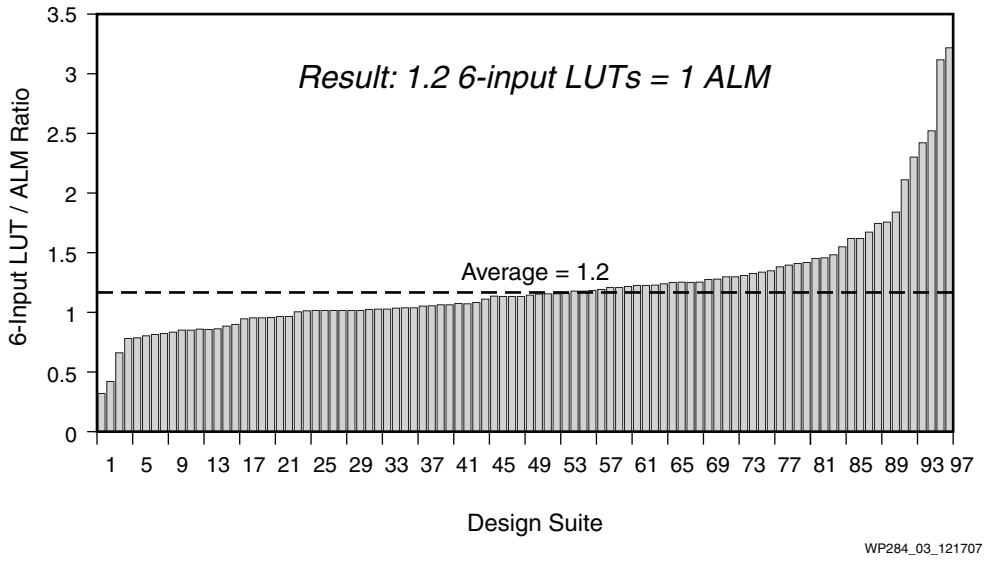

Figure 3: **Utilization Benchmarking Results**

This ratio is not meaningful in isolation. To be meaningful, it needs to be applied to the logic capacity of full FPGA devices. As mentioned before, each ALM consumes more silicon area than a corresponding 6-input LUT and its associated logic. Therefore, there are fewer ALMs than 6-input LUTs in devices of comparable size. In Table 1, the average benchmark value of 1.2 is applied to the list of Altera Stratix III devices, with devices ordered in increasing logic capacity and with comparable Virtex-5 and Stratix III devices aligned.

Table 1: **Logic Capacity Comparison of Virtex-5 and Stratix III FPGAs**

Virtex-5 Device	6-Input LUTs	Stratix III Device	ALMs	Equivalent 6-Input LUTs
XC5VLX20T	12480			
XC5VLX30/XC5VLX30T	19200	3SL50	19000	22800
XC5VLX50/XC5VLX50T	28800	3SL70	27000	32400
XC5VLX85/XC5VLX85T	51840	3SL110	42600	51120
XC5VLX110/XC5VLX110T	69120	3SL150	56800	68160
XC5VLX155/XC5VLX155T	97280	3SL200	79560	95472
XC5VLX220/XC5VLX220T	138240			
		3SL340	135200	162240
XC5VLX330/XC5VLX330T	207360			

This analysis demonstrates that Virtex-5 devices have significantly more logic capacity than Stratix III devices with comparable part numbers.

Of course, any benchmark suite, no matter how fair and representative of customer designs, is only a representation. Individual designs can fall anywhere within the range of results. For this reason, Xilinx highly recommends to all customers who wish to precisely compare device utilization between Virtex-5 and Stratix III devices to run their own designs through each company's respective tool suite using all recommended constraints.

Guidelines for optimizing the Xilinx ISE tool flow for area, speed, power, and run time, are available in WP248: *Retargeting Guidelines for Virtex-5 FPGAs*. Even though the white paper focuses on retargeting designs from Virtex-4 to Virtex-5 FPGAs, the guidelines are equally applicable to new Virtex-5 designs.

Why are Altera's Utilization Benchmarking Results Different?

Altera recently published a white paper titled, "Stratix III FPGAs vs. Xilinx Virtex-5 Devices: Architecture and Performance Comparison" (WP-01007-2.1, October 2007, version 2.1). In their document, Altera reported benchmark results that showed a "Virtex-5 LUT-Flipflop pair" to "Stratix III ALM" utilization ratio of 1.8, which they then used to compare FPGA logic capacity.

The 1.8 result from Altera is not meaningful because their analysis compared ALMs to "LUT-Flipflop" pairs. Architecturally, a LUT-Flipflop pair is the combination of a 6-input LUT and its associated flip-flop. But in the ISE software synthesis report, one LUT-Flipflop pair is counted whenever a 6-input LUT *or* its associated flip-flop is used in a synthesized design.

This analysis does not provide a meaningful method to count Virtex-5 logic utilization for one very important reason: the ISE tools do not artificially combine 6-input LUTs and flip-flops into a minimum number of LUT-Flipflop pairs. In fact, the ISE software tools often distribute these elements to minimize routing congestion and thereby maximize design speed. If only the 6-input LUT or the associated flip-flop is used in a LUT-Flipflop pair, the other element is still available to be used. Therefore, counting a LUT-Flipflop pair as "used" whenever *either* element is used does not provide an accurate picture of either device utilization or remaining device capacity.

In the Xilinx benchmark suite, if LUT-Flipflop pairs are counted (instead of 6-input LUTs), the resulting LUT-Flipflop pair to ALM ratio is 1.84, which is very close to the published Altera number of 1.8. This error of counting LUT-Flipflop pairs explains the disparity between the Xilinx and Altera benchmark results.

The most meaningful statistics for comparing logic utilization are the 6-input LUT count in Virtex-5 FPGAs and the ALM count in Stratix III devices. While the ALM includes flip-flops, each flip-flop necessarily uses an input from its associated ALUT to route its input signal. Therefore, an ALUT becomes wholly or partially unusable when its flip-flop is used in isolation. In contrast, a Virtex-5 FPGA 6-input LUT remains fully usable when its flip-flop is used in isolation because each flip-flop has bypass inputs available. This means that regardless of the flip-flop count in a design, the number of available 6-input LUTs and the number of available ALMs accurately represent the remaining logic capacity of their respective devices. Xilinx also attempted to compare the utilization of 6-input LUTs directly to the utilization of the logic portion of ALMs, but the Quartus II log files do not report this information.

It should also be explained why ALUT usage is not a meaningful metric for device utilization even though Quartus II reports focus on ALUT counts. Although the 6-input LUTs in Virtex-5 FPGAs are independent functional units, Stratix III ALUTs are not. The two ALUTs inside each ALM share inputs, and they must also have other factors in common to be utilized. The result of these dependencies can be seen in the synthesis results. Across the benchmark suite, an average of just 1.3 ALUTs per ALM are used, demonstrating that a large percentage of ALUTs are unusable for any given customer design (remember that these results have been optimized for minimum area). For these reasons, reported ALUT usage can be a misleading metric for determining device utilization.

When the meaningful comparison of 6-input LUTs to ALMs is made, the ratio of 1.2 6-input LUTs per ALM is achieved.

Summary

In Virtex-5 FPGAs, the new 6-input LUT architecture provides substantial resource utilization advantages over competing architectures. This advantage means that smaller Virtex-5 FPGAs can be used rather than competing devices to implement the same design, thus saving board space, power, and cost.

Any customer who needs assistance realizing the results stated should contact their authorized Xilinx field application engineer for implementation techniques specific to their application that leverage the full flexibility of the Xilinx ISE software tool suite and the Virtex-5 architecture.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/19/07	1.0	Initial Xilinx release.

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