White Paper

# Stratix III FPGAs vs. Xilinx Virtex-5 Devices: Architecture and Performance Comparison

*The 65-nm process node introduces new challenges in chipmakers' relentless quest to increase device performance while lowering power consumption. With state-of-the-art technology, Altera® Stratix® III FPGAs leverage the flexible logic structure of the previous-generation, 90-nm Stratix II FPGAs, and combine many innovative power-saving techniques to deliver the benefit of an efficient foundational architecture that is fully integrated in the Quartus® II development software. With Stratix III performance, designers gain a shorter design cycle and reduce cost, while implementing large designs with extremely low power consumption.*

*This white paper provides benchmarking data showing that Stratix III FPGAs are 35 percent faster than previous generation Stratix II devices, plus detailed architectural analysis demonstrating that the architecture efficiency of Stratix III FPGAs provides a 25 percent performance advantage with a 1.8X more logic packing capacity over competing 65-nm devices.*

## Introduction

Staying on pace with Moore's Law-increasing performance and density with a decrease in process geometry-has become particularly daunting as power consumption goes out of control. To provide the lowest power consumption at 65-nm, Altera Stratix III FPGAs employ several process techniques, include a dual core voltage operation, and leverage Altera's proprietary Programmable Power Technology. The core fabric of Stratix III FPGAs is built from innovative logic units known as adaptive logic modules (ALMs) that are routed with the MultiTrack interconnect architecture to provide the maximum connectivity with fewer hops. Coupling the power saving techniques on an efficient core architecture, Stratix III FPGAs deliver the industry's highest performance with the lowest power consumption.

## Stratix III Performance Advantage

Stratix III performance advantages include its efficient core architecture, easier timing closure for system-level performance (with margin), and its unique power saving techniques.

### *Benchmark Methodology*

Benchmarking FPGA performance is a complex task, and a poor benchmarking process can result in inconclusive or incorrect results. Altera has invested significantly in developing a rigorous and scientific benchmarking methodology that is endorsed by industry experts as a meaningful and accurate way to measure FPGA device performance.

For detailed information on the benchmarking methodology, refer to the FPGA Performance Benchmarking Methodology white paper at **www.altera.com/literature/wp/wpfpgapbm.pdf**.

Altera has a third-party, industry-expert-endorsed performance benchmarking methodology, which is used to compare FPGA performance between families from a single FPGA vendor and with those of competitive solutions. This ensures a consistent benchmarking environment when testing Altera devices and when comparing them to competitor devices.

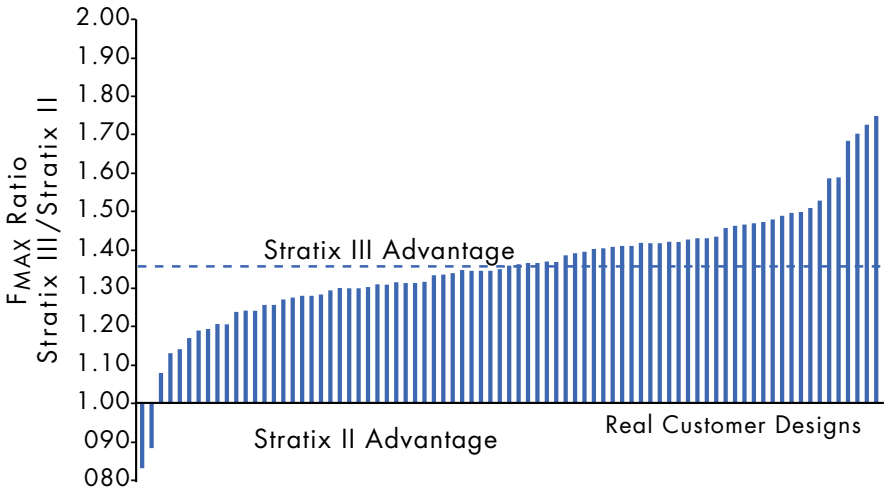
### *Core Performance*

The high performance of Stratix III devices, proven to be the industry's fastest FPGAs, can be effortlessly achieved through the unique core architecture fully integrated in Quartus II development software. Designs can be optimally synthesized with successful placement and routing for faster timing closure, thus enabling designers to increase their productivity while meeting their performance goals.

Figure 1 demonstrates a benchmarking test conducted on a suite of customer designs that shows Stratix III devices (65 nm) are, on average, 35 percent faster than Stratix II devices (90 nm).

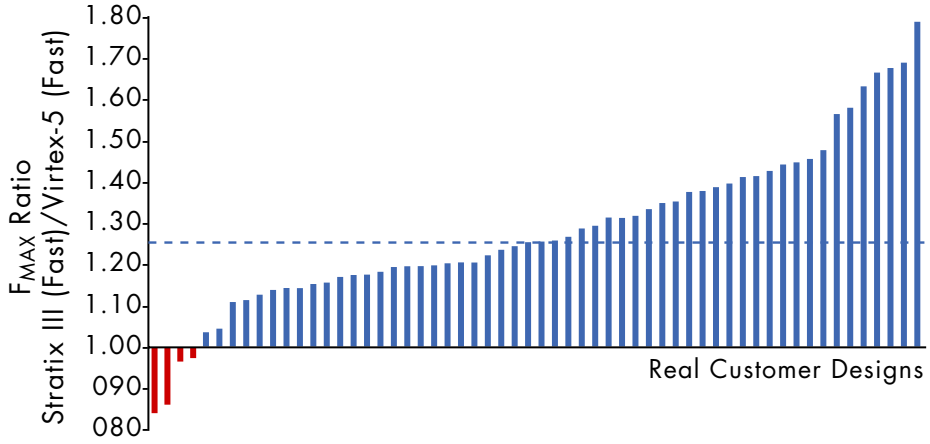
WP-01007-2.1

*Figure 1. Stratix III vs. Stratix II Benchmarking Results*




Additionally, Figure 2 shows that the fast speed grade of Stratix III FPGAs, are, on average, 25 percent faster than the fast speed grade of competing 65-nm devices. This average performance advantage is based on a set of real customer designs using the latest versions of publicly available design software.

*Figure 2. Stratix III FPGAs (Fast Speed Grade) vs. Virtex-5 (Fast Speed Grade) Benchmarking Results*




The performance advantages increase from when this paper was originally published in the fourth quarter of 2006 is due to new performance optimization techniques in Quartus II software and updated timing models that reflect the faster Stratix III silicon correlation results.

As a direct consequence of the 25 percent performance advantage of Stratix III FPGAs over the nearest competing FPGA, the slowest speed grade of Stratix III FPGAs are at par with the fast speed grade of Virtex-5. Figure 3 and Table 1 show the speed grade comparison between the two FPGA families.

In comparison to the nearest competitor's FPGAs, designers can meet their performance requirements or easily close timing in slower speed grades of Stratix III FPGAs while lowering their costs and total power consumption.

*Figure 3. Performance Comparison by Speed Grade*

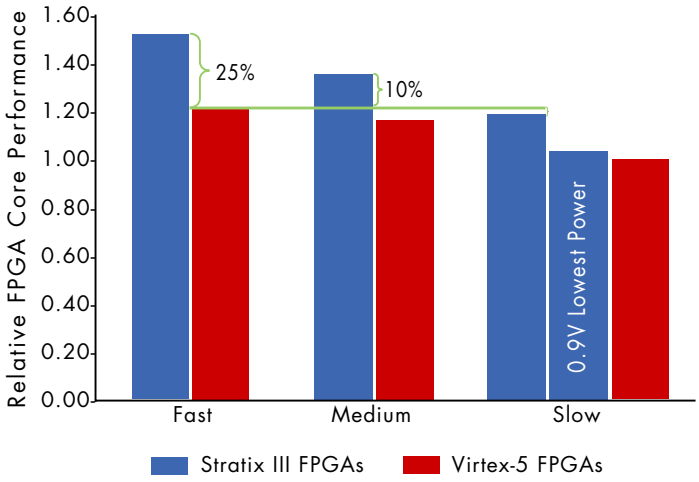



*Table 1. Performance Comparison by Speed Grade*

| Stratix III FPGA Speed Grade | Nearest Competing FPGA Speed Grade | Stratix III Performance Advantage |
|---|---|---|
| Fast | Cannot match performance | 25% faster than nearest competitor's fast speed grade |
| Medium | Cannot match performance | 10% faster than nearest competitor's fast speed grade |
| Slow | Fast | Parity |
| 0.9V, Lowest Power | Slow | Parity |

## *Stratix III FPGA Core Performance Advantage Increases With Design Size*

Figure 4 shows a plot of the $f_{MAX}$ ratio between Stratix III and Virtex-5 FPGAs on the *y*-axis and the design size on the *x*-axis. Each data point represents a real customer design. The results show that the $f_{MAX}$ ratio increases with design size because of a performance degradation in Virtex-5 FPGAs, and the Stratix III FPGA performance advantage over the nearest competing FPGA quickly increases from 25 percent to 50 percent as the design size increases (see Table 2).

*Figure 4. Stratix III FPGA Performance Advantage Increases With Design Size*

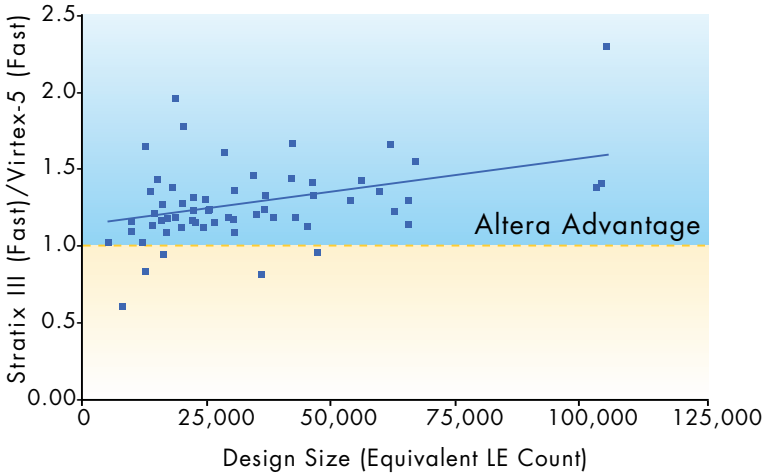


*Table 2. Stratix III FPGA Performance Advantage Increases With Design Size*

| Design Size (Logic Elements) | All Circuits | 50K - 75K | 75K - 125K | > 125K |
|---|---|---|---|---|
| Stratix III Advantage | +25% | +39% | +55% | N/A *(1)* |

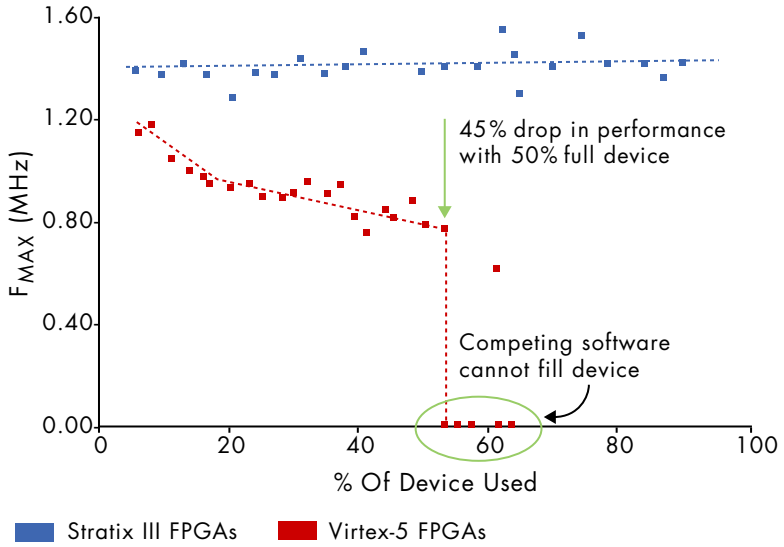
***Note:***
(1) Too many large designs failed to compile on the competitor's software to have a statistically valid sample.

## *Stratix III Performance Not Compromised With Utilization*

Figure 5 compares the performance of a parameterized customer design in Stratix III and Virtex-5 FPGAs. The size of this design was increased by varying a parameter. Each data point in Figure 5 shows a different parameterization of the same design, resulting in a different logic utilization shown on the *x*-axis. The achieved performance ($f_{MAX}$) is on the *y*-axis. The results for the same design show:

- Stratix III FPGAs have no performance degradation as the FGPA fills up.
- ISE Foundation software is unable to fit versions of the design larger than 65 percent of the device.
- A 45 percent performance degradation is seen in the nearest competing FPGA when the device was half full on this design.

*Figure 5. No Performance Degradation in Stratix III FPGAs*




## *High System-Level Performance With Margin*

While some suppliers liberally specify speeds to a point where customers are forced to assume they cannot actually meet the highest performance and manually de-rate specifications, Altera takes a conservative approach toward specifications. By using Altera FPGAs, designers are assured of meeting timing closure easily. For example, when Altera specified 333-MHz DDR2 performance (with Stratix II FPGAs), designers were actually able to get 333-MHz to work across all conditions. In fact, one customer went to production with DDR2 performance of 400-MHz. In another example, Stratix II FPGAs demonstrated ample margin in the LVDS and DDR2 specifications, capable of achieving up to 1.25 Gbps and over 400 MHz respectively. Following this trend, Stratix III FPGAs will continue to meet system-level timing requirements smoothly, and it is expected that the DDR3 and LVDS specifications are likely to increase by the end of 2007.

High system-level performance requires that, in addition to the high core performance, the on-chip RAM, digital signal processing (DSP) blocks, and I/Os must also be optimized. Stratix III FPGAs have DSP blocks that are fully optimized for the highest performances and are able to support clock rates of 550 MHz. Stratix III FPGAs provide

orders of magnitude higher performance, up to 537 giga multiply-accumulate operations per second (GMACs), than any single-chip DSP processor available today.

The TriMatrix on-chip memory offers three flavors of memory structures: 640-bit MLABs, 9-Kbit blocks (M9K), and 144-Kbit blocks (M144K). These blocks are optimized for maximum efficiency, and the MLABs can be placed anywhere in the device, making them extremely flexible and able to support clocks rates over 600 MHz. With the TriMatrix on-chip memory and DSP blocks, Stratix III devices are ideal for video and image processing, high-speed digital communications, and other high-performance DSP applications. The FPGA core block performance is shown in Table 3.

*Table 3. Stratix III FPGA Block Performance*

| Block | Stratix III (65 nm) | Virtex-5 (65 nm) |
|---|---|---|
| Max Internal Clock Speed | 600 MHz | 550 MHz |
| On-Chip RAM | 600–625 MHz | 550 MHz |
| DSP Block | 550 MHz | 550 MHz |

To complement the high-performance core, Stratix III FPGAs are designed with high-performance I/Os allowing high-bandwidth interfaces to external devices. For example, external memory devices interface with Stratix III I/Os through dedicated memory interface circuitry catering to the high-performance memory interfaces like DDR3 and QDR II+. Stratix III FPGAs are the only FPGAs today to support DDR3 DIMMs and QDR II+ at 400 MHz. In addition, DDR2, QDR2 II, and RLDRAM II performance have been increased from Stratix II devices (summarized in Table 4). Altera works with leading vendors to ensure users can connect the very latest memory devices to Stratix III FPGAs.

*Table 4. Stratix III FPGA I/O Performance*

| Interconnect | Stratix III (65 nm) | Virtex-5 (65 nm) |
|---|---|---|
| DDR2 | 400 MHz | 333 MHz |
| DDR3 | 400+ MHz *(1)* | No DIMM support |
| QDR II | 350 MHz | 300 MHz |
| QDR II+ | 400 MHz | Not Supported |
| RLDRAM II | 400 MHz | 300 MHz |
| LVDS | 1.25 Gbps *(1)* | 1.25 Gbps |

***Note:***
(1) Specification expected to increase by end of 2007.

Using these advanced features and customizable intellectual property (IP), designers can quickly and easily integrate a wide range of applications into complex system designs without compromising performance in Stratix III FPGAs.

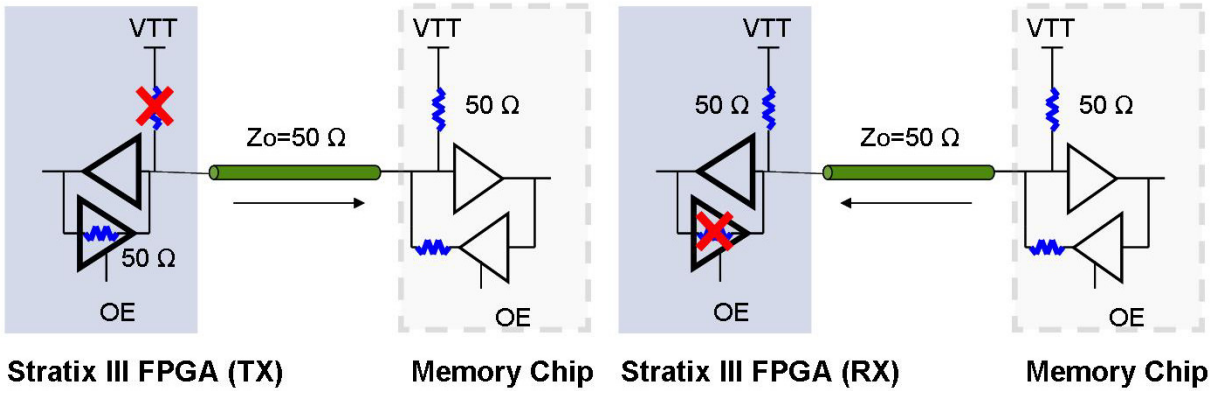
## *Low Power*

Stratix III FPGAs were developed with the latest process and new architecture innovations to minimize power while delivering the highest performance. Its unique power-conserving features include:

- *Programmable Power Technology:* This enables the Stratix III logic fabric to be programmed at the LAB level to provide high-speed logic or low-power logic depending on what is required by the specific design. In this way, only the small fraction of the design that is timing critical gets the high-speed setting. The rest can utilize the low-power setting, resulting in a dramatic decrease in leakage power for the low-power logic.
- *Selectable Core Voltage:* The user has the choice of 1.1V or 0.9V to achieve the required performance while saving on power by lowering the core voltage.
- *Process and circuit technologies:* Technologies like multi-threshold transistors, variable gate-length transistors, low-k dielectric, triple-gate oxide (TGO), and strained silicon are employed in Stratix III devices to keep power under control.

- *Dynamic on-chip termination (OCT):* Stratix III FPGAs have a built-in dynamic OCT scheme that allows the parallel and series termination to be swapped on the fly during a read or write operation. This scheme reduces not only cost but also I/O power by removing the path from the power rail to ground that would normally exist across a parallel termination. As an example, on a 72-bit DDR3 DIMM running at 200 MHz, Stratix III FPGAs save up to 2.3 W of power when compared to a standard DDR2 implementation without OCT. Figure 6 illustrates the dynamic OCT scheme.

*Figure 6. Dynamic OCT in Stratix III FPGAs*




- *Software power modeling and optimization:* Using all the power-saving features available in Stratix III devices becomes automatic and effortless with the Quartus II design software. Power optimization techniques such as power-driven synthesis and place and route can provide 10 to 40 percent reduction in dynamic power (design dependent).

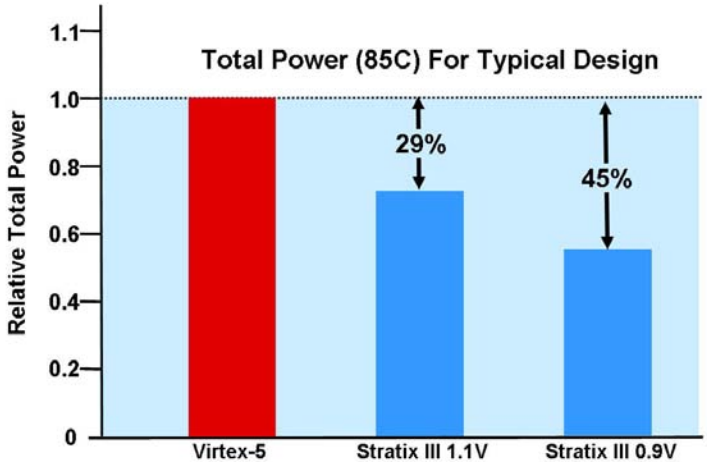
Exploiting the available power saving techniques, Stratix III FPGAs offer, on average, a 64 percent static power reduction and a 55 percent dynamic power reduction at 0.9V when compared to Stratix II FPGAs at 1.2V. The values in Table 5 are normalized to Stratix II FPGAs and are derived from the publicly available Early Power Estimator (EPE) tools.

*Table 5. Static and Dynamic Power Comparison in Stratix III and Stratix II FPGAs*

| Power Component | Stratix III | | Stratix II |
|---|---|---|---|
| | 0.9V | 1.1V | 1.2V |
| Relative Static Power | 0.36 | 0.48 | 1 |
| Relative Dynamic Power | 0.45 | 0.67 | 1 |

Competitively, Stratix III FPGAs provide on average 29 percent (at 1.1V) and 45 percent (at 0.9V) lower total power than the nearest competing FPGA. Figure 7 shows the total power advantage seen in Stratix III FPGAs over Virtex-5.

*Figure 7. Total Power Comparison Between Stratix III FPGAs and Virtex-5* (1)




***Note:***

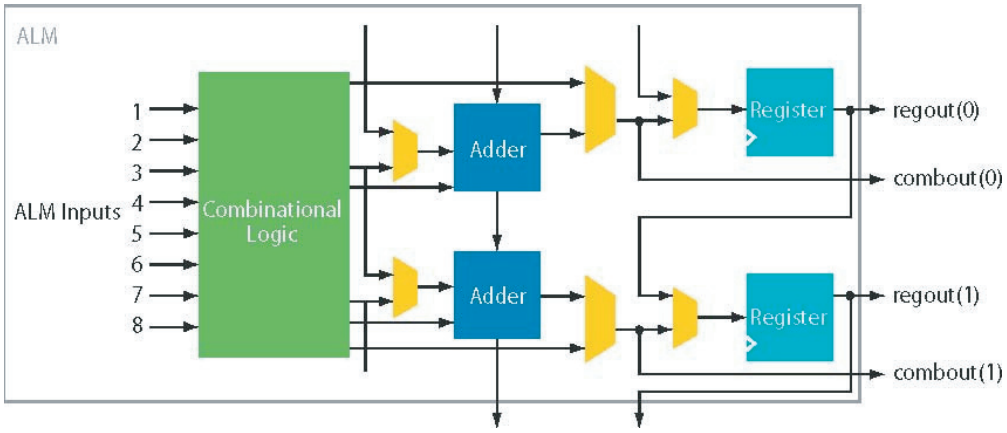
(1) Typical design resource utilization was used to derive relative total power which includes 12.5 percent toggle rates, 80 percent logic utilization, 50 percent memory utilization, 50 percent DSP block utilization, a single 200 MHz 72-pin DDR3 interface with dynamic on-chip termination, 32 in/32 out 800-MHz LVDS pins, 128 in/128 out 2.5V I/O, and 64 in/64 out 1.8V I/O.

For an in-depth description of Stratix III power-saving techniques, read the Stratix III Programmable Power white paper at **www.altera.com/literature/wp/wp-01006.pdf**.

## Architecture Advantage

The key to high performance in Stratix III FPGAs is the area-efficient adaptive logic module (ALM). It consists of combinational logic, two registers, and two adders, as shown in Figure 8. The combinational portion has eight inputs and includes a look-up table (LUT) that can be divided between two adaptive LUTs (ALUTs) using Altera's patented LUT technology. An entire ALM is needed to implement an arbitrary 6-input function, but because it has eight inputs to the combinational logic block, one ALM can implement various combinations of two functions.

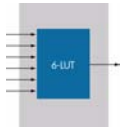
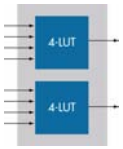
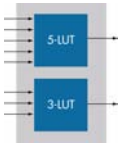
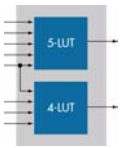
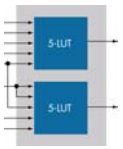
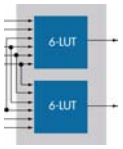
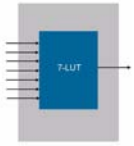
*Figure 8. ALM Block Diagram*




In addition to implementing a full 6-input LUT, the ALM can, for example, implement two independent 4-input functions or a 5-input and a 3-input function with independent inputs. (Table 6 shows a summary of combinational logic configurations supported in an ALM.) Because two registers and two adders are available, the ALM has the flexibility to implement 2.5 logic elements (LEs) of a classic 4-input LUT (4-LUT) architecture, consisting of a 4-LUT, carry logic, and a register.

For a more detailed architectural description, refer to the Stratix III Device Handbook at **www.altera.com/literature/hb/stx3/stratix3_handbook.pdf**.

*Table 6. ALM Flexibility*

| Configuration | Description |
|---|---|
|  | One Stratix III ALM can input any 6-input function. |
|  | One Stratix III ALM can be configured to implement two independent 4-input or smaller LUTs. This configuration can be viewed as the “backward-compatibility” mode. Designs that are optimized for the traditional 4-LUT FPGAs can easily be migrated to the Stratix family. |
|  | One Stratix III ALM can be configured to implement a 5-LUT and 3-LUT. The inputs to the two LUTs are independent of each other. The 3-LUT can be used to implement any logic function that has three or fewer inputs. Therefore, a 5-LUT/2-LUT combination is also available. |
|  | One Stratix III ALM can be configured to implement a 5-LUT and a 4-LUT. One of the inputs is shared between the two LUTs. The 5-LUT has up to 4 independent inputs. The 4-LUT has up to three independent inputs. The sharing of inputs between LUTs is very common in FPGA designs, and the Quartus II software automatically seeks logic functions that are structured in this manner. |
|  | One Stratix III ALM can be configured to implement two 5-LUTs. Two of the inputs between the LUTs are common, and up to three independent inputs are allowed for each 5-LUT. |
|  | If two 6-input functions have the same logic operation and four shared inputs, the two 6-input functions can be implemented in one Stratix III ALM. An example of this is a 6-input AND gate. An ALM can implement two 6-input AND gates that have four common inputs. |
|  | One Stratix III ALM in the extended mode can implement a subset of a 7-variable function. The Quartus II software automatically recognizes the applicable 7-input function and fits it into an ALM.*(1)* |

***Note:***

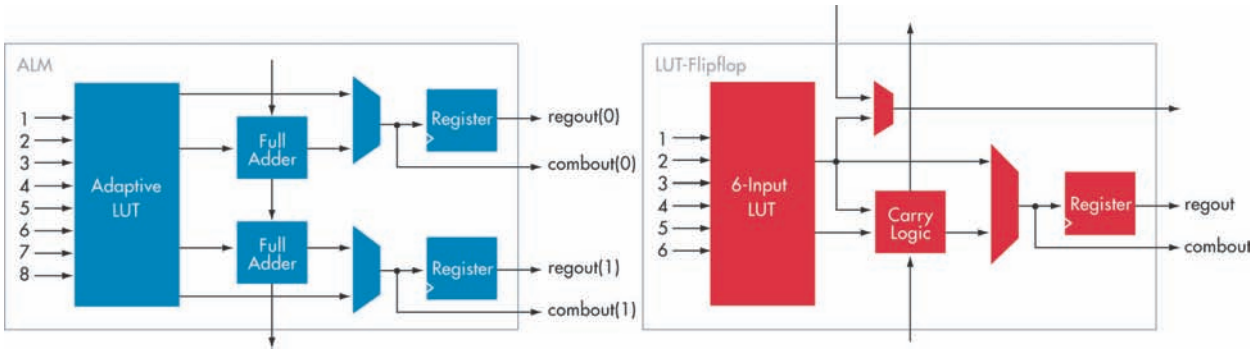
(1) Refer to the Stratix III Device Handbook (**www.altera.com/literature/hb/stx3/stratix3_handbook.pdf**) for detailed information about the types of 7-input functions that can be implemented in an ALM.

The ALM also contains two registers and two adders as shown in Figure 2. The extra register was added because experiments indicated that many customer applications required a higher than 1:1 ratio of registers and LUTs. Two extra adders were included to enhance the arithmetic capability of the ALM, allowing for two 2-bit addition or two

3-bit addition per ALM. Thus, the ALM provides twice as much register and arithmetic capability as a basic 6-LUT, making it a superior building block.

The ALM, introduced more than two years ago, is significantly more flexible and, as a result, is more area efficient than the Xilinx Virtex-5 logic element (also called a LUT-flipflop pair). The logic element consists of a basic 6-LUT, carry logic, and a single register as shown in Figure 9. In comparison, the combinational logic portion of the ALM has eight inputs and supports all 6-input functions plus many other combinations of smaller functions using its two outputs. The combinational logic portion of the Virtex-5 logic element, a basic 6-LUT, also has 64 bits of CRAM and two outputs like the ALM, but only contains 6 inputs and has a limited ability to implement more than one logic function. One of its outputs is the output of the 6-LUT and the other is the 5-LUT, corresponding to the lower half of the configuration RAM.

*Figure 9. Comparing the Stratix III ALM and the Virtex-5 LUT-Flipflop Pair*




Although the basic 6-LUT has the ability to implement two smaller functions, it will usually be used only as a 6-LUT. Because the LUT only has six inputs, the required number of shared inputs places severe restrictions on the types of functions that can be combined. These restrictions make using the basic 6-LUT as two 5-LUTs a rare occurrence. In contrast, the two additional inputs in the Stratix III ALM allow it to be used as two fully functional 5-LUTs, providing a significant area advantage.

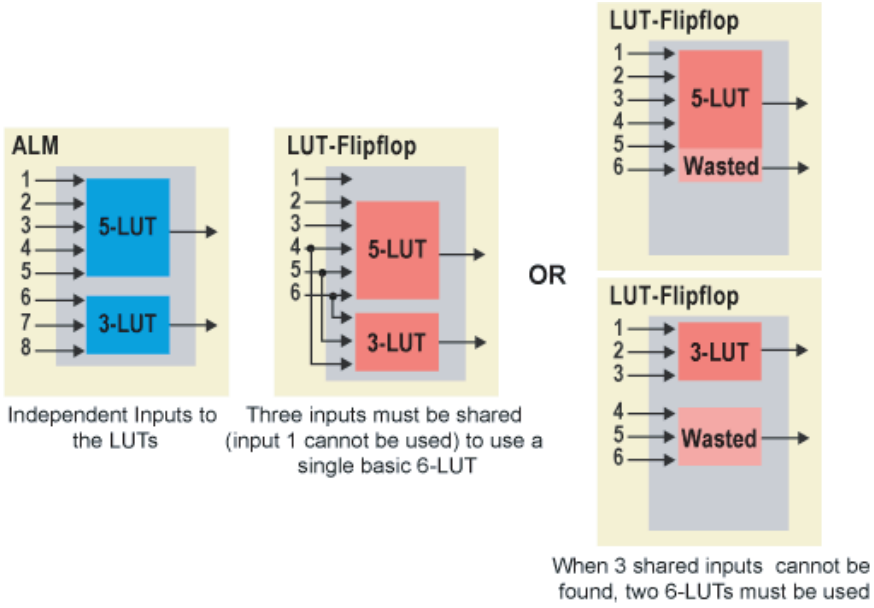
Table 7 gives the number of shared inputs required for a few combinations of functions. For example, the ALM can implement two independent 4-input functions (no inputs shared), while the Virtex-5 LUT requires three shared inputs. Figure 10 shows another example: the ALM can implement a 5-input and a 3-input function without any shared inputs, while the Virtex-5 LUT requires three shared inputs. It is difficult to find functions that can be packed into a Virtex-5 LUT, resulting in functions with less than six inputs being implemented in 6-LUT resources.

*Table 7. Stratix III ALM vs. Virtex-5 LUT Flexibility*

| Output 1 | Output 2 | Virtex-5 | ALM Shared Inputs (Minimum) |
|---|---|---|---|
| 5-LUT | 5-LUT | 5 | 2 |
| 5-LUT | 4-LUT | 4 | 1 |
| 5-LUT | 3-LUT | 3 | 0 |
| 4-LUT | 4-LUT | 3 | 0 |
| 4-LUT | 3-LUT | 2 | 0 |
| 3-LUT | 3-LUT | 1 | 0 |

Combining the 8-input fracturable LUT and 2:1 register to LUT ratio, the ALM can effectively implement two independent functions that may require a flipflop each without the need to share inputs or resources. The result is that, in virtually any design, implementation requires fewer ALMs than Virtex-5 logic elements (see Figure 10).

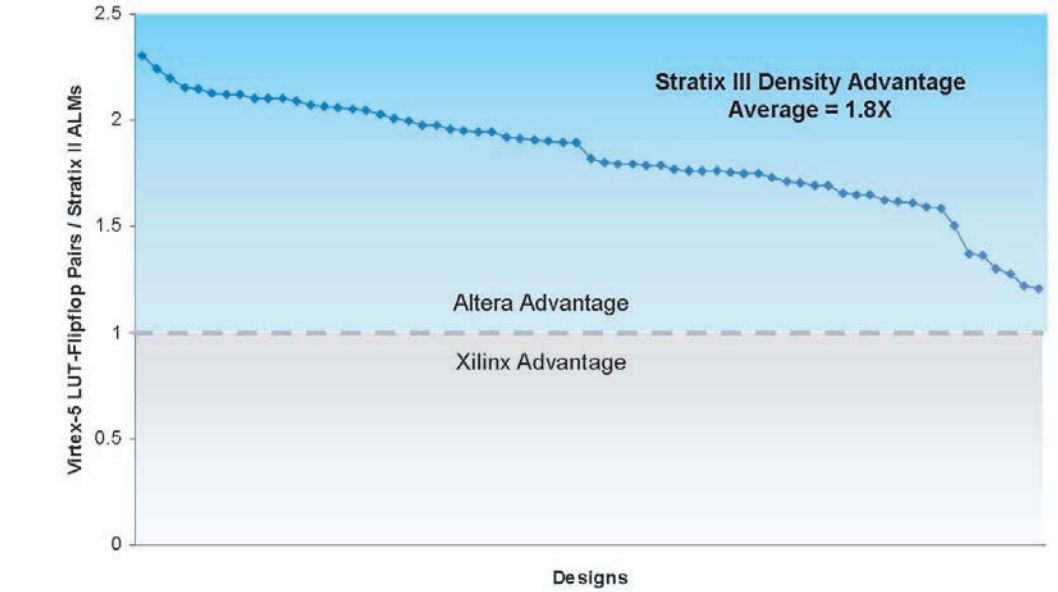
*Figure 10. Implementing 5- and 3-Input Functions in Stratix III ALM and Virtex-5 LUT-Flipflop Pair*




## Capacity Benchmarking

Capacity benchmarks on over 65 real-world designs (optimized for minimum area) were run to measure the capacity of Stratix III devices compared to Virtex-5 devices. The capacity benchmarks provide an average relative measure of capacity for Altera's ALM and Xilinx LUT-flipflop pair. Because of efficient fracturability, the Stratix III ALM has, on average, a 1.8X advantage over the Virtex-5 LUT-flipflop pair. On certain designs, the advantage can be as high as 2.3X, as shown in Figure 11. The horizontal black line at the "1" mark indicates a point at which the number of logic elements for Virtex-5 (LUT-flipflop pairs) and Stratix III (ALMs) are the same.

*Figure 11. Capacity Benchmark Comparing Stratix III ALM With Virtex-5 LUT-Flipflop Pairs*

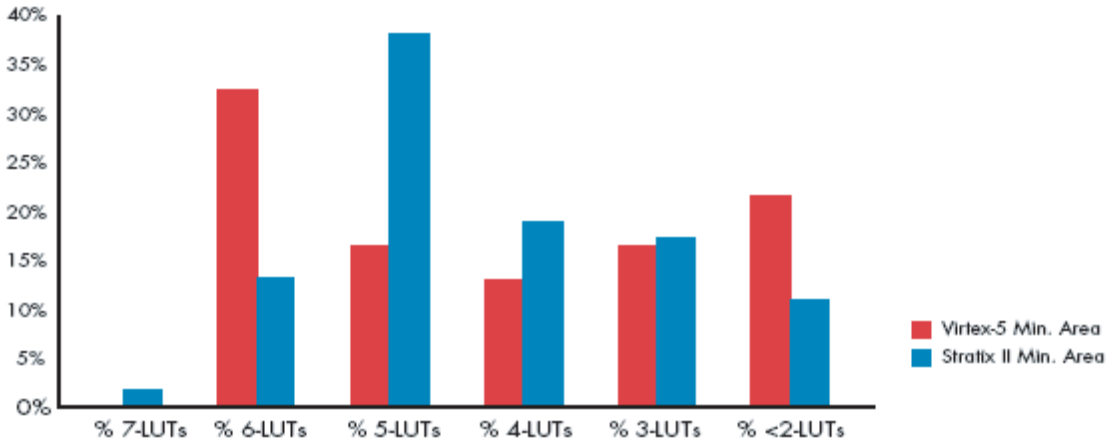



***Note:***

(1) 10 out of 75 customer designs resulted in errors when optimized for area in the latest version of ISE design software.

To better understand these results, a breakdown of LUT sizes generated by synthesis is shown in Figure 12. The graph clearly illustrates that synthesis generates a much larger percentage of 6-LUTs for Virtex-5 devices than for Stratix III devices, 32 percent versus 13 percent. The reason for this difference is that, when using a basic 6-LUT such as Virtex-5, it is desirable to use as many inputs as possible because the entire LUT is used in most cases regardless of whether the function requires six inputs or fewer. Since Virtex-5 can only efficiently implement 6-LUTs, synthesis attempts to generate as many 6-LUTs as possible. Attempting to create smaller functions does not make sense because it is unlikely that two can be packed given the number of inputs that need to be shared.

*Figure 12. LUT Sizes Generated During Synthesis*

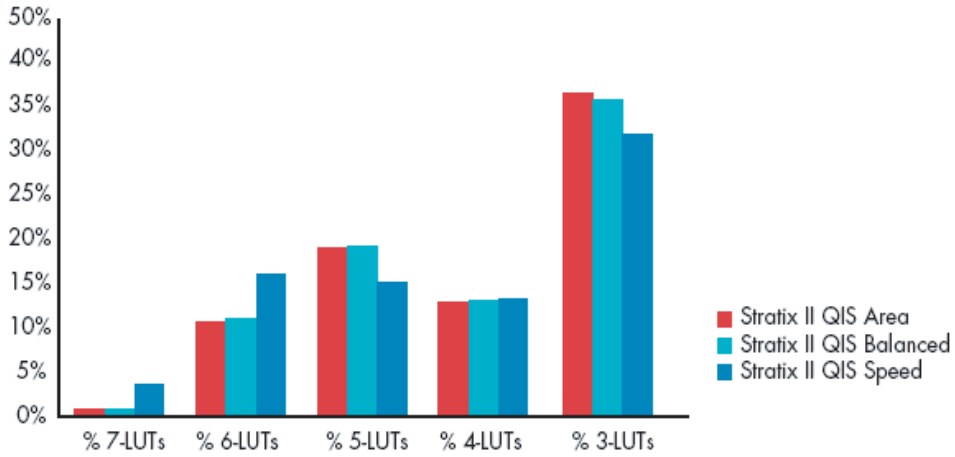



Because of the LUT fracturability, the synthesis tool can alter the distribution of LUT sizes to produce the right mix of large and small functions, and will result in fewer ALMs being used. Specifically, any function of five or fewer inputs uses only half the ALM, making it more important to use the 6-input functions only for speed-critical logic.

The ALM provides flexibility for software optimization. Figure 13 shows three distributions of LUT sizes produced by Quartus II integrated synthesis (QIS) when optimizing for three different goals: speed, area, or a balanced approach. The mixture of LUT sizes varies depending on the goal. When optimizing for speed, the largest number of 6-LUTs is generated; when optimizing for area, a different distribution that packs in the smallest number of ALMs is generated. This flexibility is unique to Altera and is the result of an intensive research effort on the interaction between software and hardware during architecture development to achieve optimal results.

For an in-depth description of the ALM design and research, read the Stratix II *FPGA Architecture* (the foundation of Stratix III architecture) white paper at **www.altera.com/literature/wp/wp-01003.pdf**.

*Figure 13. Distributions of Functions Generated by QIS*




Based on extensive benchmark analysis done using real customer designs and a full synthesis, placement, and routing design flow targeted for minimum area, the Stratix III ALM "is equivalent to" or "can hold as much logic as" 1.8X Virtex-5 logic elements (see Table 8).

*Table 8. Normalized Relative Logic Capacity*

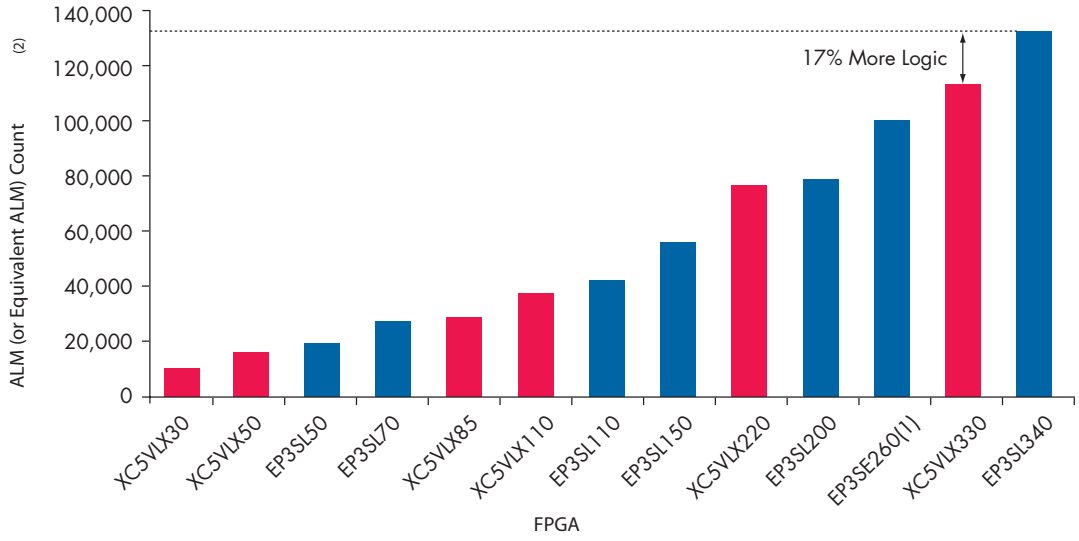
| Stratix III ALM | Virtex-5 LUT FF Pair |
|---|---|
| 1.8 | 1 |

Taking the 1.8X factor into account, an EPSL340 device has 17 percent more logic than XC5VLX330 (see Table 9 and Figure 14).

*Table 9. Stratix III and Virtex-5 Equivalent Device Match-Up*

| Altera Device | ALMs | Registers | Xilinx Device | Equivalent ALMs *(2)* | 6-LUTs | Registers |
|---|---|---|---|---|---|---|
| | | | XC5VLX30 | 10,667 | 19,200 | 19,200 |
| | | | XC5VLX50 | 15,556 | 28,000 | 28,000 |
| EP3SL50 | 19,000 | 38,000 | | | | |
| EP3SL70 | 27,000 | 54,000 | | | | |
| | | | XC5VLX85 | 28,800 | 51,840 | 51,840 |
| | | | XC5VLX110 | 38,400 | 69,120 | 69,120 |
| EP3SL110 | 42,600 | 85,200 | | | | |
| EP3SL150 | 56,800 | 113,600 | | | | |
| | | | XC5VLX220 | 76,800 | 138,240 | 138,240 |
| EP3SL200 | 79,560 | 159,120 | | | | |
| EP3SE260 *(1)* | 101,760 | 203,520 | | | | |
| | | | XC5VLX330 | 115,200 | 207,360 | 207,360 |
| EP3SL340 | 135,200 | 270,400 | | | | |

*Figure 14. Stratix III L vs.Virtex-5 LX Logic Capacity Comparison* (1)(2)



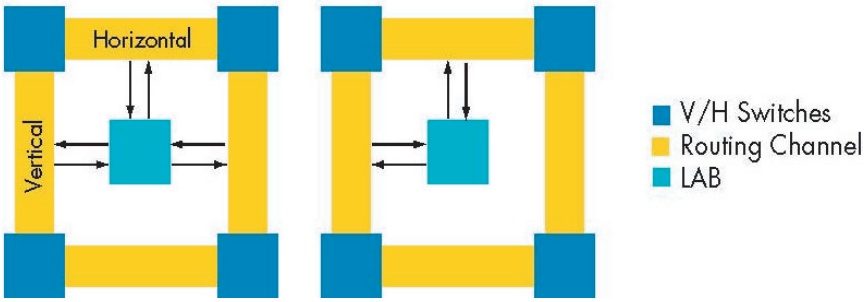

***Notes:***
(1) The EP3SE260 provides optimum logic, DSP, and memory for this device density
(2) Converting Virtex-5 6-LUT to ALM count using 1.8X factor

## Routing Architecture

In addition to logic block architecture, another key FPGA feature is its routing architecture. The Stratix series of devices introduced the MultiTrack interconnect to maximize connectivity and performance. The routing architecture provides the connectivity between different clusters of logic blocks, called logic array blocks (LABs), and can be measured by the number of "hops" required to get from one LAB to another. The fewer the number of hops and more predictable the pattern, the better the performance and the easier it is for CAD tool optimization.

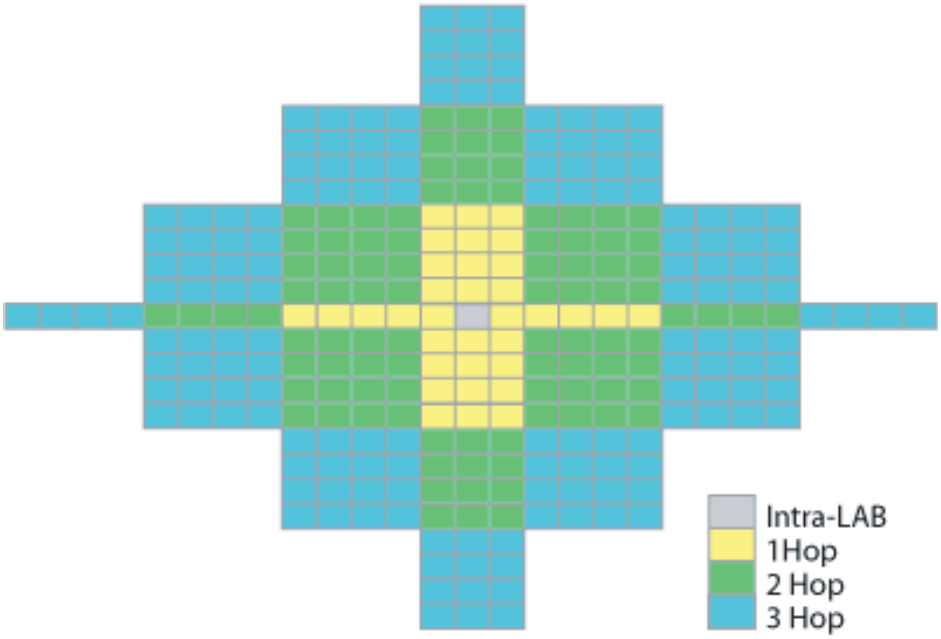
Routing is organized as wires in a number of rows and columns. The Stratix series family uses a three-sided routing architecture, shown in Figure 15. This means that a LAB can drive or listen to all of the wires on one horizontal (H) channel above it and two vertical (V) channels to the left and right side of it. The channels contain wires of length 4, 8, 16, and 24, and signals can get off at any LAB along the length of the wire.

*Figure 15. Number of Routing Architecture Sides*




Considering only wires of length four for simplicity, Figure 16 shows the number of hops required to connect to LABs from a given LAB located at the location denoted by the gray box.

*Figure 16. Stratix Series Connectivity*




The Virtex architectures use a two-sided routing architecture because a configurable logic block (CLB) can connect to all of the wires in a single vertical channel and a single horizontal channel (with connectivity to half of the wires above and to half of the wires below the CLB). In addition, it uses wires that can only connect to CLBs at select points along the length of the wire. Both of these factors place restrictions on connectivity and placement. With Virtex-5 devices, a CLB can still talk to two channels, but has also included L-shaped (referred to in Xilinx material as diagonal) wires to improve connectivity.

Table 10 compares the connectivity of the Stratix III family with Virtex-5 in terms of the number of LABs/CLBs reachable in a given number of hops. In Stratix III devices, many more LABs (34) can be reached in one hop than CLBs in Virtex-5 devices. If the numbers are scaled by the greater efficiency of the ALM, the results are even more favorable to Stratix III devices. Because a LAB contains the equivalent of 25 4-LUT-based LEs versus the approximately 11 of Virtex-5 (using the 1.8X factor), if we scale the amount of logic that can be reached within a given number of hops by these factors, the improved routing connectivity in terms of logic capacity is even greater.

*Table 10. Stratix III vs. Virtex-5 Connectivity*

| Hops | Number of LABS/CLBs Reachable | | Number of LEs Reachable | | Ratio of Stratix III LEs to Virtex-5 LEs |
|---|---|---|---|---|---|
| | Stratix III | Virtex-5 | Stratix III *(1)* | Virtex-5 | |
| 1 | 34 | 12 | 850 | 132 | 6.4 |
| 2 | 96 | 96 | 2,400 | 1,056 | 2.3 |
| 3 | 160 | 180 | 4,000 | 1,980 | 2.0 |
| Total | 290 | 288 | 7,250 | 3,168 | 2.3 |

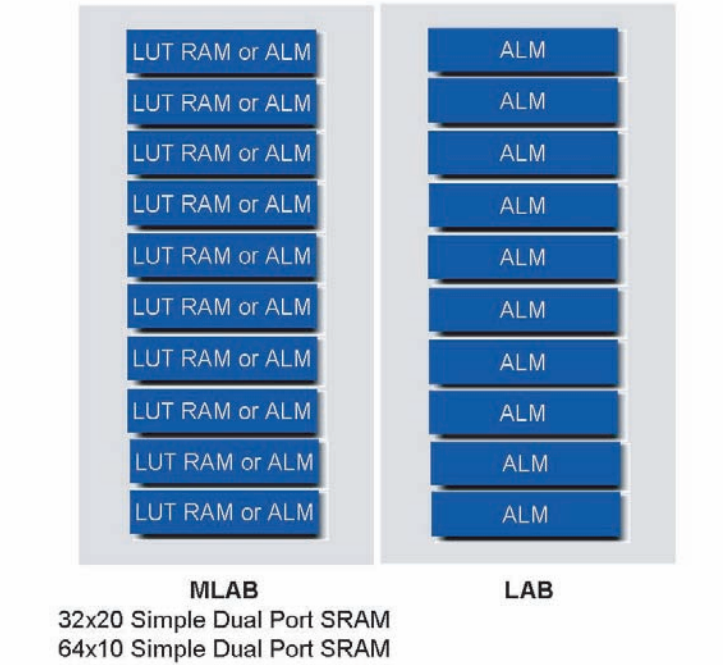
***Note:***
(1) 1 ALM = 2.5 LEs and each LAB = 10 ALMs

## Memory LABs

The Stratix III FPGA consists of LABs, with each LAB consisting of 10 flexible ALMs, which in turn are configurable to implement logic functions, register functions, and complex arithmetic functions.

New for the Stratix III FPGA core is a second flavor of the LAB, known as the memory LAB (MLAB). The LAB and MLAB coexist as pairs in Stratix III FPGAs and the MLAB ALM can be used as a regular LAB ALM or can be configured as a dual-port static random access memory (SRAM), as shown in Figure 17.

*Figure 17. Stratix III MLAB*




This LUT-RAM capability to the LAB supports a maximum of 640 bits, which can be configured as 64x10 or 32x20 simple dual port SRAM blocks as compared to the CLB of Virtex-5 that can only support a 64x4 configuration. The SRAM blocks have been optimized to implement filter delay lines, small FIFO buffers, and shift registers with maximum performance of 650-MHz clock speeds. Table 11 shows the device match-up Stratix III and Virtex-5 device families, with EP3SL340 having 4.3 Mbits of LUT-RAM.

*Table 11. Distributed RAM for Stratix III and Virtex-5 Devices*

| Stratix III | | | Virtex-5 | | | |
|---|---|---|---|---|---|---|
| **Devices** | **ALMs** | **LUT-RAM (bits)** | **Devices** | **6-LUTs** | **Equivalent ALMs** | **Distributed RAM (bits)** |
| | | | XC5VLX30 | 19,200 | 10,667 | 0.3K |
| | | | XC5VLX50 | 28,000 | 15,556 | 0.5K |
| EP3SL50 | 19,000 | 0.6M | | | | |
| EP3SL70 | 27,000 | 0.9M | | | | |
| | | | XC5VLX85 | 51,840 | 28,800 | 0.8K |
| | | | XC5VLX110 | 69,120 | 38,400 | 1.1M |
| EP3SL110 | 42,600 | 1.4M | | | | |
| EP3SL150 | 56,800 | 1.8M | | | | |
| | | | XC5VLX220 | 138,240 | 76,800 | 2.3M |
| EP3SL200 | 79,560 | 2.6M | | | | |
| EP3SE260 *(1)* | 101,760 | 3.3M | | | | |
| | | | XC5VLX330 | 207,360 | 115,200 | 3.4M |
| EP3SL340 | 135,200 | 4.3M | | | | |

## Conclusion

Due to spiraling power consumption, shrinking process nodes and innovations in process technology are no longer enough to deliver the benefits of Moore's Law. Stratix III FPGAs leverage the highly efficient Stratix II FPGA core, introduce several architectural power-saving techniques such as Programmable Power Technology, and have optimized I/Os to deliver the highest performance with the lowest power consumption. In addition, Quartus II software fully and automatically exploits every feature in Stratix III FPGAs to maximize the design engineer's productivity.

## Further Information

- *FPGA Architecture*: **www.altera.com/literature/wp/wp-01003.pdf**
- *Stratix II Performance and Logic Efficiency Analysis*: **www.altera.com/literature/wp/wpstxiiple.pdf**
- *Stratix II Logic and Routing Architecture* (foundation of Stratix III core architecture): **www.altera.com/literature/cp/cp-01005.pdf**
- *Improving FPGA Performance and Area Using an Adaptive Logic Module*: **www.altera.com/literature/cp/cp-01004.pdf**
- *Fracturable FPGA Logic Elements*: **www.altera.com/literature/cp/cp-01006.pdf**
- Benchmarking Methodology: **www.altera.com/products/devices/performance/benchmark/per-benchmarkmeth.html**

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