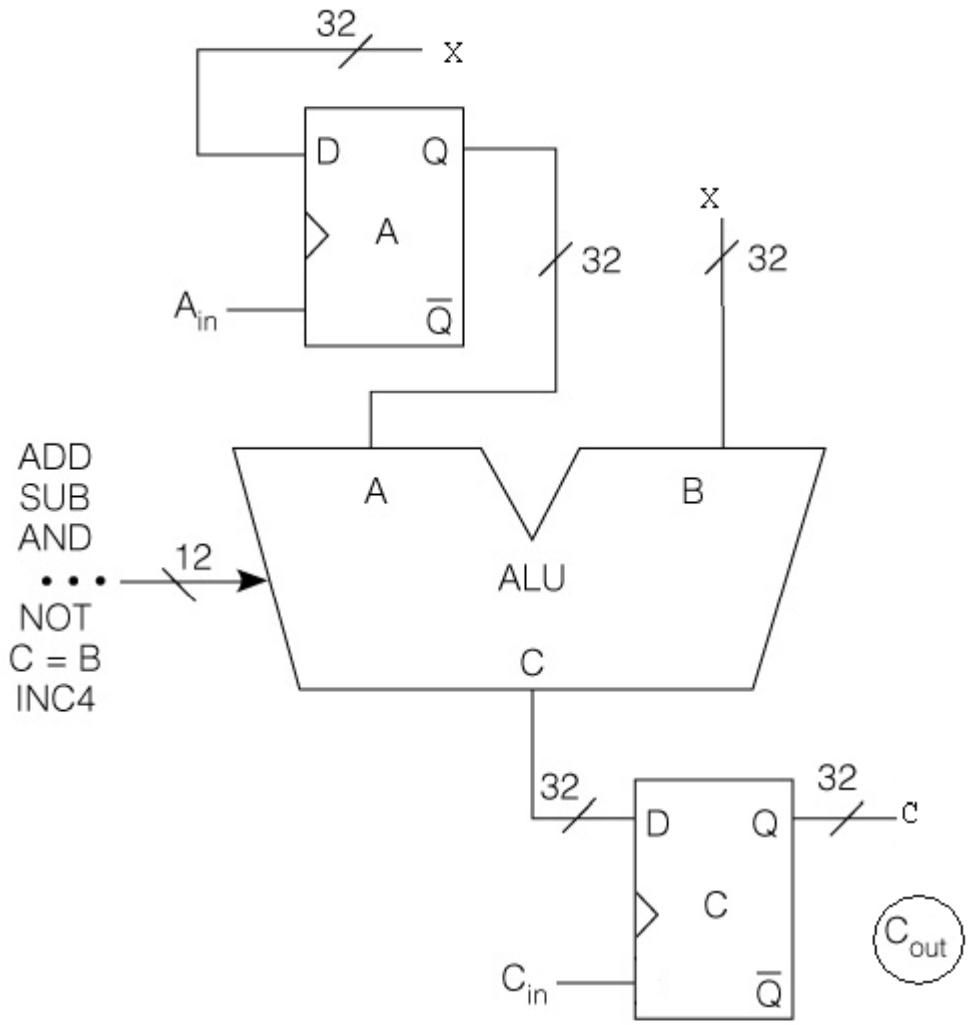
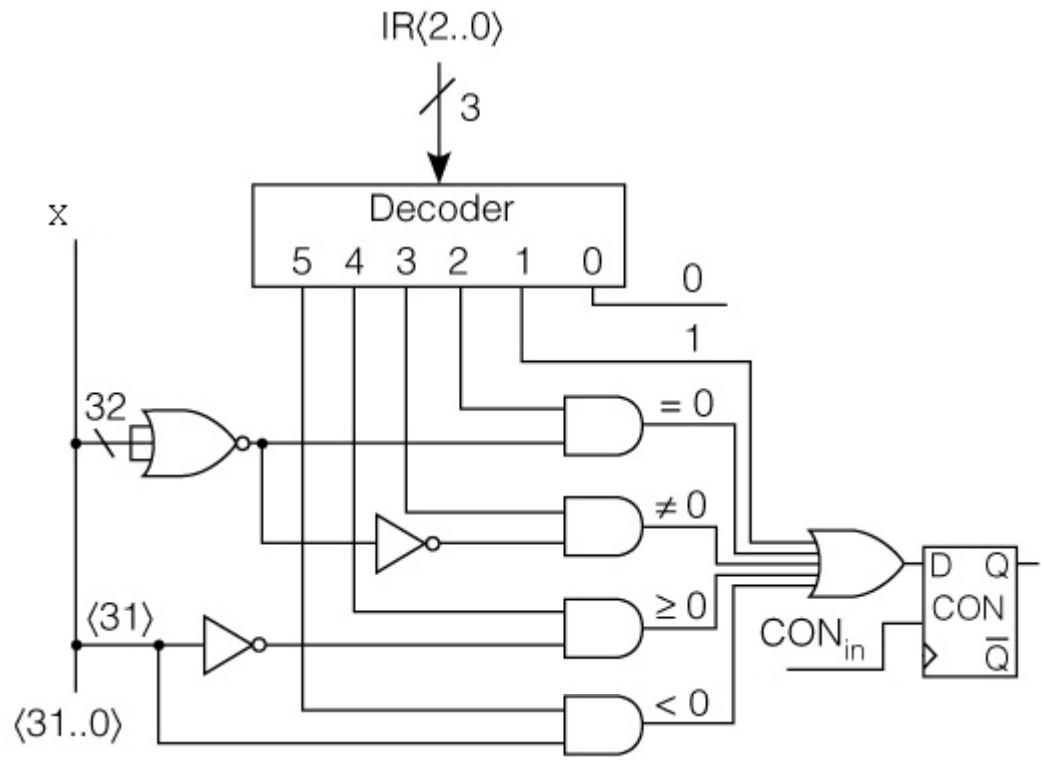
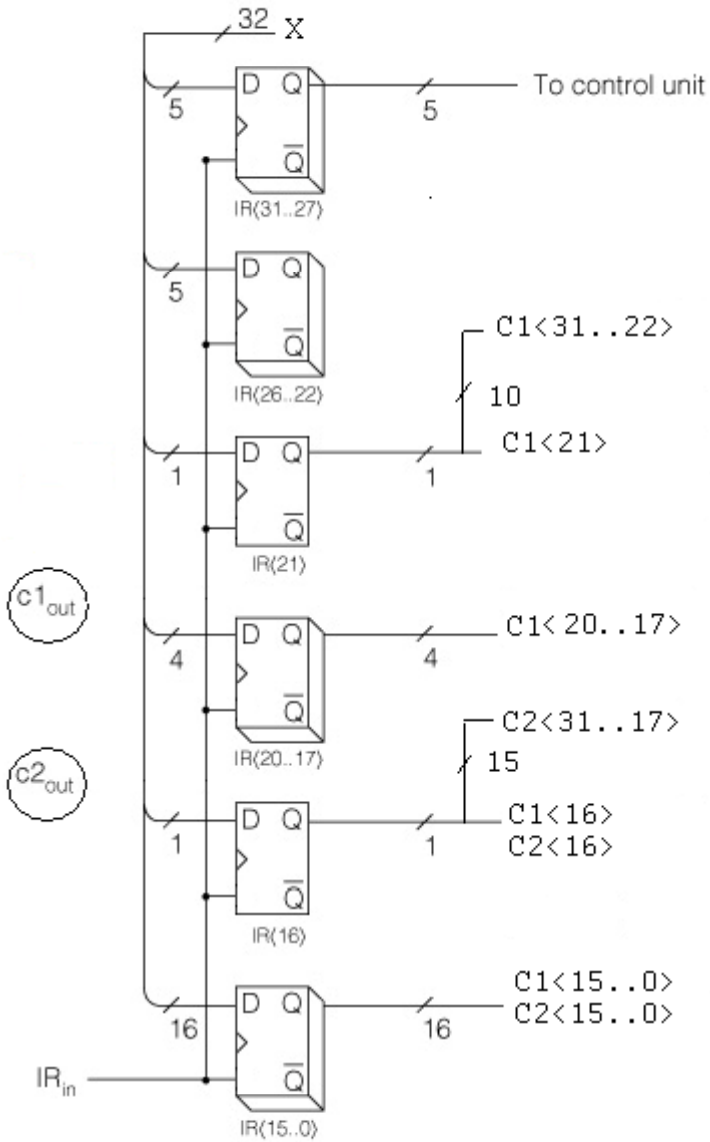
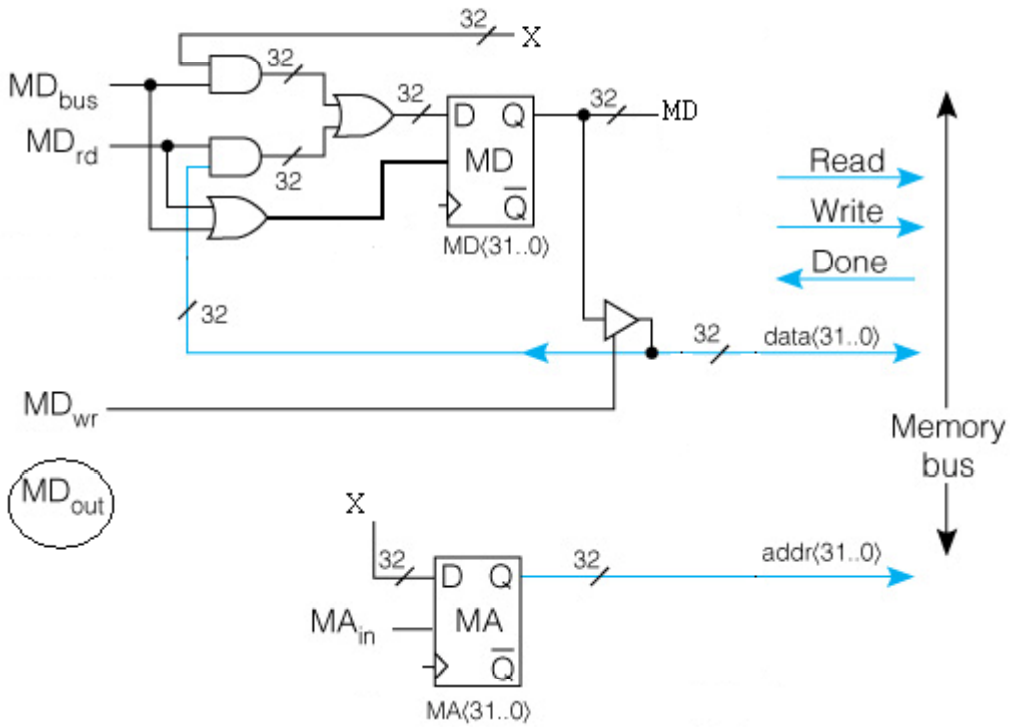
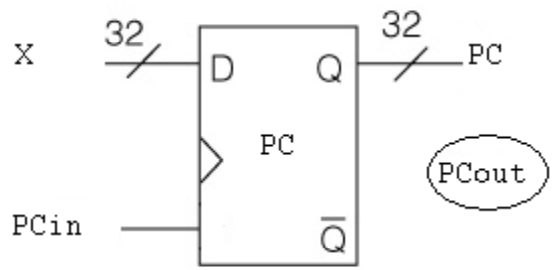
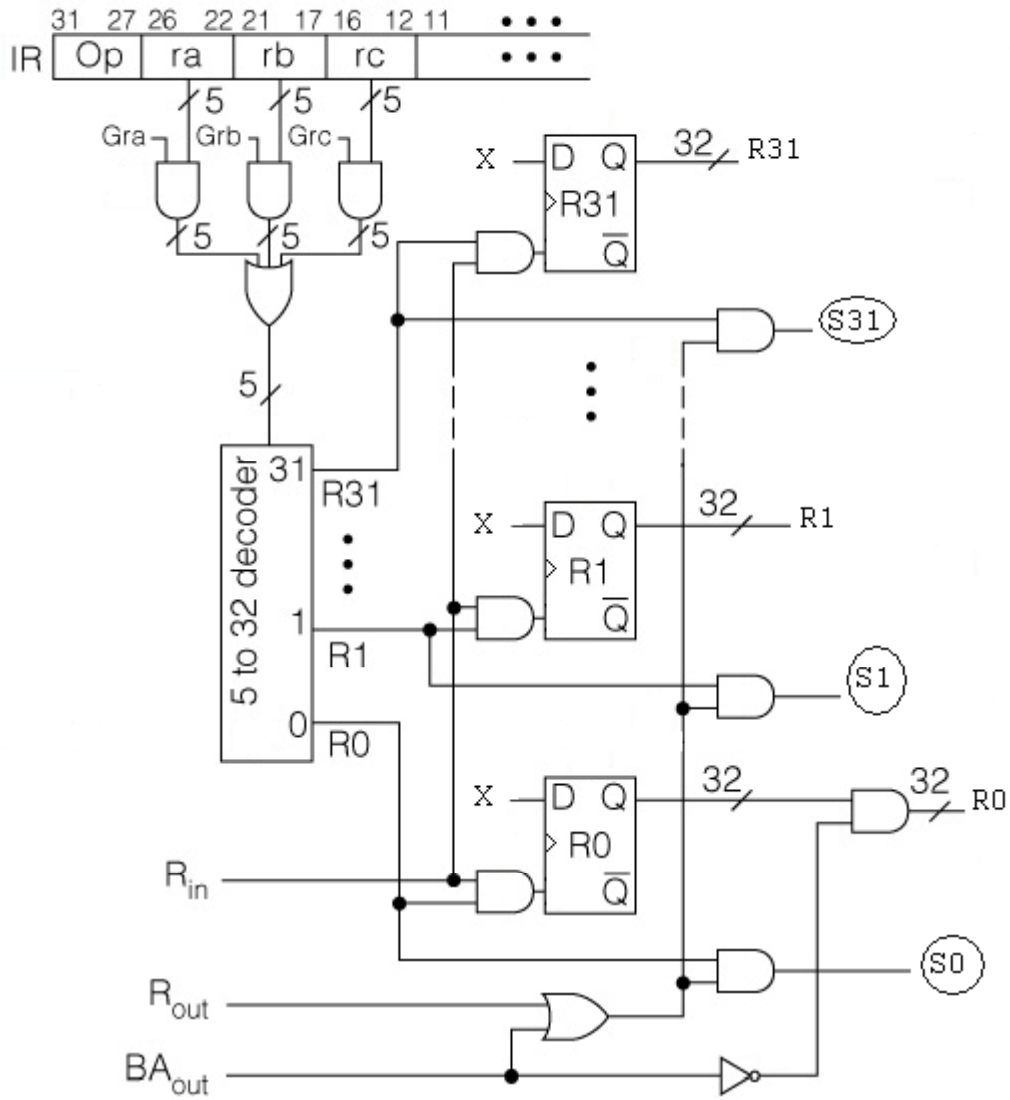

32
x
D
Q
A
A_{in}
$\overline{Q}$
32
x
32
ADD
SUB
AND
• • •
NOT
C = B
INC4
12
A
B
ALU
C
32
32
D
Q
c
C
C_{in}
$\overline{Q}$
C_{out}

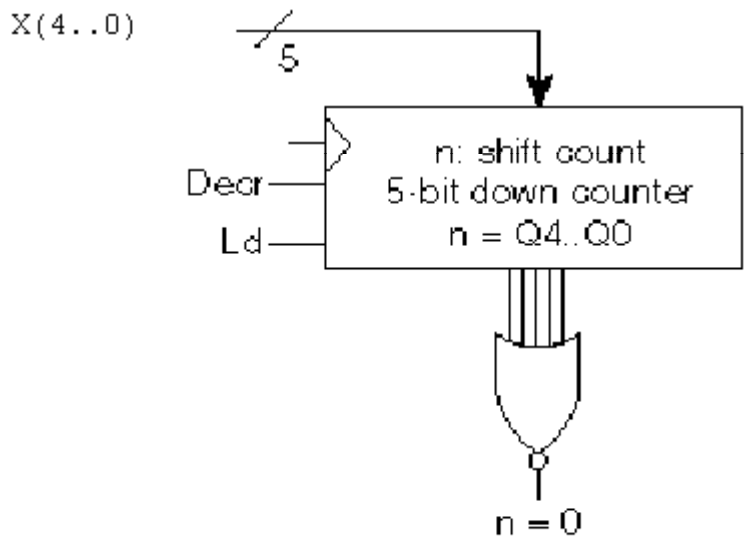

IR⟨2..0⟩
3
Decoder
5 4 3 2 1 0
0
1
x
32
= 0
≠ 0
≥ 0
< 0
⟨31⟩
⟨31..0⟩
CON_in
D Q
CON
Q̄


32
X
To control unit
5
5
D Q
Q
IR(31..27)
5
IR(26..22)
C1<31..22>
10
1
1
C1<21>
IR(21)
c1out
4
4
C1< 20..17>
IR(20..17)
C2<31..17>
15
c2out
1
1
C1<16>
C2<16>
IR(16)
16
16
C1<15..0>
C2<15..0>
IRin
IR(15..0)


32
X
MD_bus
MD_rd
32
32
32
32
D Q
MD
Q
MD⟨31..0⟩
32
MD
Read
Write
Done
32
32
data⟨31..0⟩
MD_wr
Memory
bus
MD_out
X
32
D Q
MA
Q
MA_in
MA⟨31..0⟩
32
addr⟨31..0⟩


X
32
D
Q
32
PC
PC
PCout
PCin
Q̄


31 27 26 22 21 17 16 12 11
IR
Op
ra
rb
rc
5
Gra
Grb
Grc
X
D Q
R31
Q
32
R31
S31
5 to 32 decoder
31
R31
1
R1
0
R0
R1
S1
R0
S0
R_{in}
R_{out}
BA_{out}


X(4..0)
5
Decr
Ld
n: shift count
5-bit down counter
n = Q4..Q0
n = 0