UltraSPARC® III Cu Processor

Design Engineered to Make the Net Work.

Key highlights

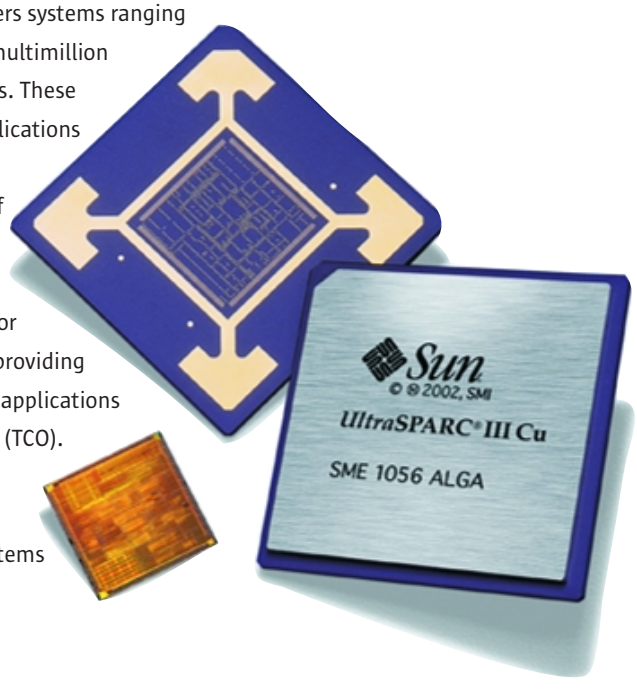
- 64-bit open standards-based SPARC® V9 with VIS™ Instruction Set
- 4-way superscalar
- 14-stage non-stalling pipeline
- Advanced RAS features
- MP scalability: architecturally designed for >1000 CPUs/system
- System bus: Sun™ Fireplane Interconnect
- Processor memory bandwidth scales with number of processors
- Integrated memory controller
- L1 caches: integrated instruction (32 KB) & data (64 KB)
- L2 cache: 8 MB external (2 way, set-associative)
- Clock frequencies: 900 MHz, 1050 MHz and 1.2 GHz

UltraSPARC® III Cu Processor Enables Customer-focused, Real-world Solutions

At Sun, we take great pride in our customer-focused, real-world solutions-based design methodology. The demands of enterprise and high performance computing mandate highly reliable and scalable 64-bit systems to power enterprise applications and next generation web services. Sun's UltraSPARC III Cu processors are the industry-leading, 3rd generation 64-bit microprocessors design engineered to make the Net work.

This award-winning UltraSPARC III Cu processor is Sun's flagship, high-end microprocessor, designed specifically for network computing with key differentiating attributes like RAS, scalability and power efficiency that deliver real-world performance while maintaining binary compatibility.

The key to real-world performance is to focus on customer requirements. UltraSPARC-based systems deliver a deliberate balance of processing power, data bandwidth and network performance because the UltraSPARC processor, software stack including the Solaris™ Operating Environment (OE), and systems are designed together in order to maximize overall performance for real-world applications. Additionally, UltraSPARC III Cu processors offer customers built-in investment protection with attributes supporting mixed speeds in a chassis, thermal and electrical footprint preservation that enable a simple upgrade path, best-in-class power density and extreme uptime (RAS). The UltraSPARC III Cu processor powers systems ranging from high-end workstations to multimillion dollar 106-way enterprise servers. These systems run mission-critical applications from companies such as Oracle, PeopleSoft, Apache, BEA, and, of course, Sun itself.



UltraSPARC III Cu based systems are optimized to meet, or exceed, customer expectations providing high performance on real-world applications and low Total Cost of Ownership (TCO). Through the customer-focused design of UltraSPARC III Cu processors, Sun is delivering systems that drive increased ROI to the customers' bottom line.

UltraSPARC® III Cu Processor Technical Information

UltraSPARC III Cu Processor Features

L1 cache: 64 KB 4-way Data, 32 KB 4-way Instruction, 2 KB Prefetch, 2 KB Write

L2 cache tag RAM and controller on-chip to support 1, 4 or 8 MB external cache

Dedicated 32-bite (256 bit) data path for the L2 cache

Sun Fireplane Interconnect system bus with crossbar control signals

Integrated SDRAM memory controller coupled to the system data bus

Clock frequency control for dynamically dropping frequency for low power modes (1/2 to 1/32 modes)

VIS SIMD Instruction Set

CPU Core Design

14-stage non-stalling pipeline

16 K-entry branch prediction table

New byte mask and shuffle VIS instructions for media applications

Jump target registration instruction to accelerate interpreted code like Java™

Scalable System Performance

4-GB memory subsystem per processor

Processor memory bandwidth scales with number of processors

Instruction Execution Features

Sustainable 4-way Superscalar

Six execution pipelines (2 integer, 2 FP/VIS, 1 load/store, 1 branch)

Multiple outstanding block stores

System Bus Architecture

150 MHz Clock Frequency

Distributed bus arbitration

Fast on-chip snoop tags to maintain system bus performance

Large, wide data crossbar switches

Enhanced Support from Solaris

Multiprocessor (MP) support provided by Solaris OE

System models for tightly coupled, shared memory and for large multi-processor clustered architectures (snoop and directory-based)

Distributed Main Memory

Memory controller on each processor and memory sharing

Industry-leading RAS Features Include:

EDC (Error Detection and Correction) on caches, tags and every external data port to ensure data integrity

Error removal and recovery system to prevent the propagation of copy-back errors

Diagnostic bus to identify system bus errors independent of the main system interface

Physical Characteristics of UltraSPARC III Cu 1.2 GHz

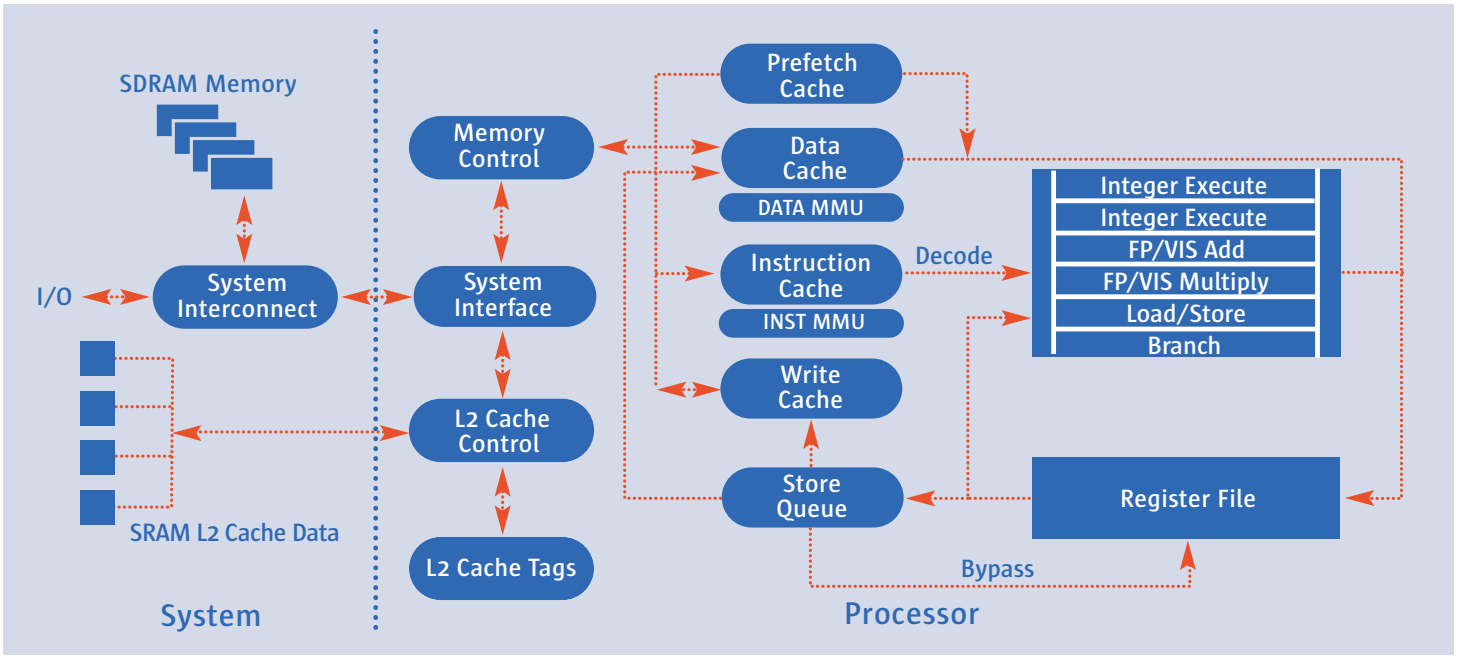
1368 pin flip-chip ceramic Land Grid Array (LGA)

Transistor Count: 29 million

Maximum Power Dissipation: 50 Watts

CMOS process: 0.13 µ, 7-layer copper

Winner of 2001's "Best Workstation/ Server Processor" Award, by *Microprocessor Report*.



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We make the net work.

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