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Release 14.7 par P.20131013 (nt64)
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OPTIPLEX9010::  Tue Sep 23 09:54:09 2014

par -w -intstyle ise -ol high -mt off src_map.ncd src.ncd src.pcf


Constraints file: src.pcf.
Loading device for application Rf_Device from file '6vlx75t.nph' in environment
C:\Xilinx\14.7\ISE_DS\ISE\.
   "src" is an NCD, version 3.2, device xc6vlx75t, package ff484, speed -3
vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv
INFO:Security:50 - The XILINXD_LICENSE_FILE environment variable is set to
'27017@licensing02.seas.wustl.edu'.
INFO:Security:53 - The LM_LICENSE_FILE environment variable is not set.
INFO:Security:54 - 'xc6vlx75t' is a WebPack part.
WARNING:Security:43 - No license file was found in the standard Xilinx license directory.
WARNING:Security:44 - Since no license file was found,
       please run the Xilinx License Configuration Manager
       (xlcm or "Manage Xilinx Licenses")
       to assist in obtaining a license.
WARNING:Security:42 - Your software subscription period has lapsed. Your current version
of Xilinx tools will continue
to function, but you no longer qualify for Xilinx software updates or new releases.

----------------------------------------------------------------------

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)


Device speed data version:  "PRODUCTION 1.17 2013-10-13".



Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers:                1,228 out of  93,120    1%
    Number used as Flip Flops:              1,228
    Number used as Latches:                     0
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:               0
  Number of Slice LUTs:                       906 out of  46,560    1%
    Number used as logic:                     905 out of  46,560    1%
      Number using O6 output only:            858
      Number using O5 output only:              0
      Number using O5 and O6:                  47
      Number used as ROM:                       0
    Number used as Memory:                      0 out of  16,720    0%
    Number used exclusively as route-thrus:     1
      Number with same-slice register load:     1
      Number with same-slice carry load:        0
      Number with other load:                   0

Slice Logic Distribution:
  Number of occupied Slices:                  449 out of  11,640    3%
  Number of LUT Flip Flop pairs used:       1,613
    Number with an unused Flip Flop:          402 out of   1,613   24%
    Number with an unused LUT:                707 out of   1,613   43%
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    Number of fully used LUT-FF pairs:         504 out of   1,613   31%
    Number of slice register sites lost
      to control set restrictions:               0 out of  93,120    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:
  Number of bonded IOBs:                        69 out of     240   28%

Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                  0 out of     156    0%
  Number of RAMB18E1/FIFO18E1s:                  0 out of     312    0%
  Number of BUFG/BUFGCTRLs:                      1 out of      32    3%
    Number used as BUFGs:                        1
    Number used as BUFGCTRLs:                    0
  Number of ILOGICE1/ISERDESE1s:                 0 out of     360    0%
  Number of OLOGICE1/OSERDESE1s:                 0 out of     360    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      72    0%
  Number of BUFIODQSs:                           0 out of      36    0%
  Number of BUFRs:                               0 out of      18    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DSP48E1s:                            0 out of     288    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of GTXE1s:                              0 out of       8    0%
  Number of IBUFDS_GTXE1s:                       0 out of       6    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       9    0%
  Number of IODELAYE1s:                          0 out of     360    0%
  Number of MMCM_ADVs:                           0 out of       6    0%
  Number of PCIE_2_0s:                           0 out of       1    0%
  Number of STARTUPs:                            1 out of       1  100%
  Number of SYSMONs:                             0 out of       1    0%
  Number of TEMAC_SINGLEs:                       0 out of       4    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

INFO:Timing:2802 - Read 100 constraints.  If you are experiencing memory or runtime issues
it may help to consolidate some of these
   constraints.  For more details please do a search for "timing:2802" at
http://www.xilinx.com/support.
Starting initial Timing Analysis.  REAL time: 9 secs
Finished initial Timing Analysis.  REAL time: 9 secs

Starting Router


Phase  1  : 9440 unrouted;      REAL time: 9 secs

Phase  2  : 8813 unrouted;      REAL time: 10 secs

Phase  3  : 1579 unrouted;      REAL time: 12 secs
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Phase  4  : 1965 unrouted; (Setup:211669, Hold:12809, Component Switching Limit:0)
REAL time: 25 secs

Updating file: src.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Setup:507220, Hold:12723, Component Switching Limit:0)     REAL
time: 32 secs

Phase  6  : 0 unrouted; (Setup:458778, Hold:12723, Component Switching Limit:0)     REAL
time: 36 secs

Updating file: src.ncd with current fully routed design.

Phase  7  : 0 unrouted; (Setup:458778, Hold:12723, Component Switching Limit:0)     REAL
time: 42 secs

Phase  8  : 0 unrouted; (Setup:458778, Hold:12723, Component Switching Limit:0)     REAL
time: 42 secs

Phase  9  : 0 unrouted; (Setup:458778, Hold:0, Component Switching Limit:0)     REAL time:
42 secs

Phase 10  : 0 unrouted; (Setup:364561, Hold:0, Component Switching Limit:0)     REAL time:
43 secs
Total REAL time to Router completion: 43 secs
Total CPU time to Router completion: 43 secs

Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.

**************************
Generating Clock Report
**************************

+----------------------+--------------+------+------+------------+-------------+
|        Clock Net     |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+----------------------+--------------+------+------+------------+-------------+
|           clk_BUFGP | BUFGCTRL_X0Y0| No   |  368 |  0.082     |  1.437      |
+----------------------+--------------+------+------+------------+-------------+

* Net Skew is the difference between the minimum and maximum routing
only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.

* The fanout is the number of component pins not the individual BEL loads,
for example SLICE loads not FF loads.

Timing Score: 364561 (Setup: 364561, Hold: 0, Component Switching Limit: 0)

WARNING:Par:468 - Your design did not meet timing.  The following are some suggestions to
assist you to meet timing in your design.

   Review the timing report using Timing Analyzer (In ISE select "Post-Place &
```

   Route Static Timing Report"). Go to the failing constraint(s) and evaluate the failing paths for each constraint.

   Try the Design Goal and Strategies for Timing Performance(In ISE select Project -> Design Goals & Strategies) to ensure the best options
   are set in the tools for timing closure.

   Use the Xilinx "SmartXplorer" script to try special combinations of
   options known to produce very good results.

   Visit the Xilinx technical support web at http://support.xilinx.com and go to
   either "Troubleshoot->Tech Tips->Timing & Constraints" or "
   TechXclusives->Timing Closure" for tips and suggestions for meeting timing
   in your design.

Asterisk (*) preceding a constraint indicates it was not met.
   This may be due to a setup or hold violation.

Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
* COMP "write" OFFSET = OUT 2 ns AFTER COMP "clk"	MAXDELAY	-5.228ns	7.228ns	1	5228
* COMP "read" OFFSET = OUT 2 ns AFTER COMP "clk"	MAXDELAY	-5.211ns	7.211ns	1	5211
* COMP "d<4>" OFFSET = OUT 4 ns AFTER COMP "clk"	MAXDELAY	-4.031ns	8.031ns	1	4031
* COMP "d<5>" OFFSET = OUT 4 ns AFTER COMP "clk"	MAXDELAY	-4.010ns	8.010ns	1	4010
* COMP "d<14>" OFFSET = OUT 4 ns AFTER COMP "clk"	MAXDELAY	-3.456ns	7.456ns	1	3456
* COMP "d<11>" OFFSET = OUT 4 ns AFTER COMP "clk"	MAXDELAY	-3.440ns	7.440ns	1	3440

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* COMP "d<13>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.365ns|
7.365ns|       1|        3365
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<16>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.363ns|
7.363ns|       1|        3363
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<12>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.346ns|
7.346ns|       1|        3346
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<9>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.323ns|
7.323ns|       1|        3323
  "clk"                                    |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<25>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.302ns|
7.302ns|       1|        3302
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<15>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.277ns|
7.277ns|       1|        3277
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<27>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.270ns|
7.270ns|       1|        3270
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<26>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.259ns|
7.259ns|       1|        3259
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<28>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.234ns|
7.234ns|       1|        3234
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "d<19>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.230ns|
7.230ns|       1|        3230
   "clk"                                   |            |            |
|        |
-------------------------------------------------------------------------------------------
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```

```
* COMP "d<8>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.229ns|
7.229ns|       1|        3229
  "clk"                                    |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<22>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.212ns|
7.212ns|       1|        3212
   "clk"                                   |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<0>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.202ns|
7.202ns|       1|        3202
  "clk"                                    |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<3>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.175ns|
7.175ns|       1|        3175
  "clk"                                    |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<6>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.137ns|
7.137ns|       1|        3137
  "clk"                                    |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<7>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.136ns|
7.136ns|       1|        3136
  "clk"                                    |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<31>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.127ns|
7.127ns|       1|        3127
   "clk"                                   |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<21>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.122ns|
7.122ns|       1|        3122
   "clk"                                   |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<18>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.097ns|
7.097ns|       1|        3097
   "clk"                                   |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<10>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.086ns|
7.086ns|       1|        3086
   "clk"                                   |            |            |
|        |
--------------------------------------------------------------------------------
--------------
* COMP "d<2>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.081ns|
```

```
7.081ns|       1|        3081
  "clk"                                    |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<1>" OFFSET = OUT 4 ns AFTER COMP  | MAXDELAY    |    -3.067ns|
7.067ns|       1|        3067
  "clk"                                    |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<17>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.037ns|
7.037ns|       1|        3037
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<30>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.028ns|
7.028ns|       1|        3028
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<23>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.007ns|
7.007ns|       1|        3007
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<24>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -3.005ns|
7.005ns|       1|        3005
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<20>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -2.920ns|
6.920ns|       1|        2920
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "d<29>" OFFSET = OUT 4 ns AFTER COMP | MAXDELAY    |    -2.917ns|
6.917ns|       1|        2917
   "clk"                                   |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "address<19>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.671ns|
5.671ns|       1|        2671
  R COMP "clk"                             |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "address<0>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.648ns|
5.648ns|       1|        2648
   COMP "clk"                              |            |           |
|        |
------------------------------------------------------------------------------------------
--------------
* COMP "address<17>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.634ns|
5.634ns|       1|        2634
```

```
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<11>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.626ns|
5.626ns|       1|        2626
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<9>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.622ns|
5.622ns|       1|        2622
   COMP "clk"                               |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<24>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.614ns|
5.614ns|       1|        2614
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<16>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.612ns|
5.612ns|       1|        2612
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<4>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.612ns|
5.612ns|       1|        2612
   COMP "clk"                               |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<26>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.610ns|
5.610ns|       1|        2610
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<30>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.610ns|
5.610ns|       1|        2610
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<29>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.607ns|
5.607ns|       1|        2607
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<1>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.606ns|
5.606ns|       1|        2606
   COMP "clk"                               |            |            |
|        |
--------------------------------------------------------------------------------------------
--------------
* COMP "address<6>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.605ns|
5.605ns|       1|        2605
   COMP "clk"                               |            |            |
```

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|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<28>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.600ns|
5.600ns|       1|        2600
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<3>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.592ns|
5.592ns|       1|        2592
   COMP "clk"                               |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<31>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.590ns|
5.590ns|       1|        2590
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<10>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.590ns|
5.590ns|       1|        2590
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<25>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.588ns|
5.588ns|       1|        2588
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<5>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.587ns|
5.587ns|       1|        2587
   COMP "clk"                               |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<8>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.586ns|
5.586ns|       1|        2586
   COMP "clk"                               |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<21>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.584ns|
5.584ns|       1|        2584
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<22>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.580ns|
5.580ns|       1|        2580
  R COMP "clk"                              |            |            |
|        |
-------------------------------------------------------------------------------------------
--------------
* COMP "address<7>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.580ns|
5.580ns|       1|        2580
   COMP "clk"                               |            |            |
|        |
```

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--------------------------------------------------------------------------------------------------
--------------
* COMP "address<15>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.575ns|
5.575ns|       1|        2575
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<14>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.563ns|
5.563ns|       1|        2563
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<18>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.562ns|
5.562ns|       1|        2562
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<13>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.546ns|
5.546ns|       1|        2546
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<20>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.545ns|
5.545ns|       1|        2545
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<2>" OFFSET = OUT 3 ns AFTER | MAXDELAY    |    -2.544ns|
5.544ns|       1|        2544
   COMP "clk"                               |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<12>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.544ns|
5.544ns|       1|        2544
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<23>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.543ns|
5.543ns|       1|        2543
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* COMP "address<27>" OFFSET = OUT 3 ns AFTE | MAXDELAY    |    -2.540ns|
5.540ns|       1|        2540
  R COMP "clk"                              |            |            |
|        |
--------------------------------------------------------------------------------------------------
--------------
* TS_CLK = PERIOD TIMEGRP "clk" 5 ns HIGH 5 | SETUP       |    -2.211ns|     7.211ns|
445|      167715
  0%                                        | HOLD        |     0.140ns|
|       0|           0
--------------------------------------------------------------------------------------------------
```

```
--------------
  COMP "d<30>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     1.071ns|
1.929ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     1.999ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<25>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     1.744ns|
1.256ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     1.314ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<23>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     1.955ns|
1.045ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     1.114ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<22>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     1.996ns|
1.004ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     1.066ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<17>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.007ns|
0.993ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.948ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<20>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.032ns|
0.968ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.964ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<29>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.037ns|
0.963ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.994ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<8>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.045ns|
0.955ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.998ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<31>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.058ns|
0.942ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.939ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<28>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.076ns|
0.924ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.935ns|
|       0|           0
--------------------------------------------------------------------------------
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```
  COMP "d<1>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.080ns|
0.920ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.909ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<26>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.081ns|
0.919ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.943ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<19>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.096ns|
0.904ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.934ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "done" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.097ns|
0.903ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.144ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<12>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.110ns|
0.890ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.896ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<15>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.113ns|
0.887ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.899ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<13>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.119ns|
0.881ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.919ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<2>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.128ns|
0.872ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.847ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<21>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.128ns|
0.872ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.875ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<10>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.131ns|
0.869ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.842ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<11>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.140ns|
```

```
0.860ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.853ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<16>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.149ns|
0.851ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.846ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<9>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.181ns|
0.819ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.805ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<14>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.195ns|
0.805ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.861ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<24>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.202ns|
0.798ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.780ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<7>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.205ns|
0.795ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.802ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<18>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.209ns|
0.791ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.791ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<6>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.214ns|
0.786ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.735ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<0>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.267ns|
0.733ns|       0|           0
  EFORE COMP "clk" "RISING"                 | HOLD        |     0.754ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<27>" OFFSET = IN 3 ns VALID 4 ns  | SETUP       |     2.312ns|
0.688ns|       0|           0
  BEFORE COMP "clk" "RISING"                | HOLD        |     0.674ns|
|       0|           0
--------------------------------------------------------------------------------
--------------
  COMP "d<3>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.383ns|
0.617ns|       0|           0
```

```
  EFORE COMP "clk" "RISING"                | HOLD        |     0.678ns|
|       0|           0
--------------------------------------------------------------------------------------------------
--------------
  COMP "d<5>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.575ns|
0.425ns|       0|           0
  EFORE COMP "clk" "RISING"                | HOLD        |     0.411ns|
|       0|           0
--------------------------------------------------------------------------------------------------
--------------
  COMP "d<4>" OFFSET = IN 3 ns VALID 4 ns B | SETUP       |     2.801ns|
0.199ns|       0|           0
  EFORE COMP "clk" "RISING"                | HOLD        |     0.121ns|
|       0|           0
--------------------------------------------------------------------------------------------------
--------------


67 constraints not met.


Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 45 secs
Total CPU time to PAR completion: 44 secs

Peak Memory Usage:  595 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.
Timing: Completed - 511 errors found.

Number of error messages: 0
Number of warning messages: 1
Number of info messages: 1

Writing design to file src.ncd



PAR done!
```