TELMOS INC.

TML1842
VIDEO DAC

Features

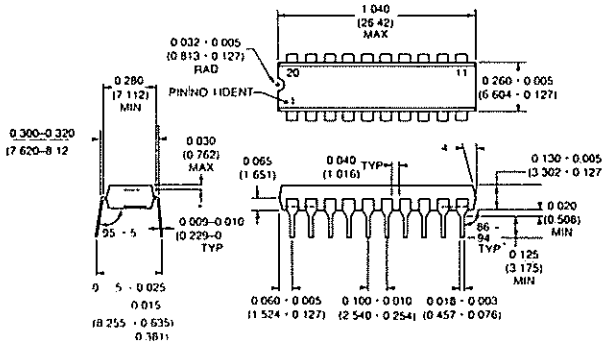
- 8 BIT RESOLUTION
- 40 MSPS TYP. UPDATE RATE
- SINGLE +5V SUPPLY
- TTL/CMOS COMPATIBLE
- LOW GLITCH ENERGY
- ADJUSTABLE CURRENT SOURCE

- CONTROLS FOR COMPOSITE SYNC, COMPOSITE BLANK, 10% BRIGHT
- INDEPENDENT OUTPUT LEVELS FOR COMPOSITE SYNC, COMPOSITE BLANK, 10% BRIGHT
- LOW POWER CMOS (100mW TYP.)
- 20 PIN 0.3" WIDE PACKAGE

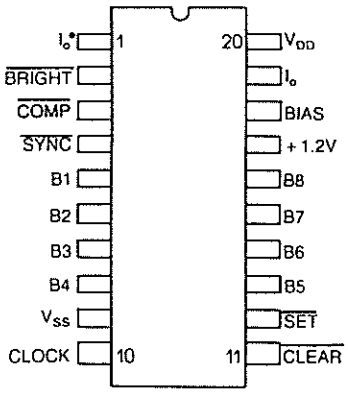
Description

The model TML1842 is a monolithic high speed, 8 bit DAC designed for video applications. The output of this silicon gate CMOS integrated circuit is a current source whose full scale value is set by an external resistor. The TML1842 has composite sync, composite blank, and 10 percent bright signals. It is able to drive 75 ohm or 37.5 ohm loads while operating at a minimum conversion rate of 25MSPS. The input code is straight binary. The TML1842 has a linearity of one bit and only requires a single +5 volt power supply. It will accept either TTL or CMOS inputs.

The TML1842A and TML1842B are indentical to the TML1842 in function with reduced performance. The major differences are: linearity and differential linearity are two and three LSB's (counts) respectively, and the voltage reference specifications are somewhat broader.



Pin Configuration



Ordering Information

COMMERCIAL TEMP. RANGE	TML1842 CCE	TML1842A CCE	TML1842B CCE

Electrical Specifications

Absolute Maximum Ratings:

PARAMETER	RATING	UNITS
Supply voltage (V_{DD})	6	volts
Supply current (I_{DD})	60	mA
Full scale output current (Io)	30	mA
Drive current into any pin	± 10	mA
I_O or I_O' output voltage range	+2.5V to −10V	volts
Logic Input Voltage min.	V_{gnd}−0.3	volts
max.	V_{DD} + 0.3	volts

Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Unless otherwise specified all voltages are referenced to ground.

Operating Conditions

POWER REQUIREMENTS:	Supply Voltage:	+ 5V ± 5%
	Supply Current:	Programmable Nominally 17mA with 75 ohm load
OPERATING TEMP:		
	Commercial	0 deg. C to + 70 deg. C

Electrical Characteristics

V_{DD} = 5V, T_a = 25 deg. C

Typical Load: 37.5 ohms or 75 ohms
Output Drive: Current source (I_O = 6 mA to 20 mA)

PARAMETER	TML 1842	TML 1842A	TML 1842B	UNITS
Max. Output Current (at 1.2V)*	33	33	33	mA
Max. Output Voltage	1.5	1.5	1.5	volts
Resolution	8	8	8	bits
Linearity Error (max)	1	2	3	counts
Diff. Linearity Error (max)	1	2	3	counts
Voltage reference min.	1.13	1.09	1.09	volts
max.	1.33	1.39	1.39	volts
Max. offset current (all current sources off)	1	1	1	uA

*I_O + I_O'

Digital Characteristics

V_{DD} = 5V, T_a = 25 deg. C

PARAMETER	TML 1842	TML 1842A	TML 1842B	Units
Compatibility	TTL, CMOS			
Input Code	Binary			
Sync	40½			IRE units
Brightness	10			IRE units
Blanking	7½			IRE units
Video	92			IRE units
Logic 0 input voltage (max.)	0.8			volts
Logic 1 input voltage (min.)	2.0			volts

Switching Characteristics

V_{DD} = 5V, T_a = 25 deg. C., 75 ohm load, 1 volt full scale output

PARAMETER	TML 1842	TML 1842A	TML 1842B	Units
Minimum conversion Rate	25	25	25	MSPS
Typical conversion Rate	40	40	40	MSPS
Settling Time to 0.2% (Note 1)	20	20	20	ns
Typical Output Transient (glitch) energy	100	100	100	pv-sec
amplitude	20	20	20	mV
Delay Time (Note 2)	30	30	30	ns

Note 1: Typical time from beginning of output current change to final settling at 1/2 LSB.
Note 2: Maximum time from negative edge of clock to beginning of output current change.

Device Operation

The output of the TML 1842 video DAC is a current source whose full scale value is set by an external resistor. This resistor is connected to an internal reference (1.23V nominal), and the current through the resistor represents 6 LSBs of output current. Thus, for a full scale current of 255 LSBs, I_O = 1.23/R x 255/6 = 52/R, where I_O = full scale output current, R = current setting resistor (ohms).

There is a separate pin (I_O') for the composite video signal. The output currents for composite sync, composite blank, and 10% bright are summed and appear at this pin (1). Normally I_O' is connected to pin 19, I_O. The three video signals have the following weighted values:

– Composite sync	112 LSB	(40½ IRE)
– Composite blank	21 LSB	(7½ IRE)
– 10% bright	28 LSB	(10 IRE)

Note that these currents are ratioed to the 8 bit DAC full scale current. (255 LSBs)
The video control pins operate as follows:

COMPOSITE SYNC ($\overline{SYNC}$): A logic "0" shuts off this current source and clears the DAC (00000000).

COMPOSITE BLANK ($\overline{COMP}$): A logic "0" shuts off this current source and clears the DAC (00000000).

10% BRIGHT ($\overline{BRIGHT}$): A logic "0" turns on this current source.

$\overline{SET}$: Sets 8 bit DAC to full scale (11111111). This is an asynchronous control, and it overrides all other controls when it is at a logic "0" level.

$\overline{CLEAR}$: This is a control pin that is synchronized with the clock. If $\overline{CLEAR}$ is pulled low, then the input latches will be set to zero when the clock goes high. When the clock then goes low, the zeros are transferred to the output latches and this sets the DAC output current to zero. This line must be kept low to override data, but $\overline{SET}$ will override $\overline{CLEAR}$.

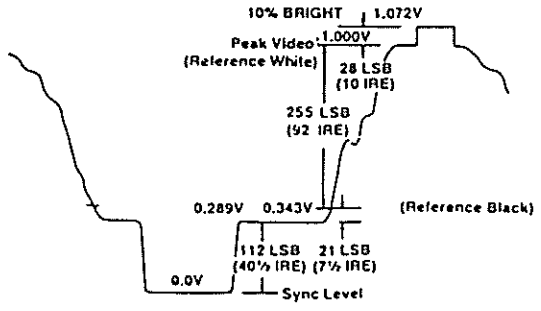


Fig. 1 Composite Video Output

Other pins:

CLOCK: Loads data from B1 through B8 into the input latch while clock is high (Logic 1). Transfers data to output latch on falling edge of clock.

BI-B8: These are the input data lines. B1 is the LSB and B8 is the MSB.

BIAS: Sets the current for the current sources. This line is driven by an internal amplifier. It can also be easily driven by an external source if desired. This line should be bypassed to V_{DD} with a .01uF capacitor.

+ 1.2V: This line is held at a nominal voltage of + 1.23V. A resistor is usually connected from it to ground to set up the full scale current of the DAC.

FIGURE 1 shows the amplitudes of various parts of a video signal. These are expressed in volts, LSBs, and IRE units. Full scale signal (peak video) is nominally + 1.00V which is equivalent to 140 IRE units (by definition). There are 416 current sources in the TML1840, and each represents 1 LSB. The active video is represented by 255 LSBs (8 bit DAC) which also represents 92 IRE units or .657V. The 10% bright signal is an optional feature, and it isn't necessary for normal video. It adds an extra 28 LSBs (10 IRE or 72mV) to the output signal.

A typical video application is shown in Figure 2. The composite video signals have been pre-set to their nominal values. The output load is a 75 ohm resistor. If this connects to a 75 ohm terminated cable, then the actual output load is 37.5 ohms, and, to achieve a 1.0V output, the resistors connected to pin 17 should be half the values shown.

Pin 22 (BIAS) should be bypassed to V_{DD} as shown. V_{DD} should be bypassed to ground.

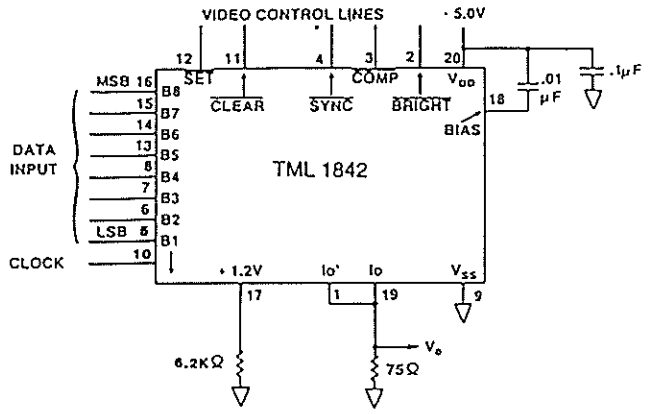


Fig. 2 Typical Video Application

Figure 3 shows the TML 1842 used as an 8 bit DAC in a non-video application. By pulling SYNC and COMP high, BRIGHT low, and leaving I_O' unconnected (floating), the current consumption of the TML1840 is reduced since the composite sync, composite blank, and 10% bright currents are shut off. The output current, I_O, can drive a 50 ohm resistor connected to ground to give a 0 to 1.0V output, or one can tie a 500 ohm resistor to –10V to get a 10V swing. For high voltage outputs, one can add a transistor and resistor. This is shown in Figure 3 as an easy way to get a 100V swing.

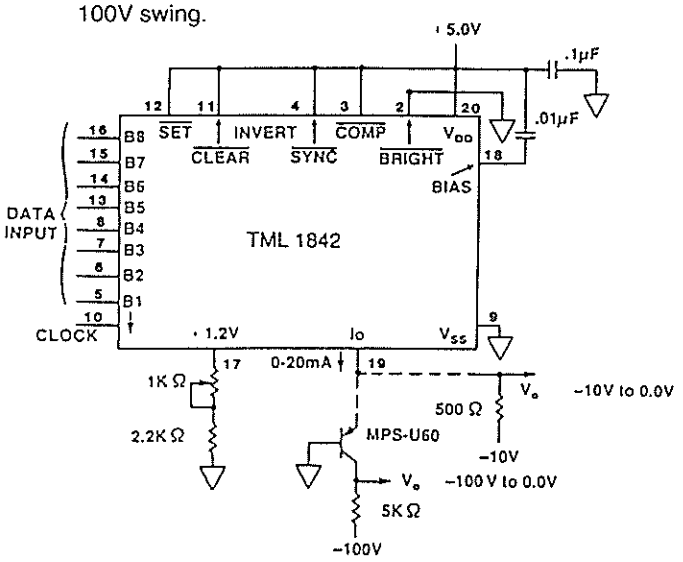
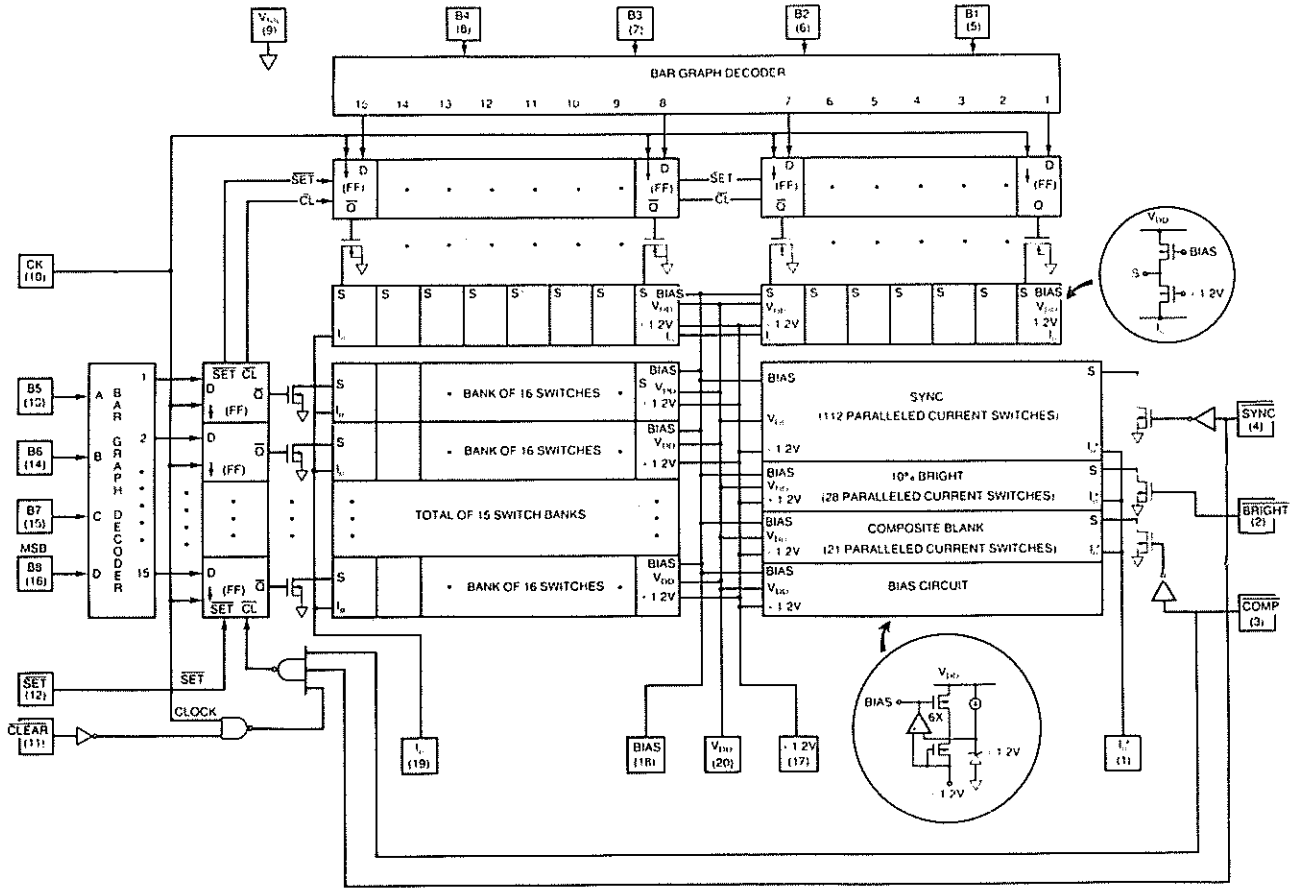


Fig. 3 Non-Video Application (10V or 100V DAC)



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