```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.06 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.06 secs

--> Reading design: src.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "src.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "src"
Output Format                      : NGC
Target Device                      : xc6vlx75t-3-ff484

---- Source Options
Top Module Name                    : src
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
```

```
Resource Sharing                  : YES
Asynchronous To Synchronous       : NO
Shift Register Minimum Size       : 2
Use DSP Block                     : Auto
Automatic Register Balancing      : No

---- Target Options
LUT Combining                     : Auto
Reduce Control Sets               : Auto
Add IO Buffers                    : YES
Global Maximum Fanout             : 100000
Add Generic Clock Buffer(BUFG)    : 32
Register Duplication              : YES
Optimize Instantiated Primitives  : NO
Use Clock Enable                  : Auto
Use Synchronous Set               : Auto
Use Synchronous Reset             : Auto
Pack IO Registers into IOBs       : Auto
Equivalent register Removal       : YES

---- General Options
Optimization Goal                 : Speed
Optimization Effort               : 1
Power Reduction                   : NO
Keep Hierarchy                    : No
Netlist Hierarchy                 : As_Optimized
RTL Output                        : Yes
Global Optimization               : AllClockNets
Read Cores                        : YES
Write Timing Constraints          : NO
Cross Clock Analysis              : NO
Hierarchy Separator               : /
Bus Delimiter                     : <>
Case Specifier                    : Maintain
Slice Utilization Ratio           : 100
BRAM Utilization Ratio            : 100
DSP48 Utilization Ratio           : 100
Auto BRAM Packing                 : NO
Slice Utilization Ratio Delta     : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\shiftcounter.vhd" into
library work
Parsing entity <shiftcounter>.
Parsing architecture <behavioral> of entity <shiftcounter>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\regfile.vhd" into library
work
Parsing entity <regfile>.
Parsing architecture <behavioral> of entity <regfile>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\pc.vhd" into library work
Parsing entity <pc>.
Parsing architecture <behavioral> of entity <pc>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\md.vhd" into library work
Parsing entity <md>.
Parsing architecture <behavioral> of entity <md>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\ma.vhd" into library work
```

```
Parsing entity <ma>.
Parsing architecture <behavioral> of entity <ma>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\ir.vhd" into library work
Parsing entity <ir>.
Parsing architecture <behavioral> of entity <ir>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\control.vhd" into library
work
Parsing entity <control>.
Parsing architecture <behavioral> of entity <control>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\conbit.vhd" into library work
Parsing entity <conbit>.
Parsing architecture <behavioral> of entity <conbit>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\c.vhd" into library work
Parsing entity <c>.
Parsing architecture <behavioral> of entity <c>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\alu.vhd" into library work
Parsing entity <alu>.
Parsing architecture <behavioral> of entity <alu>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\a.vhd" into library work
Parsing entity <a>.
Parsing architecture <behavioral> of entity <a>.
Parsing VHDL file "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\src.vhd" into library work
Parsing entity <src>.
Parsing architecture <structure> of entity <src>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating entity <src> (architecture <structure>) from library <work>.

Elaborating entity <pc> (architecture <behavioral>) from library <work>.

Elaborating entity <a> (architecture <behavioral>) from library <work>.

Elaborating entity <c> (architecture <behavioral>) from library <work>.

Elaborating entity <alu> (architecture <behavioral>) from library <work>.

Elaborating entity <shiftcounter> (architecture <behavioral>) from library <work>.

Elaborating entity <regfile> (architecture <behavioral>) from library <work>.

Elaborating entity <ma> (architecture <behavioral>) from library <work>.

Elaborating entity <md> (architecture <behavioral>) from library <work>.

Elaborating entity <ir> (architecture <behavioral>) from library <work>.

Elaborating entity <conbit> (architecture <behavioral>) from library <work>.

Elaborating entity <control> (architecture <behavioral>) from library <work>.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <src>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\src.vhd".
    Summary:
        no macro.
```

```
Unit <src> synthesized.

Synthesizing Unit <pc>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\pc.vhd".
    Found 32-bit register for signal <pc>.
    Found 1-bit tristate buffer for signal <bus_out<31>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<30>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<29>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<28>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<27>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<26>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<25>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<24>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<23>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<22>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<21>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<20>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<19>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<18>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<17>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<16>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<15>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<14>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<13>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<12>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<11>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<10>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<9>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<8>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<7>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<6>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<5>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<4>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<3>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<2>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<1>> created at line 36
    Found 1-bit tristate buffer for signal <bus_out<0>> created at line 36
    Summary:
        inferred  32 D-type flip-flop(s).
        inferred  32 Tristate(s).
Unit <pc> synthesized.

Synthesizing Unit <a>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\a.vhd".
    Found 32-bit register for signal <a>.
    Summary:
        inferred  32 D-type flip-flop(s).
Unit <a> synthesized.

Synthesizing Unit <c>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\c.vhd".
    Found 32-bit register for signal <c>.
    Found 1-bit tristate buffer for signal <bus_out<31>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<30>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<29>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<28>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<27>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<26>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<25>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<24>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<23>> created at line 32
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    Found 1-bit tristate buffer for signal <bus_out<22>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<21>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<20>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<19>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<18>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<17>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<16>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<15>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<14>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<13>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<12>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<11>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<10>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<9>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<8>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<7>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<6>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<5>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<4>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<3>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<2>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<1>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<0>> created at line 32
    Summary:
        inferred  32 D-type flip-flop(s).
        inferred  32 Tristate(s).
Unit <c> synthesized.

Synthesizing Unit <alu>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\alu.vhd".
    Found 32-bit adder for signal <a[31]_b[31]_add_1_OUT> created at line 38.
    Found 32-bit adder for signal <b[31]_GND_73_o_add_4_OUT> created at line 42.
    Found 32-bit subtractor for signal <GND_73_o_GND_73_o_sub_3_OUT<31:0>> created at line
39.
    Found 32-bit subtractor for signal <GND_73_o_GND_73_o_sub_6_OUT<31:0>> created at line
43.
    Summary:
        inferred   4 Adder/Subtractor(s).
Unit <alu> synthesized.

Synthesizing Unit <shiftcounter>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\shiftcounter.vhd".
    Found 5-bit register for signal <shift_cnt>.
    Found 5-bit subtractor for signal <GND_74_o_GND_74_o_sub_1_OUT<4:0>> created at line 30.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred   5 D-type flip-flop(s).
        inferred   1 Multiplexer(s).
Unit <shiftcounter> synthesized.

Synthesizing Unit <regfile>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\regfile.vhd".
WARNING:Xst:647 - Input <ir<11:0>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <ir<31:27>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
    Found 32-bit register for signal <reg1>.
    Found 32-bit register for signal <reg2>.
    Found 32-bit register for signal <reg3>.
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    Found 32-bit register for signal <reg4>.
    Found 32-bit register for signal <reg5>.
    Found 32-bit register for signal <reg6>.
    Found 32-bit register for signal <reg7>.
    Found 32-bit register for signal <reg8>.
    Found 32-bit register for signal <reg9>.
    Found 32-bit register for signal <reg10>.
    Found 32-bit register for signal <reg11>.
    Found 32-bit register for signal <reg12>.
    Found 32-bit register for signal <reg13>.
    Found 32-bit register for signal <reg14>.
    Found 32-bit register for signal <reg15>.
    Found 32-bit register for signal <reg16>.
    Found 32-bit register for signal <reg17>.
    Found 32-bit register for signal <reg18>.
    Found 32-bit register for signal <reg19>.
    Found 32-bit register for signal <reg20>.
    Found 32-bit register for signal <reg21>.
    Found 32-bit register for signal <reg22>.
    Found 32-bit register for signal <reg23>.
    Found 32-bit register for signal <reg24>.
    Found 32-bit register for signal <reg25>.
    Found 32-bit register for signal <reg26>.
    Found 32-bit register for signal <reg27>.
    Found 32-bit register for signal <reg28>.
    Found 32-bit register for signal <reg29>.
    Found 32-bit register for signal <reg30>.
    Found 32-bit register for signal <reg31>.
    Found 32-bit register for signal <reg0>.
    Found 32-bit 32-to-1 multiplexer for signal <mux_out[4]_reg31[31]_wide_mux_103_OUT>
created at line 129.
    Found 1-bit tristate buffer for signal <bus_out<31>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<30>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<29>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<28>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<27>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<26>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<25>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<24>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<23>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<22>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<21>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<20>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<19>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<18>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<17>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<16>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<15>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<14>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<13>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<12>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<11>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<10>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<9>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<8>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<7>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<6>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<5>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<4>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<3>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<2>> created at line 123
```

```
    Found 1-bit tristate buffer for signal <bus_out<1>> created at line 123
    Found 1-bit tristate buffer for signal <bus_out<0>> created at line 123
    Summary:
        inferred 1024 D-type flip-flop(s).
        inferred  17 Multiplexer(s).
        inferred  32 Tristate(s).
Unit <regfile> synthesized.

Synthesizing Unit <ma>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\ma.vhd".
    Found 32-bit register for signal <address>.
    Summary:
        inferred  32 D-type flip-flop(s).
Unit <ma> synthesized.

Synthesizing Unit <md>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\md.vhd".
    Found 32-bit register for signal <md>.
    Found 1-bit tristate buffer for signal <bus_out<31>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<30>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<29>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<28>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<27>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<26>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<25>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<24>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<23>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<22>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<21>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<20>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<19>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<18>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<17>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<16>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<15>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<14>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<13>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<12>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<11>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<10>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<9>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<8>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<7>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<6>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<5>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<4>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<3>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<2>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<1>> created at line 37
    Found 1-bit tristate buffer for signal <bus_out<0>> created at line 37
    Found 1-bit tristate buffer for signal <d<31>> created at line 46
    Found 1-bit tristate buffer for signal <d<30>> created at line 46
    Found 1-bit tristate buffer for signal <d<29>> created at line 46
    Found 1-bit tristate buffer for signal <d<28>> created at line 46
    Found 1-bit tristate buffer for signal <d<27>> created at line 46
    Found 1-bit tristate buffer for signal <d<26>> created at line 46
    Found 1-bit tristate buffer for signal <d<25>> created at line 46
    Found 1-bit tristate buffer for signal <d<24>> created at line 46
    Found 1-bit tristate buffer for signal <d<23>> created at line 46
    Found 1-bit tristate buffer for signal <d<22>> created at line 46
    Found 1-bit tristate buffer for signal <d<21>> created at line 46
```

```
    Found 1-bit tristate buffer for signal <d<20>> created at line 46
    Found 1-bit tristate buffer for signal <d<19>> created at line 46
    Found 1-bit tristate buffer for signal <d<18>> created at line 46
    Found 1-bit tristate buffer for signal <d<17>> created at line 46
    Found 1-bit tristate buffer for signal <d<16>> created at line 46
    Found 1-bit tristate buffer for signal <d<15>> created at line 46
    Found 1-bit tristate buffer for signal <d<14>> created at line 46
    Found 1-bit tristate buffer for signal <d<13>> created at line 46
    Found 1-bit tristate buffer for signal <d<12>> created at line 46
    Found 1-bit tristate buffer for signal <d<11>> created at line 46
    Found 1-bit tristate buffer for signal <d<10>> created at line 46
    Found 1-bit tristate buffer for signal <d<9>> created at line 46
    Found 1-bit tristate buffer for signal <d<8>> created at line 46
    Found 1-bit tristate buffer for signal <d<7>> created at line 46
    Found 1-bit tristate buffer for signal <d<6>> created at line 46
    Found 1-bit tristate buffer for signal <d<5>> created at line 46
    Found 1-bit tristate buffer for signal <d<4>> created at line 46
    Found 1-bit tristate buffer for signal <d<3>> created at line 46
    Found 1-bit tristate buffer for signal <d<2>> created at line 46
    Found 1-bit tristate buffer for signal <d<1>> created at line 46
    Found 1-bit tristate buffer for signal <d<0>> created at line 46
    Summary:
        inferred  32 D-type flip-flop(s).
        inferred   1 Multiplexer(s).
        inferred  64 Tristate(s).
Unit <md> synthesized.

Synthesizing Unit <ir>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\ir.vhd".
    Found 32-bit register for signal <ir>.
    Found 1-bit tristate buffer for signal <bus_out<31>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<30>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<29>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<28>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<27>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<26>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<25>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<24>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<23>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<22>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<21>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<20>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<19>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<18>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<17>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<16>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<15>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<14>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<13>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<12>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<11>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<10>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<9>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<8>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<7>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<6>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<5>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<4>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<3>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<2>> created at line 32
    Found 1-bit tristate buffer for signal <bus_out<1>> created at line 32
```

```
    Found 1-bit tristate buffer for signal <bus_out<0>> created at line 32
    Summary:
        inferred  32 D-type flip-flop(s).
        inferred   5 Multiplexer(s).
        inferred  32 Tristate(s).
Unit <ir> synthesized.

Synthesizing Unit <conbit>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\conbit.vhd".
WARNING:Xst:647 - Input <ir<31:3>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
    Found 1-bit register for signal <con>.
    Summary:
        inferred   1 D-type flip-flop(s).
        inferred   3 Multiplexer(s).
Unit <conbit> synthesized.

Synthesizing Unit <control>.
    Related source file is "C:\Users\wdr\Documents\VHDL\362\2014SRC\src\control.vhd".
    Found 3-bit register for signal <state>.
    Found finite state machine <FSM_0> for signal <state>.
    -----------------------------------------------------------------------
    | States             | 8                                              |
    | Transitions        | 20                                             |
    | Inputs             | 9                                              |
    | Outputs            | 10                                             |
    | Clock              | clk (rising_edge)                              |
    | Reset              | reset_l_INV_81_o (positive)                    |
    | Reset type         | synchronous                                    |
    | Reset State        | s0                                             |
    | Power Up State     | s0                                             |
    | Encoding           | auto                                           |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
    Found 1-bit 8-to-1 multiplexer for signal <c_in> created at line 197.
    Found 1-bit 7-to-1 multiplexer for signal <c_out> created at line 197.
    Found 1-bit 7-to-1 multiplexer for signal <r_out> created at line 197.
    Found 1-bit 5-to-1 multiplexer for signal <gra> created at line 197.
    Summary:
        inferred 201 Multiplexer(s).
        inferred   1 Finite State Machine(s).
Unit <control> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 5
 32-bit adder                                         : 2
 32-bit subtractor                                    : 2
 5-bit subtractor                                     : 1
# Registers                                            : 40
 1-bit register                                       : 1
 32-bit register                                      : 38
 5-bit register                                       : 1
# Multiplexers                                         : 228
 1-bit 2-to-1 multiplexer                             : 220
 1-bit 5-to-1 multiplexer                             : 1
 1-bit 7-to-1 multiplexer                             : 2
 1-bit 8-to-1 multiplexer                             : 1
```

```
 32-bit 2-to-1 multiplexer                             : 2
 32-bit 32-to-1 multiplexer                            : 1
 5-bit 2-to-1 multiplexer                              : 1
# Tristates                                            : 192
 1-bit tristate buffer                                 : 192
# FSMs                                                 : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


Synthesizing (advanced) Unit <shiftcounter>.
The following registers are absorbed into counter <shift_cnt>: 1 register on signal
<shift_cnt>.
Unit <shiftcounter> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 4
 32-bit adder                                          : 2
 32-bit subtractor                                     : 2
# Counters                                             : 1
 5-bit down counter                                    : 1
# Registers                                            : 1217
 Flip-Flops                                            : 1217
# Multiplexers                                         : 227
 1-bit 2-to-1 multiplexer                              : 220
 1-bit 5-to-1 multiplexer                              : 1
 1-bit 7-to-1 multiplexer                              : 2
 1-bit 8-to-1 multiplexer                              : 1
 32-bit 2-to-1 multiplexer                             : 2
 32-bit 32-to-1 multiplexer                            : 1
# FSMs                                                 : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Analyzing FSM <MFsm> for best encoding.
Optimizing FSM <control1/FSM_0> on signal <state[1:3]> with user encoding.
-------------------
 State | Encoding
-------------------
 s0    | 000
 s1    | 001
 s2    | 010
 s3    | 011
 s4    | 100
 s5    | 101
 s6    | 110
 s7    | 111
-------------------
WARNING:Xst:2040 - Unit src: 32 multi-source signals are replaced by logic (pull-up yes):
cpu_bus<0>, cpu_bus<10>, cpu_bus<11>, cpu_bus<12>, cpu_bus<13>, cpu_bus<14>, cpu_bus<15>,
cpu_bus<16>, cpu_bus<17>, cpu_bus<18>, cpu_bus<19>, cpu_bus<1>, cpu_bus<20>, cpu_bus<21>,
```

cpu_bus<22>, cpu_bus<23>, cpu_bus<24>, cpu_bus<25>, cpu_bus<26>, cpu_bus<27>, cpu_bus<28>,
cpu_bus<29>, cpu_bus<2>, cpu_bus<30>, cpu_bus<31>, cpu_bus<3>, cpu_bus<4>, cpu_bus<5>,
cpu_bus<6>, cpu_bus<7>, cpu_bus<8>, cpu_bus<9>.
WARNING:Xst:2042 - Unit ir: 32 internal tristates are replaced by logic (pull-up yes):
bus_out<0>, bus_out<10>, bus_out<11>, bus_out<12>, bus_out<13>, bus_out<14>, bus_out<15>,
bus_out<16>, bus_out<17>, bus_out<18>, bus_out<19>, bus_out<1>, bus_out<20>, bus_out<21>,
bus_out<22>, bus_out<23>, bus_out<24>, bus_out<25>, bus_out<26>, bus_out<27>, bus_out<28>,
bus_out<29>, bus_out<2>, bus_out<30>, bus_out<31>, bus_out<3>, bus_out<4>, bus_out<5>,
bus_out<6>, bus_out<7>, bus_out<8>, bus_out<9>.
WARNING:Xst:2042 - Unit regfile: 32 internal tristates are replaced by logic (pull-up
yes): bus_out<0>, bus_out<10>, bus_out<11>, bus_out<12>, bus_out<13>, bus_out<14>,
bus_out<15>, bus_out<16>, bus_out<17>, bus_out<18>, bus_out<19>, bus_out<1>, bus_out<20>,
bus_out<21>, bus_out<22>, bus_out<23>, bus_out<24>, bus_out<25>, bus_out<26>, bus_out<27>,
bus_out<28>, bus_out<29>, bus_out<2>, bus_out<30>, bus_out<31>, bus_out<3>, bus_out<4>,
bus_out<5>, bus_out<6>, bus_out<7>, bus_out<8>, bus_out<9>.
WARNING:Xst:2042 - Unit c: 32 internal tristates are replaced by logic (pull-up yes):
bus_out<0>, bus_out<10>, bus_out<11>, bus_out<12>, bus_out<13>, bus_out<14>, bus_out<15>,
bus_out<16>, bus_out<17>, bus_out<18>, bus_out<19>, bus_out<1>, bus_out<20>, bus_out<21>,
bus_out<22>, bus_out<23>, bus_out<24>, bus_out<25>, bus_out<26>, bus_out<27>, bus_out<28>,
bus_out<29>, bus_out<2>, bus_out<30>, bus_out<31>, bus_out<3>, bus_out<4>, bus_out<5>,
bus_out<6>, bus_out<7>, bus_out<8>, bus_out<9>.
WARNING:Xst:2042 - Unit pc: 32 internal tristates are replaced by logic (pull-up yes):
bus_out<0>, bus_out<10>, bus_out<11>, bus_out<12>, bus_out<13>, bus_out<14>, bus_out<15>,
bus_out<16>, bus_out<17>, bus_out<18>, bus_out<19>, bus_out<1>, bus_out<20>, bus_out<21>,
bus_out<22>, bus_out<23>, bus_out<24>, bus_out<25>, bus_out<26>, bus_out<27>, bus_out<28>,
bus_out<29>, bus_out<2>, bus_out<30>, bus_out<31>, bus_out<3>, bus_out<4>, bus_out<5>,
bus_out<6>, bus_out<7>, bus_out<8>, bus_out<9>.

Optimizing unit <a> ...

Optimizing unit <ma> ...

Optimizing unit <src> ...

Optimizing unit <conbit> ...

Optimizing unit <control> ...

Optimizing unit <alu> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block src, actual ratio is 4.
FlipFlop regir/ir_28 has been replicated 1 time(s)
FlipFlop regir/ir_29 has been replicated 1 time(s)
FlipFlop regir/ir_31 has been replicated 1 time(s)

Final Macro Processing ...

===
Final Register Report

Macro Statistics
Registers   : 1228
 Flip-Flops   : 1228

===

===
*   Partition Report   *
===

```
Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : src.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 1237
#      GND                         : 1
#      INV                         : 1
#      LUT2                        : 64
#      LUT3                        : 44
#      LUT4                        : 34
#      LUT5                        : 54
#      LUT6                        : 756
#      MUXCY                       : 122
#      MUXF7                       : 34
#      VCC                         : 1
#      XORCY                       : 126
# FlipFlops/Latches                : 1228
#      FDE                         : 1192
#      FDR                         : 4
#      FDRE                        : 32
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 68
#      IBUF                        : 2
#      IOBUF                       : 32
#      OBUF                        : 34

Device utilization summary:
---------------------------

Selected Device : 6vlx75tff484-3


Slice Logic Utilization:
 Number of Slice Registers:            1228  out of  93120     1%
 Number of Slice LUTs:                  953  out of  46560     2%
    Number used as Logic:               953  out of  46560     2%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   2074
   Number with an unused Flip Flop:     846  out of   2074    40%
   Number with an unused LUT:          1121  out of   2074    54%
   Number of fully used LUT-FF pairs:   107  out of   2074     5%
   Number of unique control sets:        40

IO Utilization:
 Number of IOs:                          69
 Number of bonded IOBs:                  69  out of    240    28%
```

```
Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 1228  |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.560ns (Maximum Frequency: 179.841MHz)
   Minimum input arrival time before clock: 1.344ns
   Maximum output required time after clock: 1.798ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.560ns (frequency: 179.841MHz)
  Total number of paths / destination ports: 6601567 / 2452
-------------------------------------------------------------------------
Delay:               5.560ns (Levels of Logic = 12)
  Source:            control1/state_FSM_FFd3 (FF)
  Destination:       conbit1/con (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: control1/state_FSM_FFd3 to conbit1/con
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             41   0.280   0.541  control1/state_FSM_FFd3
(control1/state_FSM_FFd3)
```

```
     LUT3:I0->O            8   0.053   0.328  control1/Mmux_c_in131
(control1/Mmux_c1_out1136)
     LUT6:I5->O            5   0.053   0.315  control1/Mmux_c1_out151
(control1/Mmux_c1_out15)
     LUT6:I5->O            1   0.053   0.357  regfile1/Mmux_mux_out<0>11_SW0 (N189)
     LUT6:I4->O          288   0.053   0.503  regfile1/Mmux_mux_out<0>11
(regfile1/mux_out<0>)
     LUT6:I4->O            1   0.053   0.481
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_831
(regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_831)
     LUT6:I2->O            1   0.053   0.000
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_9_G (N398)
     MUXF7:I1->O           5   0.187   0.315
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_9
(regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<19>)
     LUT6:I5->O            1   0.053   0.594  cpu_bus<19>LogicTrst_1 (cpu_bus<19>LogicTrst1)
     LUT6:I0->O            1   0.053   0.481  conbit1/GND_207_o_bus_in[31]_equal_5_o2
(conbit1/GND_207_o_bus_in[31]_equal_5_o2)
     LUT5:I1->O            1   0.053   0.296  conbit1/con_glue_set_SW0 (N369)
     LUT6:I5->O            1   0.053   0.296  conbit1/con_rstpot_G (N446)
     LUT3:I2->O            1   0.053   0.000  conbit1/con_rstpot1 (conbit1/con_rstpot)
     FDR:D                    -0.012          conbit1/con
    ----------------------------------------
    Total                      5.560ns (1.050ns logic, 4.510ns route)
                                       (18.9% logic, 81.1% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 76 / 71
--------------------------------------------------------------------------
Offset:              1.344ns (Levels of Logic = 4)
  Source:            done (PAD)
  Destination:       control1/state_FSM_FFd1 (FF)
  Destination Clock: clk rising

  Data Path: done to control1/state_FSM_FFd1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.003   0.615  done_IBUF (done_IBUF)
     LUT6:I1->O            1   0.053   0.000  control1/state_FSM_FFd1-In3_F (N449)
     MUXF7:I0->O           1   0.186   0.433  control1/state_FSM_FFd1-In3
(control1/state_FSM_FFd1-In3)
     LUT6:I3->O            1   0.053   0.000  control1/state_FSM_FFd1-In6
(control1/state_FSM_FFd1-In)
     FDR:D                    -0.012          control1/state_FSM_FFd1
    ----------------------------------------
    Total                      1.344ns (0.295ns logic, 1.049ns route)
                                       (22.0% logic, 78.0% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 338 / 66
--------------------------------------------------------------------------
Offset:              1.798ns (Levels of Logic = 4)
  Source:            control1/state_FSM_FFd1 (FF)
  Destination:       read (PAD)
  Source Clock:      clk rising

  Data Path: control1/state_FSM_FFd1 to read
                              Gate     Net
```

```
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             41   0.280   0.465  control1/state_FSM_FFd1
(control1/state_FSM_FFd1)
     LUT2:I0->O            1   0.053   0.296  control1/Mmux_c1_out181_SW0 (N70)
     LUT6:I5->O            5   0.053   0.315  control1/Mmux_c1_out181
(control1/Mmux_c1_out181)
     LUT4:I3->O            1   0.053   0.279  control1/Mmux_c1_out182 (md_rd)
     OBUF:I->O                 0.003          read_OBUF (read)
    ----------------------------------------
    Total                      1.798ns (0.442ns logic, 1.356ns route)
                                       (24.6% logic, 75.4% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    5.560|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 15.54 secs

-->

Total memory usage is 272716 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    8 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```