```
--------------------------------------------------------------------------------
Release 14.7 Trace  (nt64)
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C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3
-n 3 -fastpaths -xml src.twx src.ncd -o src.twr src.pcf -ucf src.ucf

Design file:              src.ncd
Physical constraint file: src.pcf
Device,package,speed:     xc6vlx75t,ff484,C,-3 (PRODUCTION 1.17 2013-10-13)
Report level:             verbose report

Environment Variable      Effect
--------------------      ------
NONE                      No environment variables were set
--------------------------------------------------------------------------------

INFO:Timing:2802 - Read 100 constraints.  If you are experiencing memory or
   runtime issues it may help to consolidate some of these constraints.  For
   more details please do a search for "timing:2802" at
   http://www.xilinx.com/support.
INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
   option. All paths that are not constrained will be reported in the
   unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.

================================================================================
Timing constraint: TS_CLK = PERIOD TIMEGRP "clk" 5 ns HIGH 50%;
For more information, see Period Analysis in the Timing Closure User Guide (UG612).

 6601565 paths analyzed, 2784 endpoints analyzed, 445 failing endpoints
 445 timing errors detected. (445 setup errors, 0 hold errors, 0 component switching limit
errors)
 Minimum period is   7.211ns.
--------------------------------------------------------------------------------

Paths for end point regc/c_24 (SLICE_X24Y68.A1), 45370 paths
--------------------------------------------------------------------------------
Slack (setup path):     -2.211ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_24 (FF)
  Requirement:          5.000ns
  Data Path Delay:      7.172ns (Levels of Logic = 9)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y70.B3      net (fanout=288)      0.794   regfile1/mux_out<0>
    SLICE_X19Y70.B       Tilo                  0.053
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.C1      net (fanout=1)        0.482
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.AMUX    Tcina                 0.166   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X24Y68.A1      net (fanout=1)        0.897   srcalu/a[31]_b[31]_add_1_OUT<24>
    SLICE_X24Y68.CLK     Tas                   0.012   regc/c<25>
                                                       srcalu/c<24>6
                                                       regc/c_24
    ------------------------------------------------  ---------------------------
    Total                                      7.172ns (1.311ns logic, 5.861ns route)
                                                       (18.3% logic, 81.7% route)

--------------------------------------------------------------------------------
Slack (setup path):     -2.143ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_24 (FF)
  Requirement:          5.000ns
  Data Path Delay:      7.104ns (Levels of Logic = 9)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X17Y69.C4      net (fanout=288)      0.740   regfile1/mux_out<0>
    SLICE_X17Y69.C       Tilo                  0.053   regfile1/reg15<27>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.D1      net (fanout=1)        0.472
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.CMUX    Topdc                 0.269
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_F

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.AMUX    Tcina                 0.166   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X24Y68.A1      net (fanout=1)        0.897   srcalu/a[31]_b[31]_add_1_OUT<24>
    SLICE_X24Y68.CLK     Tas                   0.012   regc/c<25>
                                                       srcalu/c<24>6
                                                       regc/c_24
    -------------------------------------------------  ---------------------------
    Total                                      7.104ns (1.307ns logic, 5.797ns route)
                                                       (18.4% logic, 81.6% route)

--------------------------------------------------------------------------------
Slack (setup path):     -2.127ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_24 (FF)
  Requirement:          5.000ns
  Data Path Delay:      7.088ns (Levels of Logic = 9)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y71.B6      net (fanout=288)      0.708   regfile1/mux_out<0>
    SLICE_X19Y71.B       Tilo                  0.053   regfile1/reg26<23>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
    SLICE_X19Y70.C2      net (fanout=1)        0.484
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.AMUX    Tcina                 0.166   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X24Y68.A1      net (fanout=1)        0.897   srcalu/a[31]_b[31]_add_1_OUT<24>
    SLICE_X24Y68.CLK     Tas                   0.012   regc/c<25>
                                                       srcalu/c<24>6
                                                       regc/c_24
    -------------------------------------------------  ---------------------------
    Total                                      7.088ns (1.311ns logic, 5.777ns route)
                                                       (18.5% logic, 81.5% route)

--------------------------------------------------------------------------------
```

```
Paths for end point regc/c_29 (SLICE_X24Y69.C3), 54370 paths
--------------------------------------------------------------------------------
Slack (setup path):     -1.937ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_29 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.900ns (Levels of Logic = 10)
  Clock Path Skew:      -0.002ns (0.078 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y70.B3      net (fanout=288)      0.794   regfile1/mux_out<0>
    SLICE_X19Y70.B       Tilo                  0.053
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.C1      net (fanout=1)        0.482
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>
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srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.BMUX    Tcinb                 0.210   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X24Y69.C3      net (fanout=1)        0.521   srcalu/a[31]_b[31]_add_1_OUT<29>
    SLICE_X24Y69.CLK     Tas                   0.012   regc/c<29>
                                                       srcalu/c<29>6
                                                       regc/c_29
    ------------------------------------------------  ---------------------------
    Total                                      6.900ns (1.415ns logic, 5.485ns route)
                                                       (20.5% logic, 79.5% route)

--------------------------------------------------------------------------------
Slack (setup path):     -1.869ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_29 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.832ns (Levels of Logic = 10)
  Clock Path Skew:      -0.002ns (0.078 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X17Y69.C4      net (fanout=288)      0.740   regfile1/mux_out<0>
    SLICE_X17Y69.C       Tilo                  0.053   regfile1/reg15<27>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.D1      net (fanout=1)        0.472
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.CMUX    Topdc                 0.269
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_F

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
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```
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.BMUX    Tcinb                 0.210   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X24Y69.C3      net (fanout=1)        0.521   srcalu/a[31]_b[31]_add_1_OUT<29>
    SLICE_X24Y69.CLK     Tas                   0.012   regc/c<29>
                                                       srcalu/c<29>6
                                                       regc/c_29
    -------------------------------------------------  ---------------------------
    Total                                      6.832ns (1.411ns logic, 5.421ns route)
                                                       (20.7% logic, 79.3% route)

--------------------------------------------------------------------------------
Slack (setup path):     -1.853ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_29 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.816ns (Levels of Logic = 10)
  Clock Path Skew:      -0.002ns (0.078 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y71.B6      net (fanout=288)      0.708   regfile1/mux_out<0>
    SLICE_X19Y71.B       Tilo                  0.053   regfile1/reg26<23>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
```

```
    SLICE_X19Y70.C2      net (fanout=1)        0.484
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.BMUX    Tcinb                 0.210   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X24Y69.C3      net (fanout=1)        0.521   srcalu/a[31]_b[31]_add_1_OUT<29>
    SLICE_X24Y69.CLK     Tas                   0.012   regc/c<29>
                                                       srcalu/c<29>6
                                                       regc/c_29
    -------------------------------------------------  ---------------------------
    Total                                      6.816ns (1.415ns logic, 5.401ns route)
                                                       (20.8% logic, 79.2% route)

--------------------------------------------------------------------------------

Paths for end point regc/c_31 (SLICE_X25Y68.C4), 57970 paths
--------------------------------------------------------------------------------
Slack (setup path):     -1.913ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_31 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.874ns (Levels of Logic = 10)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
```

```
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y70.B3      net (fanout=288)      0.794   regfile1/mux_out<0>
    SLICE_X19Y70.B       Tilo                  0.053
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.C1      net (fanout=1)        0.482
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.DMUX    Tcind                 0.239   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X25Y68.C4      net (fanout=1)        0.431   srcalu/a[31]_b[31]_add_1_OUT<31>
    SLICE_X25Y68.CLK     Tas                   0.047   regc/c<31>
                                                       srcalu/c<31>6
                                                       regc/c_31
    -------------------------------------------------  ---------------------------
    Total                                      6.874ns (1.479ns logic, 5.395ns route)
                                                       (21.5% logic, 78.5% route)

--------------------------------------------------------------------------------
Slack (setup path):     -1.845ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_31 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.806ns (Levels of Logic = 10)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X17Y69.C4      net (fanout=288)      0.740   regfile1/mux_out<0>
    SLICE_X17Y69.C       Tilo                  0.053   regfile1/reg15<27>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.D1      net (fanout=1)        0.472
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_941
    SLICE_X19Y70.CMUX    Topdc                 0.269
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_F

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.DMUX    Tcind                 0.239   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X25Y68.C4      net (fanout=1)        0.431   srcalu/a[31]_b[31]_add_1_OUT<31>
    SLICE_X25Y68.CLK     Tas                   0.047   regc/c<31>
                                                       srcalu/c<31>6
                                                       regc/c_31
    -------------------------------------------------  ---------------------------
    Total                                      6.806ns (1.475ns logic, 5.331ns route)
                                                       (21.7% logic, 78.3% route)
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -1.829ns (requirement - (data path - clock path skew + uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          regc/c_31 (FF)
  Requirement:          5.000ns
  Data Path Delay:      6.790ns (Levels of Logic = 10)
  Clock Path Skew:      -0.004ns (0.076 - 0.080)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: regir/ir_29 to regc/c_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X26Y62.D4      net (fanout=40)       0.632   regir/ir<29>
    SLICE_X26Y62.D       Tilo                  0.053   regfile1/reg10<31>
                                                       control1/Mmux_c1_out15211
    SLICE_X25Y61.A4      net (fanout=13)       0.782   control1/Mmux_c1_out11
    SLICE_X25Y61.A       Tilo                  0.053   regir/ir_29_1
                                                       regfile1/Mmux_mux_out<0>11_SW0
    SLICE_X19Y61.A4      net (fanout=1)        0.518   N189
    SLICE_X19Y61.A       Tilo                  0.053   regir/ir<25>
                                                       regfile1/Mmux_mux_out<0>11
    SLICE_X19Y71.B6      net (fanout=288)      0.708   regfile1/mux_out<0>
    SLICE_X19Y71.B       Tilo                  0.053   regfile1/reg26<23>

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
    SLICE_X19Y70.C2      net (fanout=1)        0.484
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_839
    SLICE_X19Y70.CMUX    Tilo                  0.273
regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_713

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12_G

regfile1/Mmux_mux_out[4]_reg31[31]_wide_mux_103_OUT_2_f7_12
    SLICE_X23Y72.B6      net (fanout=5)        0.401
regfile1/mux_out[4]_reg31[31]_wide_mux_103_OUT<21>
    SLICE_X23Y72.B       Tilo                  0.053   regfile1/reg23<23>
                                                       cpu_bus<21>LogicTrst
    SLICE_X22Y66.B1      net (fanout=41)       1.355   cpu_bus<21>
    SLICE_X22Y66.COUT    Topcyb                0.312   regfile1/reg2<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_lut<21>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.CIN     net (fanout=1)        0.000
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<23>
    SLICE_X22Y67.COUT    Tbyp                  0.060   regfile1/reg5<19>

srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.CIN     net (fanout=1)        0.000
```

```
srcalu/Madd_a[31]_b[31]_add_1_OUT_cy<27>
    SLICE_X22Y68.DMUX    Tcind                0.239   regpc/pc<22>

srcalu/Madd_a[31]_b[31]_add_1_OUT_xor<31>
    SLICE_X25Y68.C4      net (fanout=1)       0.431   srcalu/a[31]_b[31]_add_1_OUT<31>
    SLICE_X25Y68.CLK     Tas                  0.047   regc/c<31>
                                                      srcalu/c<31>6
                                                      regc/c_31
    ------------------------------------------------  ---------------------------
    Total                                     6.790ns (1.479ns logic, 5.311ns route)
                                                      (21.8% logic, 78.2% route)

--------------------------------------------------------------------------------

Hold Paths: TS_CLK = PERIOD TIMEGRP "clk" 5 ns HIGH 50%;
--------------------------------------------------------------------------------

Paths for end point regpc/pc_11 (SLICE_X23Y59.B4), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.140ns (requirement - (clock path skew + uncertainty - data path))
  Source:               regpc/pc_11 (FF)
  Destination:          regpc/pc_11 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.140ns (Levels of Logic = 1)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_BUFGP rising at 5.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path at Fast Process Corner: regpc/pc_11 to regpc/pc_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X23Y59.BQ      Tcko                  0.098   regpc/pc<13>
                                                       regpc/pc_11
    SLICE_X23Y59.B4      net (fanout=4)        0.099   regpc/pc<11>
    SLICE_X23Y59.CLK     Tah         (-Th)     0.057   regpc/pc<13>
                                                       cpu_bus<11>LogicTrst
                                                       regpc/pc_11
    -------------------------------------------------  ---------------------------
    Total                                      0.140ns (0.041ns logic, 0.099ns route)
                                                       (29.3% logic, 70.7% route)

--------------------------------------------------------------------------------

Paths for end point shiftcounter1/shift_cnt_4 (SLICE_X26Y57.A3), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.146ns (requirement - (clock path skew + uncertainty - data path))
  Source:               shiftcounter1/shift_cnt_2 (FF)
  Destination:          shiftcounter1/shift_cnt_4 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.155ns (Levels of Logic = 1)
  Clock Path Skew:      0.009ns (0.053 - 0.044)
  Source Clock:         clk_BUFGP rising at 5.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path at Fast Process Corner: shiftcounter1/shift_cnt_2 to
shiftcounter1/shift_cnt_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    SLICE_X27Y57.CQ      Tcko                  0.098   shiftcounter1/shift_cnt<3>
                                                       shiftcounter1/shift_cnt_2
    SLICE_X26Y57.A3      net (fanout=4)        0.133   shiftcounter1/shift_cnt<2>
    SLICE_X26Y57.CLK     Tah         (-Th)     0.076   shiftcounter1/shift_cnt<1>

shiftcounter1/Mcount_shift_cnt_xor<4>1
                                                       shiftcounter1/shift_cnt_4
    ------------------------------------------------  --------------------------
    Total                                      0.155ns (0.022ns logic, 0.133ns route)
                                                       (14.2% logic, 85.8% route)

--------------------------------------------------------------------------------

Paths for end point shiftcounter1/shift_cnt_1 (SLICE_X26Y57.D4), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.146ns (requirement - (clock path skew + uncertainty - data path))
  Source:               shiftcounter1/shift_cnt_1 (FF)
  Destination:          shiftcounter1/shift_cnt_1 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.146ns (Levels of Logic = 1)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_BUFGP rising at 5.000ns
  Destination Clock:    clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path at Fast Process Corner: shiftcounter1/shift_cnt_1 to
shiftcounter1/shift_cnt_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  ------------------
    SLICE_X26Y57.DQ      Tcko                  0.115   shiftcounter1/shift_cnt<1>
                                                       shiftcounter1/shift_cnt_1
    SLICE_X26Y57.D4      net (fanout=4)        0.108   shiftcounter1/shift_cnt<1>
    SLICE_X26Y57.CLK     Tah         (-Th)     0.077   shiftcounter1/shift_cnt<1>

shiftcounter1/Mcount_shift_cnt_xor<1>11
                                                       shiftcounter1/shift_cnt_1
    ------------------------------------------------  --------------------------
    Total                                      0.146ns (0.038ns logic, 0.108ns route)
                                                       (26.0% logic, 74.0% route)

--------------------------------------------------------------------------------

Component Switching Limit Checks: TS_CLK = PERIOD TIMEGRP "clk" 5 ns HIGH 50%;
--------------------------------------------------------------------------------
Slack: 3.750ns (period - min period limit)
  Period: 5.000ns
  Min period limit: 1.250ns (800.000MHz) (Tbcper_I)
  Physical resource: clk_BUFGP/BUFG/I0
  Logical resource: clk_BUFGP/BUFG/I0
  Location pin: BUFGCTRL_X0Y0.I0
  Clock network: clk_BUFGP/IBUFG
--------------------------------------------------------------------------------
Slack: 4.272ns (period - (min low pulse limit / (low pulse / period)))
  Period: 5.000ns
  Low pulse: 2.500ns
  Low pulse limit: 0.364ns (Tcl)
  Physical resource: regma/address<30>/CLK
  Logical resource: regma/address_30/CK
  Location pin: SLICE_X0Y43.CLK
```

```
  Clock network: clk_BUFGP
--------------------------------------------------------------------------------
Slack: 4.272ns (period - (min high pulse limit / (high pulse / period)))
  Period: 5.000ns
  High pulse: 2.500ns
  High pulse limit: 0.364ns (Tch)
  Physical resource: regma/address<30>/CLK
  Logical resource: regma/address_30/CK
  Location pin: SLICE_X0Y43.CLK
  Clock network: clk_BUFGP
--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<31>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.127ns.
--------------------------------------------------------------------------------

Paths for end point d<31> (A17.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.127ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.625ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
```

```
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A17.T                net (fanout=32)       1.150   regmd/md_wr_inv
    A17.PAD              Tiotp                 1.869   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    ------------------------------------------------  ---------------------------
    Total                                      4.625ns (2.258ns logic, 2.367ns route)
                                                       (48.8% logic, 51.2% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.083ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.576ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A17.T                net (fanout=32)       1.150   regmd/md_wr_inv
    A17.PAD              Tiotp                 1.869   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    ------------------------------------------------  ---------------------------
    Total                                      4.576ns (2.205ns logic, 2.371ns route)
                                                       (48.2% logic, 51.8% route)
```

```
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.981ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.479ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A17.T                net (fanout=32)       1.150   regmd/md_wr_inv
    A17.PAD              Tiotp                 1.869   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    -------------------------------------------------  ---------------------------
    Total                                      4.479ns (2.221ns logic, 2.258ns route)
                                                       (49.6% logic, 50.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<31>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<31> (A17.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.498ns (clock arrival + clock path + data path - uncertainty)
```

```
  Source:               regir/ir_30 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.383ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A17.T                net (fanout=32)       0.557   regmd/md_wr_inv
    A17.PAD              Tiotp                 1.157   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    -------------------------------------------------  ---------------------------
    Total                                      2.383ns (1.289ns logic, 1.094ns route)
                                                       (54.1% logic, 45.9% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.491ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.378ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A17.T                net (fanout=32)       0.557   regmd/md_wr_inv
    A17.PAD              Tiotp                 1.157   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    -------------------------------------------------  ---------------------------
    Total                                      2.378ns (1.306ns logic, 1.072ns route)
                                                       (54.9% logic, 45.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.980ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_31 (FF)
  Destination:          d<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.847ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y65.CLK     net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)
```

```
  Minimum Data Path at Fast Process Corner: regmd/md_31 to d<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y65.CMUX    Tshcko                0.128   regmd/md<30>
                                                       regmd/md_31
    A17.O                net (fanout=2)        0.562   regmd/md<31>
    A17.PAD              Tioop                 1.157   d<31>
                                                       d_31_IOBUF/OBUFT
                                                       d<31>
    -------------------------------------------------  ---------------------------
    Total                                      1.847ns (1.285ns logic, 0.562ns route)
                                                       (69.6% logic, 30.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<31>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.942ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_31 (SLICE_X35Y65.C2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.058ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<31> (PAD)
  Destination:          regmd/md_31 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.075ns (Levels of Logic = 2)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<31> to regmd/md_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A17.I                Tiopi                 0.402   d<31>
                                                       d<31>
                                                       d_31_IOBUF/IBUF
    SLICE_X35Y65.C2      net (fanout=1)        1.650   N89
    SLICE_X35Y65.CLK     Tas                   0.023   regmd/md<30>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT251
                                                       regmd/md_31
    -------------------------------------------------  ---------------------------
    Total                                      2.075ns (0.425ns logic, 1.650ns route)
                                                       (20.5% logic, 79.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_31
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y65.CLK     net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<31>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_31 (SLICE_X35Y65.C2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.939ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<31> (PAD)
  Destination:          regmd/md_31 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.478ns (Levels of Logic = 2)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<31> to regmd/md_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A17.I                Tiopi                 0.547   d<31>
                                                       d<31>
                                                       d_31_IOBUF/IBUF
    SLICE_X35Y65.C2      net (fanout=1)        2.041   N89
    SLICE_X35Y65.CLK     Tah         (-Th)     0.110   regmd/md<30>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT251
                                                       regmd/md_31
    -------------------------------------------------  ---------------------------
    Total                                      2.478ns (0.437ns logic, 2.041ns route)
                                                       (17.6% logic, 82.4% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y65.CLK     net (fanout=368)      1.412   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<30>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.028ns.
--------------------------------------------------------------------------------

Paths for end point d<30> (E12.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.028ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.526ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
```

```
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E12.T                net (fanout=32)       1.086   regmd/md_wr_inv
    E12.PAD              Tiotp                 1.834   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    ------------------------------------------------  ---------------------------
    Total                                      4.526ns (2.223ns logic, 2.303ns route)
                                                       (49.1% logic, 50.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.984ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.477ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E12.T                net (fanout=32)       1.086   regmd/md_wr_inv
    E12.PAD              Tiotp                 1.834   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    ------------------------------------------------  ---------------------------
    Total                                      4.477ns (2.170ns logic, 2.307ns route)
                                                       (48.5% logic, 51.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.882ns (requirement - (clock arrival + clock path + data path +
```

```
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.380ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E12.T                net (fanout=32)       1.086   regmd/md_wr_inv
    E12.PAD              Tiotp                 1.834   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    -------------------------------------------------  ---------------------------
    Total                                      4.380ns (2.186ns logic, 2.194ns route)
                                                       (49.9% logic, 50.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<30>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<30> (E12.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.436ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
```

```
  Data Path Delay:      2.321ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E12.T                net (fanout=32)       0.525   regmd/md_wr_inv
    E12.PAD              Tiotp                 1.127   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    -------------------------------------------------  ---------------------------
    Total                                      2.321ns (1.259ns logic, 1.062ns route)
                                                       (54.2% logic, 45.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.429ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.316ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E12.T                net (fanout=32)       0.525   regmd/md_wr_inv
    E12.PAD              Tiotp                 1.127   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    -------------------------------------------------  ---------------------------
    Total                                      2.316ns (1.276ns logic, 1.040ns route)
                                                       (55.1% logic, 44.9% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.962ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_30 (FF)
  Destination:          d<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.829ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y65.CLK     net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_30 to d<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    SLICE_X35Y65.CQ      Tcko                  0.098   regmd/md<30>
                                                       regmd/md_30
    E12.O                net (fanout=2)        0.604   regmd/md<30>
    E12.PAD              Tioop                 1.127   d<30>
                                                       d_30_IOBUF/OBUFT
                                                       d<30>
    ------------------------------------------------  --------------------------
    Total                                      1.829ns (1.225ns logic, 0.604ns route)
                                                       (67.0% logic, 33.0% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<30>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   1.929ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_30 (SLICE_X35Y65.C1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     1.071ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<30> (PAD)
  Destination:          regmd/md_30 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      4.143ns (Levels of Logic = 2)
  Clock Path Delay:     2.239ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: d<30> to regmd/md_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E12.I                Tiopi                 0.543   d<30>
                                                       d<30>
                                                       d_30_IOBUF/IBUF
    SLICE_X35Y65.C1      net (fanout=1)        3.553   N90
    SLICE_X35Y65.CLK     Tas                   0.047   regmd/md<30>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT241
                                                       regmd/md_30
    -------------------------------------------------  --------------------------
    Total                                      4.143ns (0.590ns logic, 3.553ns route)
                                                       (14.2% logic, 85.8% route)

  Minimum Clock Path at Slow Process Corner: clk to regmd/md_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    D12.I               Tiopi                 0.525   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0    net (fanout=1)        0.438   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O     Tbgcko_O              0.066   clk_BUFGP/BUFG
                                                      clk_BUFGP/BUFG
    SLICE_X35Y65.CLK    net (fanout=368)      1.210   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                     2.239ns (0.591ns logic, 1.648ns route)
                                                      (26.4% logic, 73.6% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<30>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_30 (SLICE_X35Y65.C1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      1.999ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<30> (PAD)
  Destination:          regmd/md_30 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      3.538ns (Levels of Logic = 2)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<30> to regmd/md_30
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    E12.I               Tiopi                 0.517   d<30>
                                                      d<30>
                                                      d_30_IOBUF/IBUF
    SLICE_X35Y65.C1     net (fanout=1)        3.096   N90
    SLICE_X35Y65.CLK    Tah         (-Th)     0.075   regmd/md<30>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT241
                                                      regmd/md_30
    ------------------------------------------------  ---------------------------
    Total                                     3.538ns (0.442ns logic, 3.096ns route)
                                                      (12.5% logic, 87.5% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_30
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I               Tiopi                 0.552   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0    net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O     Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                      clk_BUFGP/BUFG
    SLICE_X35Y65.CLK    net (fanout=368)      1.412   clk_BUFGP
```

```
    ----------------------------------------------------  ---------------------------
    Total                                          2.514ns (0.622ns logic, 1.892ns route)
                                                           (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<29>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   6.917ns.
--------------------------------------------------------------------------------

Paths for end point d<29> (D13.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.917ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.415ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D13.T                net (fanout=32)       0.975   regmd/md_wr_inv
```

```
    D13.PAD             Tiotp                 1.834   d<29>
                                                      d_29_IOBUF/OBUFT
                                                      d<29>
    ------------------------------------------------  --------------------------
    Total                                     4.415ns (2.223ns logic, 2.192ns route)
                                                      (50.4% logic, 49.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.873ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.366ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D13.T                net (fanout=32)       0.975   regmd/md_wr_inv
    D13.PAD              Tiotp                 1.834   d<29>
                                                       d_29_IOBUF/OBUFT
                                                       d<29>
    -------------------------------------------------  ---------------------------
    Total                                      4.366ns (2.170ns logic, 2.196ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.771ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<29> (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.269ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D13.T                net (fanout=32)       0.975   regmd/md_wr_inv
    D13.PAD              Tiotp                 1.834   d<29>
                                                       d_29_IOBUF/OBUFT
                                                       d<29>
    -------------------------------------------------  ---------------------------
    Total                                      4.269ns (2.186ns logic, 2.083ns route)
                                                       (51.2% logic, 48.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<29>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<29> (D13.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.375ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.260ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D13.T                net (fanout=32)       0.464   regmd/md_wr_inv
    D13.PAD              Tiotp                 1.127   d<29>
                                                       d_29_IOBUF/OBUFT
                                                       d<29>
    -------------------------------------------------  ---------------------------
    Total                                      2.260ns (1.259ns logic, 1.001ns route)
                                                       (55.7% logic, 44.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.368ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.255ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D13.T                net (fanout=32)       0.464   regmd/md_wr_inv
    D13.PAD              Tiotp                 1.127   d<29>
                                                       d_29_IOBUF/OBUFT
                                                       d<29>
    ------------------------------------------------  ---------------------------
    Total                                      2.255ns (1.276ns logic, 0.979ns route)
                                                       (56.6% logic, 43.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.010ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_29 (FF)
  Destination:          d<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.881ns (Levels of Logic = 1)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      0.570   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regmd/md_29 to d<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y58.CQ      Tcko                  0.098   regmd/md<29>
                                                       regmd/md_29
```

```
    D13.O               net (fanout=2)        0.656   regmd/md<29>
    D13.PAD             Tioop                 1.127   d<29>
                                                      d_29_IOBUF/OBUFT
                                                      d<29>
    ------------------------------------------------  ---------------------------
    Total                                     1.881ns (1.225ns logic, 0.656ns route)
                                                      (65.1% logic, 34.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<29>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.963ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_29 (SLICE_X35Y58.C1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.037ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<29> (PAD)
  Destination:          regmd/md_29 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.092ns (Levels of Logic = 2)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<29> to regmd/md_29
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D13.I               Tiopi                 0.367   d<29>
                                                      d<29>
                                                      d_29_IOBUF/IBUF
    SLICE_X35Y58.C1     net (fanout=1)        1.695   N91
    SLICE_X35Y58.CLK    Tas                   0.030   regmd/md<29>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT221
                                                      regmd/md_29
    ------------------------------------------------  ---------------------------
    Total                                     2.092ns (0.397ns logic, 1.695ns route)
                                                      (19.0% logic, 81.0% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_29
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I               Tiopi                 0.320   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      0.570   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<29>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_29 (SLICE_X35Y58.C1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.994ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<29> (PAD)
  Destination:          regmd/md_29 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.525ns (Levels of Logic = 2)
  Clock Path Delay:     2.506ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<29> to regmd/md_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D13.I                Tiopi                 0.517   d<29>
                                                       d<29>
                                                       d_29_IOBUF/IBUF
    SLICE_X35Y58.C1      net (fanout=1)        2.083   N91
    SLICE_X35Y58.CLK     Tah         (-Th)     0.075   regmd/md<29>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT221
                                                       regmd/md_29
    -------------------------------------------------  ---------------------------
    Total                                      2.525ns (0.442ns logic, 2.083ns route)
                                                       (17.5% logic, 82.5% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      1.404   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.506ns (0.622ns logic, 1.884ns route)
                                                       (24.8% logic, 75.2% route)
```

```
--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<28>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.234ns.
--------------------------------------------------------------------------------

Paths for end point d<28> (A13.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.234ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.732ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A13.T                net (fanout=32)       1.268   regmd/md_wr_inv
    A13.PAD              Tiotp                 1.858   d<28>
                                                       d_28_IOBUF/OBUFT
                                                       d<28>
```

```
    ----------------------------------------------------  -------------------------
    Total                                          4.732ns (2.247ns logic, 2.485ns route)
                                                           (47.5% logic, 52.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.190ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.683ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ----------------------------------------------------  -------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A13.T                net (fanout=32)       1.268   regmd/md_wr_inv
    A13.PAD              Tiotp                 1.858   d<28>
                                                       d_28_IOBUF/OBUFT
                                                       d<28>
    ----------------------------------------------------  -------------------------
    Total                                      4.683ns (2.194ns logic, 2.489ns route)
                                                       (46.9% logic, 53.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.088ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.586ns (Levels of Logic = 3)
```

```
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A13.T                net (fanout=32)       1.268   regmd/md_wr_inv
    A13.PAD              Tiotp                 1.858   d<28>
                                                       d_28_IOBUF/OBUFT
                                                       d<28>
    -------------------------------------------------  ---------------------------
    Total                                      4.586ns (2.210ns logic, 2.376ns route)
                                                       (48.2% logic, 51.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<28>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

  Paths for end point d<28> (A13.PAD), 9 paths
  ------------------------------------------------------------------------------
  Delay (fastest paths):  3.567ns (clock arrival + clock path + data path - uncertainty)
    Source:               regir/ir_30 (FF)
    Destination:          d<28> (PAD)
    Source Clock:         clk_BUFGP rising at 0.000ns
    Data Path Delay:      2.452ns (Levels of Logic = 2)
    Clock Path Delay:     1.140ns (Levels of Logic = 2)
    Clock Uncertainty:    0.025ns

    Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
      Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A13.T                net (fanout=32)       0.635   regmd/md_wr_inv
    A13.PAD              Tiotp                 1.148   d<28>
                                                       d_28_IOBUF/OBUFT
                                                       d<28>
    -------------------------------------------------  ---------------------------
    Total                                      2.452ns (1.280ns logic, 1.172ns route)
                                                       (52.2% logic, 47.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.560ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.447ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
```

```
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A13.T                net (fanout=32)       0.635   regmd/md_wr_inv
    A13.PAD              Tiotp                 1.148   d<28>
                                                       d_28_IOBUF/OBUFT
                                                       d<28>
    ------------------------------------------------  --------------------------
    Total                                      2.447ns (1.297ns logic, 1.150ns route)
                                                       (53.0% logic, 47.0% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.012ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_28 (FF)
  Destination:          d<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.879ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y54.CLK     net (fanout=368)      0.574   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_28 to d<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y54.BMUX    Tshcko                0.129   regmd/md<27>
                                                       regmd/md_28
    A13.O                net (fanout=2)        0.602   regmd/md<28>
    A13.PAD              Tioop                 1.148   d<28>
                                                       d_28_IOBUF/OBUFT
```

```
                                                       d<28>
    ---------------------------------------------  --------------------------
    Total                                       1.879ns (1.277ns logic, 0.602ns route)
                                                       (68.0% logic, 32.0% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<28>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.924ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_28 (SLICE_X35Y54.B1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.076ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<28> (PAD)
  Destination:          regmd/md_28 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.057ns (Levels of Logic = 2)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<28> to regmd/md_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    A13.I                Tiopi                 0.391   d<28>
                                                       d<28>
                                                       d_28_IOBUF/IBUF
    SLICE_X35Y54.B1      net (fanout=1)        1.641   N92
    SLICE_X35Y54.CLK     Tas                   0.025   regmd/md<27>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT211
                                                       regmd/md_28
    ---------------------------------------------  --------------------------
    Total                                       2.057ns (0.416ns logic, 1.641ns route)
                                                       (20.2% logic, 79.8% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
```

```
    SLICE_X35Y54.CLK     net (fanout=368)      0.574   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<28>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_28 (SLICE_X35Y54.B1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.935ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<28> (PAD)
  Destination:          regmd/md_28 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.474ns (Levels of Logic = 2)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<28> to regmd/md_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A13.I                Tiopi                 0.538   d<28>
                                                       d<28>
                                                       d_28_IOBUF/IBUF
    SLICE_X35Y54.B1      net (fanout=1)        2.045   N92
    SLICE_X35Y54.CLK     Tah         (-Th)     0.109   regmd/md<27>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT211
                                                       regmd/md_28
    -------------------------------------------------  ---------------------------
    Total                                      2.474ns (0.429ns logic, 2.045ns route)
                                                       (17.3% logic, 82.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y54.CLK     net (fanout=368)      1.412   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------
```

```
==============================================================================
Timing constraint: COMP "d<27>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.270ns.
------------------------------------------------------------------------------

Paths for end point d<27> (B18.PAD), 9 paths
------------------------------------------------------------------------------
Slack (slowest paths):  -3.270ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.768ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B18.T                net (fanout=32)       1.296   regmd/md_wr_inv
    B18.PAD              Tiotp                 1.866   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      4.768ns (2.255ns logic, 2.513ns route)
                                                       (47.3% logic, 52.7% route)
```

```
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.226ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.719ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B18.T                net (fanout=32)       1.296   regmd/md_wr_inv
    B18.PAD              Tiotp                 1.866   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      4.719ns (2.202ns logic, 2.517ns route)
                                                       (46.7% logic, 53.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.124ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.622ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B18.T                net (fanout=32)       1.296   regmd/md_wr_inv
    B18.PAD              Tiotp                 1.866   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      4.622ns (2.218ns logic, 2.404ns route)
                                                       (48.0% logic, 52.0% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<27>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<27> (B18.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.594ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.479ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B18.T                net (fanout=32)       0.655   regmd/md_wr_inv
    B18.PAD              Tiotp                 1.155   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      2.479ns (1.287ns logic, 1.192ns route)
                                                       (51.9% logic, 48.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.587ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.474ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
```

```
                                                        (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B18.T                net (fanout=32)       0.655   regmd/md_wr_inv
    B18.PAD              Tiotp                 1.155   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      2.474ns (1.304ns logic, 1.170ns route)
                                                       (52.7% logic, 47.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.950ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_27 (FF)
  Destination:          d<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.817ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y54.CLK     net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_27 to d<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y54.BQ      Tcko                  0.098   regmd/md<27>
                                                       regmd/md_27
    B18.O                net (fanout=2)        0.564   regmd/md<27>
    B18.PAD              Tioop                 1.155   d<27>
                                                       d_27_IOBUF/OBUFT
                                                       d<27>
    -------------------------------------------------  ---------------------------
    Total                                      1.817ns (1.253ns logic, 0.564ns route)
```

```
                                                       (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<27>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.688ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_27 (SLICE_X35Y54.B2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.312ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<27> (PAD)
  Destination:          regmd/md_27 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.821ns (Levels of Logic = 2)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<27> to regmd/md_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B18.I                Tiopi                 0.399   d<27>
                                                       d<27>
                                                       d_27_IOBUF/IBUF
    SLICE_X35Y54.B2      net (fanout=1)        1.393   N93
    SLICE_X35Y54.CLK     Tas                   0.029   regmd/md<27>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT201
                                                       regmd/md_27
    -------------------------------------------------  ---------------------------
    Total                                      1.821ns (0.428ns logic, 1.393ns route)
                                                       (23.5% logic, 76.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y54.CLK     net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
```

```
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<27>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_27 (SLICE_X35Y54.B2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.674ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<27> (PAD)
  Destination:          regmd/md_27 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.213ns (Levels of Logic = 2)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<27> to regmd/md_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B18.I                Tiopi                 0.545   d<27>
                                                       d<27>
                                                       d_27_IOBUF/IBUF
    SLICE_X35Y54.B2      net (fanout=1)        1.746   N93
    SLICE_X35Y54.CLK     Tah         (-Th)     0.078   regmd/md<27>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT201
                                                       regmd/md_27
    -------------------------------------------------  ---------------------------
    Total                                      2.213ns (0.467ns logic, 1.746ns route)
                                                       (21.1% logic, 78.9% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y54.CLK     net (fanout=368)      1.412   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<26>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).
```

```
 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.259ns.
--------------------------------------------------------------------------------

Paths for end point d<26> (F14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.259ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.757ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F14.T                net (fanout=32)       1.326   regmd/md_wr_inv
    F14.PAD              Tiotp                 1.825   d<26>
                                                       d_26_IOBUF/OBUFT
                                                       d<26>
    -------------------------------------------------  ---------------------------
    Total                                      4.757ns (2.214ns logic, 2.543ns route)
                                                       (46.5% logic, 53.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.215ns (requirement - (clock arrival + clock path + data path +
```

```
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.708ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F14.T                net (fanout=32)       1.326   regmd/md_wr_inv
    F14.PAD              Tiotp                 1.825   d<26>
                                                       d_26_IOBUF/OBUFT
                                                       d<26>
    -------------------------------------------------  ---------------------------
    Total                                      4.708ns (2.161ns logic, 2.547ns route)
                                                       (45.9% logic, 54.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.113ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.611ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F14.T                net (fanout=32)       1.326   regmd/md_wr_inv
    F14.PAD              Tiotp                 1.825   d<26>
                                                       d_26_IOBUF/OBUFT
                                                       d<26>
    -------------------------------------------------  ---------------------------
    Total                                      4.611ns (2.177ns logic, 2.434ns route)
                                                       (47.2% logic, 52.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<26>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<26> (F14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.575ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.460ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)       0.556   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       1.140ns (0.353ns logic, 0.787ns route)
                                                        (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                   0.098   regir/ir_28_1
                                                        regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)        0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                   0.034   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    F14.T                net (fanout=32)        0.672   regmd/md_wr_inv
    F14.PAD              Tiotp                  1.119   d<26>
                                                        d_26_IOBUF/OBUFT
                                                        d<26>
    ---------------------------------------------------  ---------------------------
    Total                                       2.460ns (1.251ns logic, 1.209ns route)
                                                        (50.9% logic, 49.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.568ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.455ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)       0.554   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       1.138ns (0.353ns logic, 0.785ns route)
                                                        (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<26>
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F14.T                net (fanout=32)       0.672   regmd/md_wr_inv
    F14.PAD              Tiotp                 1.119   d<26>
                                                       d_26_IOBUF/OBUFT
                                                       d<26>
    -------------------------------------------------  ---------------------------
    Total                                      2.455ns (1.268ns logic, 1.187ns route)
                                                       (51.6% logic, 48.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.946ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_26 (FF)
  Destination:          d<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.809ns (Levels of Logic = 1)
  Clock Path Delay:     1.162ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      0.578   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.162ns (0.353ns logic, 0.809ns route)
                                                       (30.4% logic, 69.6% route)

  Minimum Data Path at Fast Process Corner: regmd/md_26 to d<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y50.AMUX    Tshcko                0.130   regmd/md<25>
                                                       regmd/md_26
    F14.O                net (fanout=2)        0.560   regmd/md<26>
    F14.PAD              Tioop                 1.119   d<26>
                                                       d_26_IOBUF/OBUFT
                                                       d<26>
    -------------------------------------------------  ---------------------------
    Total                                      1.809ns (1.249ns logic, 0.560ns route)
                                                       (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------
```

```
==============================================================================
Timing constraint: COMP "d<26>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.919ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_26 (SLICE_X35Y50.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.081ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<26> (PAD)
  Destination:          regmd/md_26 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.056ns (Levels of Logic = 2)
  Clock Path Delay:     1.162ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<26> to regmd/md_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F14.I                Tiopi                 0.358   d<26>
                                                       d<26>
                                                       d_26_IOBUF/IBUF
    SLICE_X35Y50.A2      net (fanout=1)        1.674   N94
    SLICE_X35Y50.CLK     Tas                   0.024   regmd/md<25>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT191
                                                       regmd/md_26
    -------------------------------------------------  ---------------------------
    Total                                      2.056ns (0.382ns logic, 1.674ns route)
                                                       (18.6% logic, 81.4% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      0.578   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.162ns (0.353ns logic, 0.809ns route)
                                                       (30.4% logic, 69.6% route)

--------------------------------------------------------------------------------
```

```
Hold Paths: COMP "d<26>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_26 (SLICE_X35Y50.A2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.943ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<26> (PAD)
  Destination:          regmd/md_26 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.489ns (Levels of Logic = 2)
  Clock Path Delay:     2.521ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<26> to regmd/md_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F14.I                Tiopi                 0.509   d<26>
                                                       d<26>
                                                       d_26_IOBUF/IBUF
    SLICE_X35Y50.A2      net (fanout=1)        2.089   N94
    SLICE_X35Y50.CLK     Tah         (-Th)     0.109   regmd/md<25>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT191
                                                       regmd/md_26
    -------------------------------------------------  ---------------------------
    Total                                      2.489ns (0.400ns logic, 2.089ns route)
                                                       (16.1% logic, 83.9% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      1.419   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.521ns (0.622ns logic, 1.899ns route)
                                                       (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<25>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
```

```
 Minimum allowable offset is   7.302ns.
--------------------------------------------------------------------------------

Paths for end point d<25> (G14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.302ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.800ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G14.T                net (fanout=32)       1.379   regmd/md_wr_inv
    G14.PAD              Tiotp                 1.815   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    -------------------------------------------------  ---------------------------
    Total                                      4.800ns (2.204ns logic, 2.596ns route)
                                                       (45.9% logic, 54.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.258ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<25> (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.751ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G14.T                net (fanout=32)       1.379   regmd/md_wr_inv
    G14.PAD              Tiotp                 1.815   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    -------------------------------------------------  ---------------------------
    Total                                      4.751ns (2.151ns logic, 2.600ns route)
                                                       (45.3% logic, 54.7% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.156ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.654ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G14.T                net (fanout=32)       1.379   regmd/md_wr_inv
    G14.PAD              Tiotp                 1.815   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    -------------------------------------------------  ---------------------------
    Total                                      4.654ns (2.167ns logic, 2.487ns route)
                                                       (46.6% logic, 53.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<25>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<25> (G14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.590ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.475ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
```

```
                                                          clk
                                                          clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                          clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G14.T                net (fanout=32)       0.695   regmd/md_wr_inv
    G14.PAD              Tiotp                 1.111   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    ------------------------------------------------  --------------------------
    Total                                      2.475ns (1.243ns logic, 1.232ns route)
                                                       (50.2% logic, 49.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.583ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.470ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
```

```
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G14.T                net (fanout=32)       0.695   regmd/md_wr_inv
    G14.PAD              Tiotp                 1.111   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    ------------------------------------------------  --------------------------
    Total                                      2.470ns (1.260ns logic, 1.210ns route)
                                                       (51.0% logic, 49.0% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.952ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_25 (FF)
  Destination:          d<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.815ns (Levels of Logic = 1)
  Clock Path Delay:     1.162ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      0.578   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.162ns (0.353ns logic, 0.809ns route)
                                                       (30.4% logic, 69.6% route)

  Minimum Data Path at Fast Process Corner: regmd/md_25 to d<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y50.AQ      Tcko                  0.098   regmd/md<25>
                                                       regmd/md_25
    G14.O                net (fanout=2)        0.606   regmd/md<25>
    G14.PAD              Tioop                 1.111   d<25>
                                                       d_25_IOBUF/OBUFT
                                                       d<25>
    ------------------------------------------------  --------------------------
    Total                                      1.815ns (1.209ns logic, 0.606ns route)
                                                       (66.6% logic, 33.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<25>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
```

```
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   1.256ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_25 (SLICE_X35Y50.A1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     1.744ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<25> (PAD)
  Destination:          regmd/md_25 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.393ns (Levels of Logic = 2)
  Clock Path Delay:     1.162ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<25> to regmd/md_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    G14.I                Tiopi                 0.348   d<25>
                                                       d<25>
                                                       d_25_IOBUF/IBUF
    SLICE_X35Y50.A1      net (fanout=1)        2.014   N95
    SLICE_X35Y50.CLK     Tas                   0.031   regmd/md<25>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT181
                                                       regmd/md_25
    -------------------------------------------------  ---------------------------
    Total                                      2.393ns (0.379ns logic, 2.014ns route)
                                                       (15.8% logic, 84.2% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      0.578   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.162ns (0.353ns logic, 0.809ns route)
                                                       (30.4% logic, 69.6% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<25>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------
```

```
Paths for end point regmd/md_25 (SLICE_X35Y50.A1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      1.314ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<25> (PAD)
  Destination:          regmd/md_25 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.860ns (Levels of Logic = 2)
  Clock Path Delay:     2.521ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<25> to regmd/md_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    G14.I                Tiopi                 0.501   d<25>
                                                       d<25>
                                                       d_25_IOBUF/IBUF
    SLICE_X35Y50.A1      net (fanout=1)        2.434   N95
    SLICE_X35Y50.CLK     Tah         (-Th)     0.075   regmd/md<25>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT181
                                                       regmd/md_25
    -------------------------------------------------  ---------------------------
    Total                                      2.860ns (0.426ns logic, 2.434ns route)
                                                       (14.9% logic, 85.1% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y50.CLK     net (fanout=368)      1.419   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.521ns (0.622ns logic, 1.899ns route)
                                                       (24.7% logic, 75.3% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<24>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.005ns.
--------------------------------------------------------------------------------
```

```
Paths for end point d<24> (E16.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.005ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.503ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E16.T                net (fanout=32)       1.056   regmd/md_wr_inv
    E16.PAD              Tiotp                 1.841   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    -------------------------------------------------  ---------------------------
    Total                                      4.503ns (2.230ns logic, 2.273ns route)
                                                       (49.5% logic, 50.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.961ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.454ns (Levels of Logic = 2)
```

```
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E16.T                net (fanout=32)       1.056   regmd/md_wr_inv
    E16.PAD              Tiotp                 1.841   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    -------------------------------------------------  ---------------------------
    Total                                      4.454ns (2.177ns logic, 2.277ns route)
                                                       (48.9% logic, 51.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.859ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.357ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  ------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E16.T                net (fanout=32)       1.056   regmd/md_wr_inv
    E16.PAD              Tiotp                 1.841   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    ------------------------------------------------  --------------------------
    Total                                      4.357ns (2.193ns logic, 2.164ns route)
                                                       (50.3% logic, 49.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<24>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<24> (E16.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.427ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.312ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  ------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E16.T                net (fanout=32)       0.510   regmd/md_wr_inv
    E16.PAD              Tiotp                 1.133   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    -------------------------------------------------  ---------------------------
    Total                                      2.312ns (1.265ns logic, 1.047ns route)
                                                       (54.7% logic, 45.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.420ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.307ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
```

```
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E16.T                net (fanout=32)       0.510   regmd/md_wr_inv
    E16.PAD              Tiotp                 1.133   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    ---------------------------------------------  ---------------------------
    Total                                      2.307ns (1.282ns logic, 1.025ns route)
                                                       (55.6% logic, 44.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.905ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_24 (FF)
  Destination:          d<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.764ns (Levels of Logic = 1)
  Clock Path Delay:     1.166ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y62.CLK     net (fanout=368)      0.582   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      1.166ns (0.353ns logic, 0.813ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_24 to d<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X36Y62.BMUX    Tshcko                0.148   regmd/md<23>
                                                       regmd/md_24
    E16.O                net (fanout=2)        0.483   regmd/md<24>
    E16.PAD              Tioop                 1.133   d<24>
                                                       d_24_IOBUF/OBUFT
                                                       d<24>
    ---------------------------------------------  ---------------------------
    Total                                      1.764ns (1.281ns logic, 0.483ns route)
                                                       (72.6% logic, 27.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<24>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).
```

```
 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.798ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_24 (SLICE_X36Y62.B2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.202ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<24> (PAD)
  Destination:          regmd/md_24 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.939ns (Levels of Logic = 2)
  Clock Path Delay:     1.166ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<24> to regmd/md_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E16.I                Tiopi                 0.374   d<24>
                                                       d<24>
                                                       d_24_IOBUF/IBUF
    SLICE_X36Y62.B2      net (fanout=1)        1.551   N96
    SLICE_X36Y62.CLK     Tas                   0.014   regmd/md<23>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT171
                                                       regmd/md_24
    -------------------------------------------------  ---------------------------
    Total                                      1.939ns (0.388ns logic, 1.551ns route)
                                                       (20.0% logic, 80.0% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y62.CLK     net (fanout=368)      0.582   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.166ns (0.353ns logic, 0.813ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<24>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_24 (SLICE_X36Y62.B2), 1 path
--------------------------------------------------------------------------------
```

```
Slack (hold path):      0.780ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<24> (PAD)
  Destination:          regmd/md_24 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.330ns (Levels of Logic = 2)
  Clock Path Delay:     2.525ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<24> to regmd/md_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E16.I                Tiopi                 0.523   d<24>
                                                       d<24>
                                                       d_24_IOBUF/IBUF
    SLICE_X36Y62.B2      net (fanout=1)        1.947   N96
    SLICE_X36Y62.CLK     Tah         (-Th)     0.140   regmd/md<23>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT171
                                                       regmd/md_24
    -------------------------------------------------  ---------------------------
    Total                                      2.330ns (0.383ns logic, 1.947ns route)
                                                       (16.4% logic, 83.6% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y62.CLK     net (fanout=368)      1.423   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.525ns (0.622ns logic, 1.903ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<23>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.007ns.
--------------------------------------------------------------------------------

Paths for end point d<23> (C13.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.007ns (requirement - (clock arrival + clock path + data path +
```

```
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.505ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C13.T                net (fanout=32)       1.058   regmd/md_wr_inv
    C13.PAD              Tiotp                 1.841   d<23>
                                                       d_23_IOBUF/OBUFT
                                                       d<23>
    -------------------------------------------------  ---------------------------
    Total                                      4.505ns (2.230ns logic, 2.275ns route)
                                                       (49.5% logic, 50.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.963ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.456ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C13.T                net (fanout=32)       1.058   regmd/md_wr_inv
    C13.PAD              Tiotp                 1.841   d<23>
                                                       d_23_IOBUF/OBUFT
                                                       d<23>
    -------------------------------------------------  ---------------------------
    Total                                      4.456ns (2.177ns logic, 2.279ns route)
                                                       (48.9% logic, 51.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.861ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.359ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
```

```
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C13.T                net (fanout=32)       1.058   regmd/md_wr_inv
    C13.PAD              Tiotp                 1.841   d<23>
                                                       d_23_IOBUF/OBUFT
                                                       d<23>
    ------------------------------------------------  ---------------------------
    Total                                      4.359ns (2.193ns logic, 2.166ns route)
                                                       (50.3% logic, 49.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<23>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<23> (C13.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.425ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.310ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
```

```
    ------------------------------------------------  --------------------------
    Total                                             1.140ns (0.353ns logic, 0.787ns route)
                                                              (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C13.T                net (fanout=32)       0.508   regmd/md_wr_inv
    C13.PAD              Tiotp                 1.133   d<23>
                                                       d_23_IOBUF/OBUFT
                                                       d<23>
    ------------------------------------------------  --------------------------
    Total                                             2.310ns (1.265ns logic, 1.045ns route)
                                                              (54.8% logic, 45.2% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.418ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.305ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                             1.138ns (0.353ns logic, 0.785ns route)
                                                              (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C13.T                net (fanout=32)       0.508   regmd/md_wr_inv
```

```
    C13.PAD             Tiotp                 1.133   d<23>
                                                      d_23_IOBUF/OBUFT
                                                      d<23>
    ------------------------------------------------  --------------------------
    Total                                     2.305ns (1.282ns logic, 1.023ns route)
                                                      (55.6% logic, 44.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.824ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_23 (FF)
  Destination:          d<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.683ns (Levels of Logic = 1)
  Clock Path Delay:     1.166ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_23
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I               Tiopi                 0.320   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0    net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O     Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                      clk_BUFGP/BUFG
    SLICE_X36Y62.CLK    net (fanout=368)      0.582   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                     1.166ns (0.353ns logic, 0.813ns route)
                                                      (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_23 to d<23>
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X36Y62.BQ     Tcko                  0.115   regmd/md<23>
                                                      regmd/md_23
    C13.O               net (fanout=2)        0.435   regmd/md<23>
    C13.PAD             Tioop                 1.133   d<23>
                                                      d_23_IOBUF/OBUFT
                                                      d<23>
    ------------------------------------------------  --------------------------
    Total                                     1.683ns (1.248ns logic, 0.435ns route)
                                                      (74.2% logic, 25.8% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<23>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   1.045ns.
```

```
--------------------------------------------------------------------------------

Paths for end point regmd/md_23 (SLICE_X36Y62.B1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     1.955ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<23> (PAD)
  Destination:          regmd/md_23 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.186ns (Levels of Logic = 2)
  Clock Path Delay:     1.166ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<23> to regmd/md_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C13.I                Tiopi                 0.374   d<23>
                                                       d<23>
                                                       d_23_IOBUF/IBUF
    SLICE_X36Y62.B1      net (fanout=1)        1.803   N97
    SLICE_X36Y62.CLK     Tas                   0.009   regmd/md<23>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT161
                                                       regmd/md_23
    -------------------------------------------------  ---------------------------
    Total                                      2.186ns (0.383ns logic, 1.803ns route)
                                                       (17.5% logic, 82.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y62.CLK     net (fanout=368)      0.582   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.166ns (0.353ns logic, 0.813ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<23>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_23 (SLICE_X36Y62.B1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      1.114ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<23> (PAD)
```

```
  Destination:          regmd/md_23 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.664ns (Levels of Logic = 2)
  Clock Path Delay:     2.525ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<23> to regmd/md_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C13.I                Tiopi                 0.523   d<23>
                                                       d<23>
                                                       d_23_IOBUF/IBUF
    SLICE_X36Y62.B1      net (fanout=1)        2.257   N97
    SLICE_X36Y62.CLK     Tah         (-Th)     0.116   regmd/md<23>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT161
                                                       regmd/md_23
    -------------------------------------------------  ---------------------------
    Total                                      2.664ns (0.407ns logic, 2.257ns route)
                                                       (15.3% logic, 84.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y62.CLK     net (fanout=368)      1.423   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.525ns (0.622ns logic, 1.903ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<22>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.212ns.
--------------------------------------------------------------------------------

Paths for end point d<22> (F13.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.212ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<22> (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.710ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F13.T                net (fanout=32)       1.288   regmd/md_wr_inv
    F13.PAD              Tiotp                 1.816   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
    -------------------------------------------------  ---------------------------
    Total                                      4.710ns (2.205ns logic, 2.505ns route)
                                                       (46.8% logic, 53.2% route)


--------------------------------------------------------------------------------
Slack (slowest paths):  -3.168ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.661ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F13.T                net (fanout=32)       1.288   regmd/md_wr_inv
    F13.PAD              Tiotp                 1.816   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
    -------------------------------------------------  ---------------------------
    Total                                      4.661ns (2.152ns logic, 2.509ns route)
                                                       (46.2% logic, 53.8% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.066ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.564ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
```

```
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F13.T                net (fanout=32)       1.288   regmd/md_wr_inv
    F13.PAD              Tiotp                 1.816   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
    ---------------------------------------------  ---------------------------
    Total                                      4.564ns (2.168ns logic, 2.396ns route)
                                                       (47.5% logic, 52.5% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<22>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<22> (F13.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.534ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.419ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)
```

```
  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F13.T                net (fanout=32)       0.638   regmd/md_wr_inv
    F13.PAD              Tiotp                 1.112   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
    -------------------------------------------------  ---------------------------
    Total                                      2.419ns (1.244ns logic, 1.175ns route)
                                                       (51.4% logic, 48.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.527ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.414ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F13.T                net (fanout=32)       0.638   regmd/md_wr_inv
    F13.PAD              Tiotp                 1.112   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
```

```
    ----------------------------------------------------  ---------------------------
    Total                                          2.414ns (1.261ns logic, 1.153ns route)
                                                           (52.2% logic, 47.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.844ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_22 (FF)
  Destination:          d<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.695ns (Levels of Logic = 1)
  Clock Path Delay:     1.174ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      0.590   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                      1.174ns (0.353ns logic, 0.821ns route)
                                                       (30.1% logic, 69.9% route)

  Minimum Data Path at Fast Process Corner: regmd/md_22 to d<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X36Y70.DMUX    Tshcko                0.146   regmd/md<21>
                                                       regmd/md_22
    F13.O                net (fanout=2)        0.437   regmd/md<22>
    F13.PAD              Tioop                 1.112   d<22>
                                                       d_22_IOBUF/OBUFT
                                                       d<22>
    ----------------------------------------------------  ---------------------------
    Total                                      1.695ns (1.258ns logic, 0.437ns route)
                                                       (74.2% logic, 25.8% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<22>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   1.004ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_22 (SLICE_X36Y70.D1), 1 path
```

```
--------------------------------------------------------------------------------
Slack (setup path):     1.996ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<22> (PAD)
  Destination:          regmd/md_22 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.153ns (Levels of Logic = 2)
  Clock Path Delay:     1.174ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<22> to regmd/md_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F13.I                Tiopi                 0.349   d<22>
                                                       d<22>
                                                       d_22_IOBUF/IBUF
    SLICE_X36Y70.D1      net (fanout=1)        1.791   N98
    SLICE_X36Y70.CLK     Tas                   0.013   regmd/md<21>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT151
                                                       regmd/md_22
    -------------------------------------------------  ---------------------------
    Total                                      2.153ns (0.362ns logic, 1.791ns route)
                                                       (16.8% logic, 83.2% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      0.590   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.174ns (0.353ns logic, 0.821ns route)
                                                       (30.1% logic, 69.9% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<22>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_22 (SLICE_X36Y70.D1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      1.066ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<22> (PAD)
  Destination:          regmd/md_22 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
```

```
  Data Path Delay:      2.630ns (Levels of Logic = 2)
  Clock Path Delay:     2.539ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<22> to regmd/md_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F13.I                Tiopi                 0.502   d<22>
                                                       d<22>
                                                       d_22_IOBUF/IBUF
    SLICE_X36Y70.D1      net (fanout=1)        2.269   N98
    SLICE_X36Y70.CLK     Tah         (-Th)     0.141   regmd/md<21>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT151
                                                       regmd/md_22
    -------------------------------------------------  ---------------------------
    Total                                      2.630ns (0.361ns logic, 2.269ns route)
                                                       (13.7% logic, 86.3% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      1.437   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.539ns (0.622ns logic, 1.917ns route)
                                                       (24.5% logic, 75.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<21>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.122ns.
--------------------------------------------------------------------------------

Paths for end point d<21> (G13.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.122ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.620ns (Levels of Logic = 3)
```

```
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G13.T                net (fanout=32)       1.205   regmd/md_wr_inv
    G13.PAD              Tiotp                 1.809   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    -------------------------------------------------  ---------------------------
    Total                                      4.620ns (2.198ns logic, 2.422ns route)
                                                       (47.6% logic, 52.4% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.078ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.571ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G13.T                net (fanout=32)       1.205   regmd/md_wr_inv
    G13.PAD              Tiotp                 1.809   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    -------------------------------------------------  ---------------------------
    Total                                      4.571ns (2.145ns logic, 2.426ns route)
                                                       (46.9% logic, 53.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.976ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.474ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
```

```
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G13.T                net (fanout=32)       1.205   regmd/md_wr_inv
    G13.PAD              Tiotp                 1.809   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    -------------------------------------------------  ---------------------------
    Total                                     4.474ns (2.161ns logic, 2.313ns route)
                                                      (48.3% logic, 51.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<21>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<21> (G13.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.484ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.369ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.140ns (0.353ns logic, 0.787ns route)
                                                      (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G13.T                net (fanout=32)       0.594   regmd/md_wr_inv
    G13.PAD              Tiotp                 1.106   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    ---------------------------------------------------  ---------------------------
    Total                                      2.369ns (1.238ns logic, 1.131ns route)
                                                       (52.3% logic, 47.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.477ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.364ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    G13.T                net (fanout=32)       0.594   regmd/md_wr_inv
    G13.PAD              Tiotp                 1.106   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    ---------------------------------------------------  ---------------------------
    Total                                      2.364ns (1.255ns logic, 1.109ns route)
                                                       (53.1% logic, 46.9% route)
```

```
--------------------------------------------------------------------------------
Delay (fastest paths):  2.849ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_21 (FF)
  Destination:          d<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.700ns (Levels of Logic = 1)
  Clock Path Delay:     1.174ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      0.590   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.174ns (0.353ns logic, 0.821ns route)
                                                       (30.1% logic, 69.9% route)

  Minimum Data Path at Fast Process Corner: regmd/md_21 to d<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y70.DQ      Tcko                  0.115   regmd/md<21>
                                                       regmd/md_21
    G13.O                net (fanout=2)        0.479   regmd/md<21>
    G13.PAD              Tioop                 1.106   d<21>
                                                       d_21_IOBUF/OBUFT
                                                       d<21>
    -------------------------------------------------  ---------------------------
    Total                                      1.700ns (1.221ns logic, 0.479ns route)
                                                       (71.8% logic, 28.2% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<21>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.872ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_21 (SLICE_X36Y70.D2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.128ns (requirement - (data path - clock path - clock arrival +
uncertainty))
```

```
  Source:               d<21> (PAD)
  Destination:          regmd/md_21 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.021ns (Levels of Logic = 2)
  Clock Path Delay:     1.174ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<21> to regmd/md_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    G13.I                Tiopi                 0.342   d<21>
                                                       d<21>
                                                       d_21_IOBUF/IBUF
    SLICE_X36Y70.D2      net (fanout=1)        1.669   N99
    SLICE_X36Y70.CLK     Tas                   0.010   regmd/md<21>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT141
                                                       regmd/md_21
    -------------------------------------------------  ---------------------------
    Total                                      2.021ns (0.352ns logic, 1.669ns route)
                                                       (17.4% logic, 82.6% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      0.590   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.174ns (0.353ns logic, 0.821ns route)
                                                       (30.1% logic, 69.9% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<21>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_21 (SLICE_X36Y70.D2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.875ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<21> (PAD)
  Destination:          regmd/md_21 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.439ns (Levels of Logic = 2)
  Clock Path Delay:     2.539ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<21> to regmd/md_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    G13.I                Tiopi                 0.496   d<21>
                                                       d<21>
                                                       d_21_IOBUF/IBUF
    SLICE_X36Y70.D2      net (fanout=1)        2.059   N99
    SLICE_X36Y70.CLK     Tah         (-Th)     0.116   regmd/md<21>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT141
                                                       regmd/md_21
    -------------------------------------------------  ---------------------------
    Total                                      2.439ns (0.380ns logic, 2.059ns route)
                                                       (15.6% logic, 84.4% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y70.CLK     net (fanout=368)      1.437   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.539ns (0.622ns logic, 1.917ns route)
                                                       (24.5% logic, 75.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<20>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   6.920ns.
--------------------------------------------------------------------------------

Paths for end point d<20> (F16.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.920ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.418ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F16.T                net (fanout=32)       0.976   regmd/md_wr_inv
    F16.PAD              Tiotp                 1.836   d<20>
                                                       d_20_IOBUF/OBUFT
                                                       d<20>
    -------------------------------------------------  ---------------------------
    Total                                      4.418ns (2.225ns logic, 2.193ns route)
                                                       (50.4% logic, 49.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.876ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.369ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)       1.380   clk_BUFGP
    ----------------------------------------------------  --------------------------
    Total                                       2.482ns (0.622ns logic, 1.860ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    SLICE_X26Y61.AQ      Tcko                   0.283   control1/state_FSM_FFd2
                                                        control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)        1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                   0.053   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    F16.T                net (fanout=32)        0.976   regmd/md_wr_inv
    F16.PAD              Tiotp                  1.836   d<20>
                                                        d_20_IOBUF/OBUFT
                                                        d<20>
    ----------------------------------------------------  --------------------------
    Total                                       4.369ns (2.172ns logic, 2.197ns route)
                                                        (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.774ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.272ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)       1.375   clk_BUFGP
    ----------------------------------------------------  --------------------------
    Total                                       2.477ns (0.622ns logic, 1.855ns route)
                                                        (25.1% logic, 74.9% route)
```

```
  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F16.T                net (fanout=32)       0.976   regmd/md_wr_inv
    F16.PAD              Tiotp                 1.836   d<20>
                                                       d_20_IOBUF/OBUFT
                                                       d<20>
    -------------------------------------------------  ---------------------------
    Total                                      4.272ns (2.188ns logic, 2.084ns route)
                                                       (51.2% logic, 48.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<20>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<20> (F16.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.381ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.266ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
```

```
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F16.T                net (fanout=32)       0.467   regmd/md_wr_inv
    F16.PAD              Tiotp                 1.130   d<20>
                                                       d_20_IOBUF/OBUFT
                                                       d<20>
    ---------------------------------------------  ---------------------------
    Total                                      2.266ns (1.262ns logic, 1.004ns route)
                                                       (55.7% logic, 44.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.374ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.261ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F16.T                net (fanout=32)       0.467   regmd/md_wr_inv
    F16.PAD              Tiotp                 1.130   d<20>
                                                       d_20_IOBUF/OBUFT
                                                       d<20>
    ---------------------------------------------  ---------------------------
    Total                                      2.261ns (1.279ns logic, 0.982ns route)
                                                       (56.6% logic, 43.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.947ns (clock arrival + clock path + data path - uncertainty)
```

```
  Source:               regmd/md_20 (FF)
  Destination:          d<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.820ns (Levels of Logic = 1)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)     0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regmd/md_20 to d<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y60.AMUX    Tshcko               0.130   regmd/md<1>
                                                       regmd/md_20
    F16.O                net (fanout=2)       0.560   regmd/md<20>
    F16.PAD              Tioop                1.130   d<20>
                                                       d_20_IOBUF/OBUFT
                                                       d<20>
    -------------------------------------------------  ---------------------------
    Total                                     1.820ns (1.260ns logic, 0.560ns route)
                                                       (69.2% logic, 30.8% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<20>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.968ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_20 (SLICE_X35Y60.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.032ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<20> (PAD)
  Destination:          regmd/md_20 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
```

```
  Requirement:          3.000ns
  Data Path Delay:      2.095ns (Levels of Logic = 2)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<20> to regmd/md_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F16.I                Tiopi                 0.369   d<20>
                                                       d<20>
                                                       d_20_IOBUF/IBUF
    SLICE_X35Y60.A2      net (fanout=1)        1.702   N100
    SLICE_X35Y60.CLK     Tas                   0.024   regmd/md<1>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT131
                                                       regmd/md_20
    -------------------------------------------------  ---------------------------
    Total                                      2.095ns (0.393ns logic, 1.702ns route)
                                                       (18.8% logic, 81.2% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<20>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_20 (SLICE_X35Y60.A2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.964ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<20> (PAD)
  Destination:          regmd/md_20 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.492ns (Levels of Logic = 2)
  Clock Path Delay:     2.503ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<20> to regmd/md_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F16.I                Tiopi                 0.520   d<20>
                                                       d<20>
                                                       d_20_IOBUF/IBUF
    SLICE_X35Y60.A2      net (fanout=1)        2.081   N100
    SLICE_X35Y60.CLK     Tah         (-Th)     0.109   regmd/md<1>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT131
                                                       regmd/md_20
    -------------------------------------------------  ---------------------------
    Total                                      2.492ns (0.411ns logic, 2.081ns route)
                                                       (16.5% logic, 83.5% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)      1.401   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.503ns (0.622ns logic, 1.881ns route)
                                                       (24.9% logic, 75.1% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<19>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.230ns.
--------------------------------------------------------------------------------

Paths for end point d<19> (A16.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.230ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.728ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A16.T                net (fanout=32)       1.265   regmd/md_wr_inv
    A16.PAD              Tiotp                 1.857   d<19>
                                                       d_19_IOBUF/OBUFT
                                                       d<19>
    -------------------------------------------------  ---------------------------
    Total                                      4.728ns (2.246ns logic, 2.482ns route)
                                                       (47.5% logic, 52.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.186ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.679ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
```

```
                                                     clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                     clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A16.T                net (fanout=32)       1.265   regmd/md_wr_inv
    A16.PAD              Tiotp                 1.857   d<19>
                                                       d_19_IOBUF/OBUFT
                                                       d<19>
    -------------------------------------------------  ---------------------------
    Total                                      4.679ns (2.193ns logic, 2.486ns route)
                                                       (46.9% logic, 53.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.084ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.582ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A16.T                net (fanout=32)       1.265   regmd/md_wr_inv
    A16.PAD              Tiotp                 1.857   d<19>
                                                       d_19_IOBUF/OBUFT
                                                       d<19>
    ------------------------------------------------  --------------------------
    Total                                      4.582ns (2.209ns logic, 2.373ns route)
                                                       (48.2% logic, 51.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<19>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<19> (A16.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.553ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.438ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
```

```
                                                        regmd/md_wr_inv1
    A16.T                net (fanout=32)       0.622   regmd/md_wr_inv
    A16.PAD              Tiotp                 1.147   d<19>
                                                        d_19_IOBUF/OBUFT
                                                        d<19>
    -------------------------------------------------  ---------------------------
    Total                                      2.438ns (1.279ns logic, 1.159ns route)
                                                        (52.5% logic, 47.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.546ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.433ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A16.T                net (fanout=32)       0.622   regmd/md_wr_inv
    A16.PAD              Tiotp                 1.147   d<19>
                                                       d_19_IOBUF/OBUFT
                                                       d<19>
    -------------------------------------------------  ---------------------------
    Total                                      2.433ns (1.296ns logic, 1.137ns route)
                                                       (53.3% logic, 46.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.904ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_19 (FF)
  Destination:          d<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
```

```
  Data Path Delay:      1.758ns (Levels of Logic = 1)
  Clock Path Delay:     1.171ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      0.587   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.171ns (0.353ns logic, 0.818ns route)
                                                       (30.1% logic, 69.9% route)

  Minimum Data Path at Fast Process Corner: regmd/md_19 to d<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X37Y67.AMUX    Tshcko                0.130   regmd/md<18>
                                                       regmd/md_19
    A16.O                net (fanout=2)        0.481   regmd/md<19>
    A16.PAD              Tioop                 1.147   d<19>
                                                       d_19_IOBUF/OBUFT
                                                       d<19>
    -------------------------------------------------  ---------------------------
    Total                                      1.758ns (1.277ns logic, 0.481ns route)
                                                       (72.6% logic, 27.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<19>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.904ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_19 (SLICE_X37Y67.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.096ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<19> (PAD)
  Destination:          regmd/md_19 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.050ns (Levels of Logic = 2)
  Clock Path Delay:     1.171ns (Levels of Logic = 2)
```

```
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<19> to regmd/md_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A16.I                Tiopi                 0.390   d<19>
                                                       d<19>
                                                       d_19_IOBUF/IBUF
    SLICE_X37Y67.A2      net (fanout=1)        1.636   N101
    SLICE_X37Y67.CLK     Tas                   0.024   regmd/md<18>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT111
                                                       regmd/md_19
    -------------------------------------------------  ---------------------------
    Total                                      2.050ns (0.414ns logic, 1.636ns route)
                                                       (20.2% logic, 79.8% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      0.587   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.171ns (0.353ns logic, 0.818ns route)
                                                       (30.1% logic, 69.9% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<19>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_19 (SLICE_X37Y67.A2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.934ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<19> (PAD)
  Destination:          regmd/md_19 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.494ns (Levels of Logic = 2)
  Clock Path Delay:     2.535ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Data Path at Slow Process Corner: d<19> to regmd/md_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    A16.I                Tiopi                 0.537   d<19>
                                                       d<19>
                                                       d_19_IOBUF/IBUF
    SLICE_X37Y67.A2      net (fanout=1)        2.066   N101
    SLICE_X37Y67.CLK     Tah         (-Th)     0.109   regmd/md<18>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT111
                                                       regmd/md_19
    ------------------------------------------------  --------------------------
    Total                                      2.494ns (0.428ns logic, 2.066ns route)
                                                       (17.2% logic, 82.8% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      1.433   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.535ns (0.622ns logic, 1.913ns route)
                                                       (24.5% logic, 75.5% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<18>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.097ns.
--------------------------------------------------------------------------------

Paths for end point d<18> (F12.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.097ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.595ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F12.T                net (fanout=32)       1.169   regmd/md_wr_inv
    F12.PAD              Tiotp                 1.820   d<18>
                                                       d_18_IOBUF/OBUFT
                                                       d<18>
    -------------------------------------------------  ---------------------------
    Total                                      4.595ns (2.209ns logic, 2.386ns route)
                                                       (48.1% logic, 51.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.053ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.546ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
```

```
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                        control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    F12.T                net (fanout=32)       1.169   regmd/md_wr_inv
    F12.PAD              Tiotp                 1.820   d<18>
                                                        d_18_IOBUF/OBUFT
                                                        d<18>
    -------------------------------------------------  ---------------------------
    Total                                      4.546ns (2.156ns logic, 2.390ns route)
                                                        (47.4% logic, 52.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.951ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.449ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                        regir/ir_27
```

```
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F12.T                net (fanout=32)       1.169   regmd/md_wr_inv
    F12.PAD              Tiotp                 1.820   d<18>
                                                       d_18_IOBUF/OBUFT
                                                       d<18>
    ------------------------------------------------  ---------------------------
    Total                                      4.449ns (2.172ns logic, 2.277ns route)
                                                       (48.8% logic, 51.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<18>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<18> (F12.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.469ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.354ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F12.T                net (fanout=32)       0.569   regmd/md_wr_inv
    F12.PAD              Tiotp                 1.116   d<18>
```

```
                                                       d_18_IOBUF/OBUFT
                                                       d<18>
    ---------------------------------------------  --------------------------
    Total                                    2.354ns (1.248ns logic, 1.106ns route)
                                                       (53.0% logic, 47.0% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.462ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.349ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ---------------------------------------------  --------------------------
    Total                                    1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    F12.T                net (fanout=32)       0.569   regmd/md_wr_inv
    F12.PAD              Tiotp                 1.116   d<18>
                                                       d_18_IOBUF/OBUFT
                                                       d<18>
    ---------------------------------------------  --------------------------
    Total                                    2.349ns (1.265ns logic, 1.084ns route)
                                                       (53.9% logic, 46.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.793ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_18 (FF)
  Destination:          d<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.647ns (Levels of Logic = 1)
  Clock Path Delay:     1.171ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      0.587   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.171ns (0.353ns logic, 0.818ns route)
                                                       (30.1% logic, 69.9% route)

  Minimum Data Path at Fast Process Corner: regmd/md_18 to d<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X37Y67.AQ      Tcko                  0.098   regmd/md<18>
                                                       regmd/md_18
    F12.O                net (fanout=2)        0.433   regmd/md<18>
    F12.PAD              Tioop                 1.116   d<18>
                                                       d_18_IOBUF/OBUFT
                                                       d<18>
    -------------------------------------------------  ---------------------------
    Total                                      1.647ns (1.214ns logic, 0.433ns route)
                                                       (73.7% logic, 26.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<18>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.791ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_18 (SLICE_X37Y67.A1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.209ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<18> (PAD)
  Destination:          regmd/md_18 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.937ns (Levels of Logic = 2)
  Clock Path Delay:     1.171ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<18> to regmd/md_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    F12.I                Tiopi                 0.353   d<18>
                                                       d<18>
                                                       d_18_IOBUF/IBUF
    SLICE_X37Y67.A1      net (fanout=1)        1.553   N102
    SLICE_X37Y67.CLK     Tas                   0.031   regmd/md<18>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT101
                                                       regmd/md_18
    -------------------------------------------------  ---------------------------
    Total                                      1.937ns (0.384ns logic, 1.553ns route)
                                                       (19.8% logic, 80.2% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      0.587   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.171ns (0.353ns logic, 0.818ns route)
                                                       (30.1% logic, 69.9% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<18>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_18 (SLICE_X37Y67.A1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.791ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<18> (PAD)
  Destination:          regmd/md_18 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.351ns (Levels of Logic = 2)
  Clock Path Delay:     2.535ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<18> to regmd/md_18
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    F12.I                Tiopi                 0.506   d<18>
                                                       d<18>
                                                       d_18_IOBUF/IBUF
    SLICE_X37Y67.A1      net (fanout=1)        1.920   N102
    SLICE_X37Y67.CLK     Tah         (-Th)     0.075   regmd/md<18>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT101
                                                       regmd/md_18
    ---------------------------------------------------  ---------------------------
    Total                                      2.351ns (0.431ns logic, 1.920ns route)
                                                       (18.3% logic, 81.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X37Y67.CLK     net (fanout=368)      1.433   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.535ns (0.622ns logic, 1.913ns route)
                                                       (24.5% logic, 75.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<17>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.037ns.
--------------------------------------------------------------------------------

Paths for end point d<17> (A18.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.037ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.535ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)       1.375   clk_BUFGP
    ----------------------------------------------------  --------------------------
    Total                                       2.477ns (0.622ns logic, 1.855ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    SLICE_X24Y61.BQ      Tcko                   0.283   regir/ir<29>
                                                        regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)        0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                   0.053   regir/ir_29_1
                                                        control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)         0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                   0.053   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    A18.T                net (fanout=32)        1.061   regmd/md_wr_inv
    A18.PAD              Tiotp                  1.868   d<17>
                                                        d_17_IOBUF/OBUFT
                                                        d<17>
    ----------------------------------------------------  --------------------------
    Total                                       4.535ns (2.257ns logic, 2.278ns route)
                                                        (49.8% logic, 50.2% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.993ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.486ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)       1.380   clk_BUFGP
    ----------------------------------------------------  --------------------------
```

```
    Total                                     2.482ns (0.622ns logic, 1.860ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A18.T                net (fanout=32)       1.061   regmd/md_wr_inv
    A18.PAD              Tiotp                 1.868   d<17>
                                                       d_17_IOBUF/OBUFT
                                                       d<17>
    -------------------------------------------------  ---------------------------
    Total                                     4.486ns (2.204ns logic, 2.282ns route)
                                                      (49.1% logic, 50.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.891ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.389ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
```

```
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A18.T                net (fanout=32)       1.061   regmd/md_wr_inv
    A18.PAD              Tiotp                 1.868   d<17>
                                                       d_17_IOBUF/OBUFT
                                                       d<17>
    -------------------------------------------------  ---------------------------
    Total                                      4.389ns (2.220ns logic, 2.169ns route)
                                                       (50.6% logic, 49.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<17>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<17> (A18.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.447ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.332ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A18.T                net (fanout=32)       0.507   regmd/md_wr_inv
    A18.PAD              Tiotp                 1.156   d<17>
                                                       d_17_IOBUF/OBUFT
                                                       d<17>
    -------------------------------------------------  ---------------------------
```

```
    Total                                     2.332ns (1.288ns logic, 1.044ns route)
                                                      (55.2% logic, 44.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.440ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.327ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A18.T                net (fanout=32)       0.507   regmd/md_wr_inv
    A18.PAD              Tiotp                 1.156   d<17>
                                                       d_17_IOBUF/OBUFT
                                                       d<17>
    -------------------------------------------------  ---------------------------
    Total                                      2.327ns (1.305ns logic, 1.022ns route)
                                                       (56.1% logic, 43.9% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.850ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_17 (FF)
  Destination:          d<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.706ns (Levels of Logic = 1)
  Clock Path Delay:     1.169ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      0.585   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.169ns (0.353ns logic, 0.816ns route)
                                                       (30.2% logic, 69.8% route)

  Minimum Data Path at Fast Process Corner: regmd/md_17 to d<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y64.CQ      Tcko                  0.115   regmd/md<17>
                                                       regmd/md_17
    A18.O                net (fanout=2)        0.435   regmd/md<17>
    A18.PAD              Tioop                 1.156   d<17>
                                                       d_17_IOBUF/OBUFT
                                                       d<17>
    -------------------------------------------------  ---------------------------
    Total                                      1.706ns (1.271ns logic, 0.435ns route)
                                                       (74.5% logic, 25.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<17>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.993ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_17 (SLICE_X36Y64.C1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.007ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<17> (PAD)
  Destination:          regmd/md_17 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.137ns (Levels of Logic = 2)
  Clock Path Delay:     1.169ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<17> to regmd/md_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A18.I                Tiopi                 0.401   d<17>
                                                       d<17>
                                                       d_17_IOBUF/IBUF
    SLICE_X36Y64.C1      net (fanout=1)        1.725   N103
    SLICE_X36Y64.CLK     Tas                   0.011   regmd/md<17>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT91
                                                       regmd/md_17
    -------------------------------------------------  ---------------------------
    Total                                      2.137ns (0.412ns logic, 1.725ns route)
                                                       (19.3% logic, 80.7% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      0.585   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.169ns (0.353ns logic, 0.816ns route)
                                                       (30.2% logic, 69.8% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<17>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_17 (SLICE_X36Y64.C1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.948ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<17> (PAD)
  Destination:          regmd/md_17 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.502ns (Levels of Logic = 2)
  Clock Path Delay:     2.529ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<17> to regmd/md_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A18.I                Tiopi                 0.546   d<17>
```

```
                                                       d<17>
                                                       d_17_IOBUF/IBUF
    SLICE_X36Y64.C1      net (fanout=1)        2.070   N103
    SLICE_X36Y64.CLK     Tah         (-Th)     0.114   regmd/md<17>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT91
                                                       regmd/md_17
    ---------------------------------------------------  ---------------------------
    Total                                      2.502ns (0.432ns logic, 2.070ns route)
                                                       (17.3% logic, 82.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      1.427   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.529ns (0.622ns logic, 1.907ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<16>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.363ns.
--------------------------------------------------------------------------------

Paths for end point d<16> (A14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.363ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.861ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
```

```
                                                     clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                     clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A14.T                net (fanout=32)       1.408   regmd/md_wr_inv
    A14.PAD              Tiotp                 1.847   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    ------------------------------------------------  --------------------------
    Total                                      4.861ns (2.236ns logic, 2.625ns route)
                                                       (46.0% logic, 54.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.319ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.812ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)
```

```
  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A14.T                net (fanout=32)       1.408   regmd/md_wr_inv
    A14.PAD              Tiotp                 1.847   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    -------------------------------------------------  ---------------------------
    Total                                      4.812ns (2.183ns logic, 2.629ns route)
                                                       (45.4% logic, 54.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.217ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.715ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
```

```
    A14.T                net (fanout=32)       1.408   regmd/md_wr_inv
    A14.PAD              Tiotp                 1.847   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    -------------------------------------------------  ---------------------------
    Total                                      4.715ns (2.199ns logic, 2.516ns route)
                                                       (46.6% logic, 53.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<16>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<16> (A14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.631ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.516ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A14.T                net (fanout=32)       0.708   regmd/md_wr_inv
    A14.PAD              Tiotp                 1.139   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    -------------------------------------------------  ---------------------------
    Total                                      2.516ns (1.271ns logic, 1.245ns route)
                                                       (50.5% logic, 49.5% route)
```

```
--------------------------------------------------------------------------------
Delay (fastest paths):  3.624ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.511ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A14.T                net (fanout=32)       0.708   regmd/md_wr_inv
    A14.PAD              Tiotp                 1.139   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    -------------------------------------------------  ---------------------------
    Total                                      2.511ns (1.288ns logic, 1.223ns route)
                                                       (51.3% logic, 48.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.973ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_16 (FF)
  Destination:          d<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.834ns (Levels of Logic = 1)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Clock Path at Fast Process Corner: clk to regmd/md_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y74.CLK     net (fanout=368)      0.580   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_16 to d<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y74.DMUX    Tshcko                0.129   regmd/md<15>
                                                       regmd/md_16
    A14.O                net (fanout=2)        0.566   regmd/md<16>
    A14.PAD              Tioop                 1.139   d<16>
                                                       d_16_IOBUF/OBUFT
                                                       d<16>
    -------------------------------------------------  ---------------------------
    Total                                      1.834ns (1.268ns logic, 0.566ns route)
                                                       (69.1% logic, 30.9% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<16>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.851ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_16 (SLICE_X35Y74.D2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.149ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<16> (PAD)
  Destination:          regmd/md_16 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.990ns (Levels of Logic = 2)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<16> to regmd/md_16
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A14.I                Tiopi                 0.380   d<16>
                                                       d<16>
                                                       d_16_IOBUF/IBUF
    SLICE_X35Y74.D2      net (fanout=1)        1.588   N104
    SLICE_X35Y74.CLK     Tas                   0.022   regmd/md<15>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT81
                                                       regmd/md_16
    -------------------------------------------------  ---------------------------
    Total                                      1.990ns (0.402ns logic, 1.588ns route)
                                                       (20.2% logic, 79.8% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y74.CLK     net (fanout=368)      0.580   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<16>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_16 (SLICE_X35Y74.D2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.846ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<16> (PAD)
  Destination:          regmd/md_16 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.396ns (Levels of Logic = 2)
  Clock Path Delay:     2.525ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<16> to regmd/md_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A14.I                Tiopi                 0.529   d<16>
                                                       d<16>
                                                       d_16_IOBUF/IBUF
    SLICE_X35Y74.D2      net (fanout=1)        1.981   N104
```

```
    SLICE_X35Y74.CLK     Tah         (-Th)     0.114   regmd/md<15>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT81
                                                       regmd/md_16
    ---------------------------------------------------  ---------------------------
    Total                                          2.396ns (0.415ns logic, 1.981ns route)
                                                           (17.3% logic, 82.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y74.CLK     net (fanout=368)      1.423   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                          2.525ns (0.622ns logic, 1.903ns route)
                                                           (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<15>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.277ns.
--------------------------------------------------------------------------------

Paths for end point d<15> (B14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.277ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.775ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
```

```
                                                        clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                        regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                        control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    B14.T                net (fanout=32)       1.325   regmd/md_wr_inv
    B14.PAD              Tiotp                 1.844   d<15>
                                                        d_15_IOBUF/OBUFT
                                                        d<15>
    ---------------------------------------------------  ---------------------------
    Total                                      4.775ns (2.233ns logic, 2.542ns route)
                                                        (46.8% logic, 53.2% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.233ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.726ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
```

```
    ----------------------------------------------------  ------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B14.T                net (fanout=32)       1.325   regmd/md_wr_inv
    B14.PAD              Tiotp                 1.844   d<15>
                                                       d_15_IOBUF/OBUFT
                                                       d<15>
    ----------------------------------------------------  ---------------------------
    Total                                      4.726ns (2.180ns logic, 2.546ns route)
                                                       (46.1% logic, 53.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.131ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.629ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  ------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B14.T                net (fanout=32)       1.325   regmd/md_wr_inv
    B14.PAD              Tiotp                 1.844   d<15>
                                                       d_15_IOBUF/OBUFT
```

```
                                                       d<15>
    ---------------------------------------------  ---------------------------
    Total                                    4.629ns (2.196ns logic, 2.433ns route)
                                                       (47.4% logic, 52.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<15>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<15> (B14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.584ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.469ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B14.T                net (fanout=32)       0.664   regmd/md_wr_inv
    B14.PAD              Tiotp                 1.136   d<15>
                                                       d_15_IOBUF/OBUFT
                                                       d<15>
    ---------------------------------------------  ---------------------------
    Total                                      2.469ns (1.268ns logic, 1.201ns route)
                                                       (51.4% logic, 48.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.577ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
```

```
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.464ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B14.T                net (fanout=32)       0.664   regmd/md_wr_inv
    B14.PAD              Tiotp                 1.136   d<15>
                                                       d_15_IOBUF/OBUFT
                                                       d<15>
    -------------------------------------------------  ---------------------------
    Total                                      2.464ns (1.285ns logic, 1.179ns route)
                                                       (52.2% logic, 47.8% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.979ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_15 (FF)
  Destination:          d<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.840ns (Levels of Logic = 1)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_15
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y74.CLK     net (fanout=368)      0.580   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_15 to d<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X35Y74.DQ      Tcko                  0.098   regmd/md<15>
                                                       regmd/md_15
    B14.O                net (fanout=2)        0.606   regmd/md<15>
    B14.PAD              Tioop                 1.136   d<15>
                                                       d_15_IOBUF/OBUFT
                                                       d<15>
    ---------------------------------------------------  ---------------------------
    Total                                      1.840ns (1.234ns logic, 0.606ns route)
                                                       (67.1% logic, 32.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<15>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.887ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_15 (SLICE_X35Y74.D5), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.113ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<15> (PAD)
  Destination:          regmd/md_15 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.026ns (Levels of Logic = 2)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<15> to regmd/md_15
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
```

```
    B14.I               Tiopi                 0.377   d<15>
                                                      d<15>
                                                      d_15_IOBUF/IBUF
    SLICE_X35Y74.D5     net (fanout=1)        1.620   N105
    SLICE_X35Y74.CLK    Tas                   0.029   regmd/md<15>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT71
                                                      regmd/md_15
    ------------------------------------------------  --------------------------
    Total                                     2.026ns (0.406ns logic, 1.620ns route)
                                                      (20.0% logic, 80.0% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_15
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I               Tiopi                 0.320   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0    net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O     Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                      clk_BUFGP/BUFG
    SLICE_X35Y74.CLK    net (fanout=368)      0.580   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                     1.164ns (0.353ns logic, 0.811ns route)
                                                      (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<15>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_15 (SLICE_X35Y74.D5), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.899ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<15> (PAD)
  Destination:          regmd/md_15 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.449ns (Levels of Logic = 2)
  Clock Path Delay:     2.525ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<15> to regmd/md_15
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    B14.I               Tiopi                 0.526   d<15>
                                                      d<15>
                                                      d_15_IOBUF/IBUF
    SLICE_X35Y74.D5     net (fanout=1)        2.001   N105
    SLICE_X35Y74.CLK    Tah         (-Th)     0.078   regmd/md<15>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT71
```

```
                                                       regmd/md_15
    ------------------------------------------------  --------------------------
    Total                                          2.449ns (0.448ns logic, 2.001ns route)
                                                           (18.3% logic, 81.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_15
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y74.CLK     net (fanout=368)      1.423   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                          2.525ns (0.622ns logic, 1.903ns route)
                                                           (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<14>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.456ns.
--------------------------------------------------------------------------------

Paths for end point d<14> (D14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.456ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.954ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  --------------------------
```

```
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D14.T                net (fanout=32)       1.521   regmd/md_wr_inv
    D14.PAD              Tiotp                 1.827   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    -------------------------------------------------  ---------------------------
    Total                                     4.954ns (2.216ns logic, 2.738ns route)
                                                      (44.7% logic, 55.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.412ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.905ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.482ns (0.622ns logic, 1.860ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
```

```
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D14.T                net (fanout=32)       1.521   regmd/md_wr_inv
    D14.PAD              Tiotp                 1.827   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    ------------------------------------------------  ---------------------------
    Total                                      4.905ns (2.163ns logic, 2.742ns route)
                                                       (44.1% logic, 55.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.310ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.808ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D14.T                net (fanout=32)       1.521   regmd/md_wr_inv
    D14.PAD              Tiotp                 1.827   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    ------------------------------------------------  ---------------------------
    Total                                      4.808ns (2.179ns logic, 2.629ns route)
```

```
                                                        (45.3% logic, 54.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<14>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<14> (D14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.676ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.561ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D14.T                net (fanout=32)       0.771   regmd/md_wr_inv
    D14.PAD              Tiotp                 1.121   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    -------------------------------------------------  ---------------------------
    Total                                      2.561ns (1.253ns logic, 1.308ns route)
                                                       (48.9% logic, 51.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.669ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.556ns (Levels of Logic = 2)
```

```
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D14.T                net (fanout=32)       0.771   regmd/md_wr_inv
    D14.PAD              Tiotp                 1.121   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    -------------------------------------------------  ---------------------------
    Total                                      2.556ns (1.270ns logic, 1.286ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.956ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_14 (FF)
  Destination:          d<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.816ns (Levels of Logic = 1)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
```

```
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      0.581   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_14 to d<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y78.DMUX    Tshcko                0.129   regmd/md<13>
                                                       regmd/md_14
    D14.O                net (fanout=2)        0.566   regmd/md<14>
    D14.PAD              Tioop                 1.121   d<14>
                                                       d_14_IOBUF/OBUFT
                                                       d<14>
    ------------------------------------------------  --------------------------
    Total                                      1.816ns (1.250ns logic, 0.566ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<14>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.805ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_14 (SLICE_X35Y78.D4), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.195ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<14> (PAD)
  Destination:          regmd/md_14 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.945ns (Levels of Logic = 2)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<14> to regmd/md_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D14.I                Tiopi                 0.360   d<14>
                                                       d<14>
                                                       d_14_IOBUF/IBUF
```

```
    SLICE_X35Y78.D4      net (fanout=1)        1.558   N106
    SLICE_X35Y78.CLK     Tas                   0.027   regmd/md<13>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT61
                                                       regmd/md_14
    ---------------------------------------------  ---------------------------
    Total                                      1.945ns (0.387ns logic, 1.558ns route)
                                                       (19.9% logic, 80.1% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      0.581   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                      1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<14>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_14 (SLICE_X35Y78.D4), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.861ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<14> (PAD)
  Destination:          regmd/md_14 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.412ns (Levels of Logic = 2)
  Clock Path Delay:     2.526ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<14> to regmd/md_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D14.I                Tiopi                 0.511   d<14>
                                                       d<14>
                                                       d_14_IOBUF/IBUF
    SLICE_X35Y78.D4      net (fanout=1)        2.015   N106
    SLICE_X35Y78.CLK     Tah         (-Th)     0.114   regmd/md<13>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT61
                                                       regmd/md_14
    ---------------------------------------------  ---------------------------
    Total                                      2.412ns (0.397ns logic, 2.015ns route)
```

```
                                                        (16.5% logic, 83.5% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      1.424   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.526ns (0.622ns logic, 1.904ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<13>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.365ns.
--------------------------------------------------------------------------------

Paths for end point d<13> (E14.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.365ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.863ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)
```

```
  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E14.T                net (fanout=32)       1.438   regmd/md_wr_inv
    E14.PAD              Tiotp                 1.819   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                      4.863ns (2.208ns logic, 2.655ns route)
                                                       (45.4% logic, 54.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.321ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.814ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
```

```
    E14.T                net (fanout=32)       1.438   regmd/md_wr_inv
    E14.PAD              Tiotp                 1.819   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                      4.814ns (2.155ns logic, 2.659ns route)
                                                       (44.8% logic, 55.2% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.219ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.717ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E14.T                net (fanout=32)       1.438   regmd/md_wr_inv
    E14.PAD              Tiotp                 1.819   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                      4.717ns (2.171ns logic, 2.546ns route)
                                                       (46.0% logic, 54.0% route)

--------------------------------------------------------------------------------
```

```
Fastest Paths: COMP "d<13>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<13> (E14.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.626ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.511ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)     0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                 0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)      0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                 0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E14.T                net (fanout=32)      0.727   regmd/md_wr_inv
    E14.PAD              Tiotp                1.115   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                     2.511ns (1.247ns logic, 1.264ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.619ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.506ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E14.T                net (fanout=32)       0.727   regmd/md_wr_inv
    E14.PAD              Tiotp                 1.115   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                      2.506ns (1.264ns logic, 1.242ns route)
                                                       (50.4% logic, 49.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.959ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_13 (FF)
  Destination:          d<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.819ns (Levels of Logic = 1)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      0.581   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_13 to d<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y78.DQ      Tcko                  0.098   regmd/md<13>
                                                       regmd/md_13
    E14.O                net (fanout=2)        0.606   regmd/md<13>
    E14.PAD              Tioop                 1.115   d<13>
                                                       d_13_IOBUF/OBUFT
                                                       d<13>
    -------------------------------------------------  ---------------------------
    Total                                      1.819ns (1.213ns logic, 0.606ns route)
                                                       (66.7% logic, 33.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<13>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.881ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_13 (SLICE_X35Y78.D2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.119ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<13> (PAD)
  Destination:          regmd/md_13 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.021ns (Levels of Logic = 2)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<13> to regmd/md_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E14.I                Tiopi                 0.352   d<13>
                                                       d<13>
                                                       d_13_IOBUF/IBUF
    SLICE_X35Y78.D2      net (fanout=1)        1.640   N107
    SLICE_X35Y78.CLK     Tas                   0.029   regmd/md<13>
```

```
regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT51
                                                       regmd/md_13
    -------------------------------------------------  ---------------------------
    Total                                    2.021ns (0.381ns logic, 1.640ns route)
                                                       (18.9% logic, 81.1% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      0.581   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                    1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<13>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_13 (SLICE_X35Y78.D2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.919ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<13> (PAD)
  Destination:          regmd/md_13 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.470ns (Levels of Logic = 2)
  Clock Path Delay:     2.526ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<13> to regmd/md_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E14.I                Tiopi                 0.505   d<13>
                                                       d<13>
                                                       d_13_IOBUF/IBUF
    SLICE_X35Y78.D2      net (fanout=1)        2.043   N107
    SLICE_X35Y78.CLK     Tah         (-Th)     0.078   regmd/md<13>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT51
                                                       regmd/md_13
    -------------------------------------------------  ---------------------------
    Total                                    2.470ns (0.427ns logic, 2.043ns route)
                                                       (17.3% logic, 82.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_13
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y78.CLK     net (fanout=368)      1.424   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.526ns (0.622ns logic, 1.904ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<12>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.346ns.
--------------------------------------------------------------------------------

Paths for end point d<12> (C15.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.346ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.844ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  ------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C15.T                net (fanout=32)       1.400   regmd/md_wr_inv
    C15.PAD              Tiotp                 1.838   d<12>
                                                       d_12_IOBUF/OBUFT
                                                       d<12>
    ----------------------------------------------------  ---------------------------
    Total                                      4.844ns (2.227ns logic, 2.617ns route)
                                                       (46.0% logic, 54.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.302ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.795ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  ------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C15.T                net (fanout=32)       1.400   regmd/md_wr_inv
    C15.PAD              Tiotp                 1.838   d<12>
                                                       d_12_IOBUF/OBUFT
```

```
                                                       d<12>
    ---------------------------------------------  ---------------------------
    Total                                    4.795ns (2.174ns logic, 2.621ns route)
                                                       (45.3% logic, 54.7% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.200ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.698ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)     1.375   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                 0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)      0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                 0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)       0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                 0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C15.T                net (fanout=32)      1.400   regmd/md_wr_inv
    C15.PAD              Tiotp                1.838   d<12>
                                                       d_12_IOBUF/OBUFT
                                                       d<12>
    ---------------------------------------------  ---------------------------
    Total                                     4.698ns (2.190ns logic, 2.508ns route)
                                                       (46.6% logic, 53.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<12>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------
```

```
Paths for end point d<12> (C15.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.611ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.496ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C15.T                net (fanout=32)       0.696   regmd/md_wr_inv
    C15.PAD              Tiotp                 1.131   d<12>
                                                       d_12_IOBUF/OBUFT
                                                       d<12>
    -------------------------------------------------  ---------------------------
    Total                                      2.496ns (1.263ns logic, 1.233ns route)
                                                       (50.6% logic, 49.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.604ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.491ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C15.T                net (fanout=32)       0.696   regmd/md_wr_inv
    C15.PAD              Tiotp                 1.131   d<12>
                                                       d_12_IOBUF/OBUFT
                                                       d<12>
    -------------------------------------------------  ---------------------------
    Total                                      2.491ns (1.280ns logic, 1.211ns route)
                                                       (51.4% logic, 48.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.961ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_12 (FF)
  Destination:          d<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.821ns (Levels of Logic = 1)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      0.581   clk_BUFGP
```

```
    ------------------------------------------------  --------------------------
    Total                                     1.165ns (0.353ns logic, 0.812ns route)
                                                      (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_12 to d<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y76.AMUX    Tshcko                0.130   regmd/md<11>
                                                       regmd/md_12
    C15.O                net (fanout=2)        0.560   regmd/md<12>
    C15.PAD              Tioop                 1.131   d<12>
                                                       d_12_IOBUF/OBUFT
                                                       d<12>
    ------------------------------------------------  --------------------------
    Total                                     1.821ns (1.261ns logic, 0.560ns route)
                                                      (69.2% logic, 30.8% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<12>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.890ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_12 (SLICE_X35Y76.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.110ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<12> (PAD)
  Destination:          regmd/md_12 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.030ns (Levels of Logic = 2)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<12> to regmd/md_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    C15.I                Tiopi                 0.371   d<12>
                                                       d<12>
                                                       d_12_IOBUF/IBUF
    SLICE_X35Y76.A2      net (fanout=1)        1.635   N108
    SLICE_X35Y76.CLK     Tas                   0.024   regmd/md<11>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT41
                                                       regmd/md_12
    ------------------------------------------------  --------------------------
```

```
    Total                                     2.030ns (0.395ns logic, 1.635ns route)
                                                      (19.5% logic, 80.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      0.581   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.165ns (0.353ns logic, 0.812ns route)
                                                      (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<12>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_12 (SLICE_X35Y76.A2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.896ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<12> (PAD)
  Destination:          regmd/md_12 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.447ns (Levels of Logic = 2)
  Clock Path Delay:     2.526ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<12> to regmd/md_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C15.I                Tiopi                 0.521   d<12>
                                                       d<12>
                                                       d_12_IOBUF/IBUF
    SLICE_X35Y76.A2      net (fanout=1)        2.035   N108
    SLICE_X35Y76.CLK     Tah         (-Th)     0.109   regmd/md<11>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT41
                                                       regmd/md_12
    -------------------------------------------------  ---------------------------
    Total                                     2.447ns (0.412ns logic, 2.035ns route)
                                                      (16.8% logic, 83.2% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      1.424   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.526ns (0.622ns logic, 1.904ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<11>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.440ns.
--------------------------------------------------------------------------------

Paths for end point d<11> (B15.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.440ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.938ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
```

```
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B15.T                net (fanout=32)       1.488   regmd/md_wr_inv
    B15.PAD              Tiotp                 1.844   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    ------------------------------------------------  --------------------------
    Total                                      4.938ns (2.233ns logic, 2.705ns route)
                                                       (45.2% logic, 54.8% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.396ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.889ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B15.T                net (fanout=32)       1.488   regmd/md_wr_inv
    B15.PAD              Tiotp                 1.844   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    ------------------------------------------------  --------------------------
    Total                                      4.889ns (2.180ns logic, 2.709ns route)
```

```
                                                          (44.6% logic, 55.4% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.294ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.792ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B15.T                net (fanout=32)       1.488   regmd/md_wr_inv
    B15.PAD              Tiotp                 1.844   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    -------------------------------------------------  ---------------------------
    Total                                      4.792ns (2.196ns logic, 2.596ns route)
                                                       (45.8% logic, 54.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<11>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<11> (B15.PAD), 9 paths
--------------------------------------------------------------------------------
```

```
Delay (fastest paths):  3.665ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.550ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B15.T                net (fanout=32)       0.745   regmd/md_wr_inv
    B15.PAD              Tiotp                 1.136   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    -------------------------------------------------  ---------------------------
    Total                                      2.550ns (1.268ns logic, 1.282ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.658ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.545ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B15.T                net (fanout=32)       0.745   regmd/md_wr_inv
    B15.PAD              Tiotp                 1.136   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    -------------------------------------------------  ---------------------------
    Total                                      2.545ns (1.285ns logic, 1.260ns route)
                                                       (50.5% logic, 49.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.980ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_11 (FF)
  Destination:          d<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.840ns (Levels of Logic = 1)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      0.581   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)
```

```
  Minimum Data Path at Fast Process Corner: regmd/md_11 to d<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y76.AQ      Tcko                  0.098   regmd/md<11>
                                                       regmd/md_11
    B15.O                net (fanout=2)        0.606   regmd/md<11>
    B15.PAD              Tioop                 1.136   d<11>
                                                       d_11_IOBUF/OBUFT
                                                       d<11>
    -------------------------------------------------  ---------------------------
    Total                                      1.840ns (1.234ns logic, 0.606ns route)
                                                       (67.1% logic, 32.9% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<11>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.860ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_11 (SLICE_X35Y76.A1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.140ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<11> (PAD)
  Destination:          regmd/md_11 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.000ns (Levels of Logic = 2)
  Clock Path Delay:     1.165ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<11> to regmd/md_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B15.I                Tiopi                 0.377   d<11>
                                                       d<11>
                                                       d_11_IOBUF/IBUF
    SLICE_X35Y76.A1      net (fanout=1)        1.592   N109
    SLICE_X35Y76.CLK     Tas                   0.031   regmd/md<11>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT33
                                                       regmd/md_11
    -------------------------------------------------  ---------------------------
    Total                                      2.000ns (0.408ns logic, 1.592ns route)
                                                       (20.4% logic, 79.6% route)
```

```
  Minimum Clock Path at Fast Process Corner: clk to regmd/md_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      0.581   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.165ns (0.353ns logic, 0.812ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<11>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_11 (SLICE_X35Y76.A1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.853ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<11> (PAD)
  Destination:          regmd/md_11 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.404ns (Levels of Logic = 2)
  Clock Path Delay:     2.526ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<11> to regmd/md_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B15.I                Tiopi                 0.526   d<11>
                                                       d<11>
                                                       d_11_IOBUF/IBUF
    SLICE_X35Y76.A1      net (fanout=1)        1.953   N109
    SLICE_X35Y76.CLK     Tah         (-Th)     0.075   regmd/md<11>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT33
                                                       regmd/md_11
    -------------------------------------------------  ---------------------------
    Total                                      2.404ns (0.451ns logic, 1.953ns route)
                                                       (18.8% logic, 81.2% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y76.CLK     net (fanout=368)      1.424   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.526ns (0.622ns logic, 1.904ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<10>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.086ns.
--------------------------------------------------------------------------------

Paths for end point d<10> (C17.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.086ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.584ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
```

```
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C17.T                net (fanout=32)       1.123   regmd/md_wr_inv
    C17.PAD              Tiotp                 1.855   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    -------------------------------------------------  ---------------------------
    Total                                      4.584ns (2.244ns logic, 2.340ns route)
                                                       (49.0% logic, 51.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.042ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.535ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C17.T                net (fanout=32)       1.123   regmd/md_wr_inv
    C17.PAD              Tiotp                 1.855   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    -------------------------------------------------  ---------------------------
    Total                                      4.535ns (2.191ns logic, 2.344ns route)
                                                       (48.3% logic, 51.7% route)

--------------------------------------------------------------------------------
```

```
Slack (slowest paths):  -2.940ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.438ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C17.T                net (fanout=32)       1.123   regmd/md_wr_inv
    C17.PAD              Tiotp                 1.855   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    -------------------------------------------------  ---------------------------
    Total                                      4.438ns (2.207ns logic, 2.231ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<10>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<10> (C17.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.492ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<10> (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.377ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C17.T                net (fanout=32)       0.563   regmd/md_wr_inv
    C17.PAD              Tiotp                 1.145   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    -------------------------------------------------  ---------------------------
    Total                                      2.377ns (1.277ns logic, 1.100ns route)
                                                       (53.7% logic, 46.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.485ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.372ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C17.T                net (fanout=32)       0.563   regmd/md_wr_inv
    C17.PAD              Tiotp                 1.145   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    ------------------------------------------------  --------------------------
    Total                                      2.372ns (1.294ns logic, 1.078ns route)
                                                       (54.6% logic, 45.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.967ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_10 (FF)
  Destination:          d<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.835ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_10 to d<10>
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X35Y56.AMUX    Tshcko                0.130   regmd/md<5>
                                                       regmd/md_10
    C17.O                net (fanout=2)        0.560   regmd/md<10>
    C17.PAD              Tioop                 1.145   d<10>
                                                       d_10_IOBUF/OBUFT
                                                       d<10>
    ---------------------------------------------  -------------------------
    Total                                      1.835ns (1.275ns logic, 0.560ns route)
                                                       (69.5% logic, 30.5% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<10>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.869ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_10 (SLICE_X35Y56.A1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.131ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<10> (PAD)
  Destination:          regmd/md_10 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.001ns (Levels of Logic = 2)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<10> to regmd/md_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    C17.I                Tiopi                 0.388   d<10>
                                                       d<10>
                                                       d_10_IOBUF/IBUF
    SLICE_X35Y56.A1      net (fanout=1)        1.590   N110
    SLICE_X35Y56.CLK     Tas                   0.023   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT210
                                                       regmd/md_10
    ---------------------------------------------  -------------------------
    Total                                      2.001ns (0.411ns logic, 1.590ns route)
                                                       (20.5% logic, 79.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<10>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_10 (SLICE_X35Y56.A1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.842ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<10> (PAD)
  Destination:          regmd/md_10 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.377ns (Levels of Logic = 2)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<10> to regmd/md_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    C17.I                Tiopi                 0.535   d<10>
                                                       d<10>
                                                       d_10_IOBUF/IBUF
    SLICE_X35Y56.A1      net (fanout=1)        1.952   N110
    SLICE_X35Y56.CLK     Tah         (-Th)     0.110   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT210
                                                       regmd/md_10
    ----------------------------------------------------  ---------------------------
    Total                                      2.377ns (0.425ns logic, 1.952ns route)
                                                       (17.9% logic, 82.1% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
```

```
    SLICE_X35Y56.CLK     net (fanout=368)      1.408   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<9>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.323ns.
--------------------------------------------------------------------------------

Paths for end point d<9> (D15.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.323ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.821ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
```

```
    D15.T                net (fanout=32)       1.379   regmd/md_wr_inv
    D15.PAD              Tiotp                 1.836   d<9>
                                                       d_9_IOBUF/OBUFT
                                                       d<9>
    -------------------------------------------------  ---------------------------
    Total                                      4.821ns (2.225ns logic, 2.596ns route)
                                                       (46.2% logic, 53.8% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.279ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.772ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D15.T                net (fanout=32)       1.379   regmd/md_wr_inv
    D15.PAD              Tiotp                 1.836   d<9>
                                                       d_9_IOBUF/OBUFT
                                                       d<9>
    -------------------------------------------------  ---------------------------
    Total                                      4.772ns (2.172ns logic, 2.600ns route)
                                                       (45.5% logic, 54.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.177ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
```

```
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.675ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)     1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                 0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)      0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                 0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)       0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                 0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D15.T                net (fanout=32)      1.379   regmd/md_wr_inv
    D15.PAD              Tiotp                1.836   d<9>
                                                       d_9_IOBUF/OBUFT
                                                       d<9>
    -------------------------------------------------  ---------------------------
    Total                                     4.675ns (2.188ns logic, 2.487ns route)
                                                       (46.8% logic, 53.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<9>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<9> (D15.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.599ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.484ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
```

```
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    D15.T                net (fanout=32)       0.686   regmd/md_wr_inv
    D15.PAD              Tiotp                 1.129   d<9>
                                                       d_9_IOBUF/OBUFT
                                                       d<9>
    -------------------------------------------------  ---------------------------
    Total                                      2.484ns (1.261ns logic, 1.223ns route)
                                                       (50.8% logic, 49.2% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.592ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.479ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
```

```
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                        (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                        regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    D15.T                net (fanout=32)       0.686   regmd/md_wr_inv
    D15.PAD              Tiotp                 1.129   d<9>
                                                        d_9_IOBUF/OBUFT
                                                        d<9>
    -------------------------------------------------  ---------------------------
    Total                                      2.479ns (1.278ns logic, 1.201ns route)
                                                        (51.6% logic, 48.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.958ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_9 (FF)
  Destination:          d<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.819ns (Levels of Logic = 1)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      0.580   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                        (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_9 to d<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y73.AMUX    Tshcko                0.130   regmd/md<8>
```

```
                                                       regmd/md_9
    D15.O                net (fanout=2)        0.560   regmd/md<9>
    D15.PAD              Tioop                 1.129   d<9>
                                                       d_9_IOBUF/OBUFT
                                                       d<9>
    ------------------------------------------------  ---------------------------
    Total                                      1.819ns (1.259ns logic, 0.560ns route)
                                                       (69.2% logic, 30.8% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<9>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.819ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_9 (SLICE_X35Y73.A1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.181ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<9> (PAD)
  Destination:          regmd/md_9 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.958ns (Levels of Logic = 2)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<9> to regmd/md_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D15.I                Tiopi                 0.369   d<9>
                                                       d<9>
                                                       d_9_IOBUF/IBUF
    SLICE_X35Y73.A1      net (fanout=1)        1.566   N111
    SLICE_X35Y73.CLK     Tas                   0.023   regmd/md<8>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT321
                                                       regmd/md_9
    ------------------------------------------------  ---------------------------
    Total                                      1.958ns (0.392ns logic, 1.566ns route)
                                                       (20.0% logic, 80.0% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
```

```
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      0.580   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<9>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_9 (SLICE_X35Y73.A1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.805ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<9> (PAD)
  Destination:          regmd/md_9 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.354ns (Levels of Logic = 2)
  Clock Path Delay:     2.524ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<9> to regmd/md_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D15.I                Tiopi                 0.519   d<9>
                                                       d<9>
                                                       d_9_IOBUF/IBUF
    SLICE_X35Y73.A1      net (fanout=1)        1.945   N111
    SLICE_X35Y73.CLK     Tah         (-Th)     0.110   regmd/md<8>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT321
                                                       regmd/md_9
    -------------------------------------------------  ---------------------------
    Total                                      2.354ns (0.409ns logic, 1.945ns route)
                                                       (17.4% logic, 82.6% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      1.422   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.524ns (0.622ns logic, 1.902ns route)
```

```
                                                        (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<8>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.229ns.
--------------------------------------------------------------------------------

Paths for end point d<8> (E15.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.229ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.727ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E15.T                net (fanout=32)       1.291   regmd/md_wr_inv
    E15.PAD              Tiotp                 1.830   d<8>
                                                       d_8_IOBUF/OBUFT
```

```
                                                       d<8>
    ---------------------------------------------  --------------------------
    Total                                     4.727ns (2.219ns logic, 2.508ns route)
                                                      (46.9% logic, 53.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.185ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.678ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    ---------------------------------------------  --------------------------
    Total                                     2.482ns (0.622ns logic, 1.860ns route)
                                                      (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E15.T                net (fanout=32)       1.291   regmd/md_wr_inv
    E15.PAD              Tiotp                 1.830   d<8>
                                                       d_8_IOBUF/OBUFT
                                                       d<8>
    ---------------------------------------------  --------------------------
    Total                                     4.678ns (2.166ns logic, 2.512ns route)
                                                      (46.3% logic, 53.7% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.083ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
```

```
  Data Path Delay:      4.581ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E15.T                net (fanout=32)       1.291   regmd/md_wr_inv
    E15.PAD              Tiotp                 1.830   d<8>
                                                       d_8_IOBUF/OBUFT
                                                       d<8>
    -------------------------------------------------  ---------------------------
    Total                                      4.581ns (2.182ns logic, 2.399ns route)
                                                       (47.6% logic, 52.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<8>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<8> (E15.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.545ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.430ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E15.T                net (fanout=32)       0.637   regmd/md_wr_inv
    E15.PAD              Tiotp                 1.124   d<8>
                                                       d_8_IOBUF/OBUFT
                                                       d<8>
    -------------------------------------------------  ---------------------------
    Total                                      2.430ns (1.256ns logic, 1.174ns route)
                                                       (51.7% logic, 48.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.538ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.425ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
```

```
                                                        clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E15.T                net (fanout=32)       0.637   regmd/md_wr_inv
    E15.PAD              Tiotp                 1.124   d<8>
                                                       d_8_IOBUF/OBUFT
                                                       d<8>
    ------------------------------------------------  --------------------------
    Total                                      2.425ns (1.273ns logic, 1.152ns route)
                                                       (52.5% logic, 47.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.964ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_8 (FF)
  Destination:          d<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.825ns (Levels of Logic = 1)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      0.580   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Data Path at Fast Process Corner: regmd/md_8 to d<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X35Y73.AQ      Tcko                  0.098   regmd/md<8>
                                                       regmd/md_8
    E15.O                net (fanout=2)        0.603   regmd/md<8>
    E15.PAD              Tioop                 1.124   d<8>
```

```
                                                       d_8_IOBUF/OBUFT
                                                       d<8>
    ---------------------------------------------  ---------------------------
    Total                                    1.825ns (1.222ns logic, 0.603ns route)
                                                       (67.0% logic, 33.0% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<8>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.955ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_8 (SLICE_X35Y73.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.045ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<8> (PAD)
  Destination:          regmd/md_8 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.094ns (Levels of Logic = 2)
  Clock Path Delay:     1.164ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<8> to regmd/md_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    E15.I                Tiopi                 0.363   d<8>
                                                       d<8>
                                                       d_8_IOBUF/IBUF
    SLICE_X35Y73.A2      net (fanout=1)        1.700   N112
    SLICE_X35Y73.CLK     Tas                   0.031   regmd/md<8>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT311
                                                       regmd/md_8
    ---------------------------------------------  ---------------------------
    Total                                    2.094ns (0.394ns logic, 1.700ns route)
                                                       (18.8% logic, 81.2% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
```

```
                                                       clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      0.580   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.164ns (0.353ns logic, 0.811ns route)
                                                       (30.3% logic, 69.7% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<8>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_8 (SLICE_X35Y73.A2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.998ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<8> (PAD)
  Destination:          regmd/md_8 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.547ns (Levels of Logic = 2)
  Clock Path Delay:     2.524ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<8> to regmd/md_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    E15.I                Tiopi                 0.514   d<8>
                                                       d<8>
                                                       d_8_IOBUF/IBUF
    SLICE_X35Y73.A2      net (fanout=1)        2.108   N112
    SLICE_X35Y73.CLK     Tah         (-Th)     0.075   regmd/md<8>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT311
                                                       regmd/md_8
    ---------------------------------------------------  ---------------------------
    Total                                      2.547ns (0.439ns logic, 2.108ns route)
                                                       (17.2% logic, 82.8% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y73.CLK     net (fanout=368)      1.422   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.524ns (0.622ns logic, 1.902ns route)
                                                       (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------
```

```
==============================================================================
Timing constraint: COMP "d<7>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.136ns.
------------------------------------------------------------------------------

Paths for end point d<7> (B16.PAD), 9 paths
------------------------------------------------------------------------------
Slack (slowest paths):  -3.136ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.634ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B16.T                net (fanout=32)       1.176   regmd/md_wr_inv
    B16.PAD              Tiotp                 1.852   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
    Total                                      4.634ns (2.241ns logic, 2.393ns route)
```

```
                                                          (48.4% logic, 51.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.092ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.585ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B16.T                net (fanout=32)       1.176   regmd/md_wr_inv
    B16.PAD              Tiotp                 1.852   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
    Total                                      4.585ns (2.188ns logic, 2.397ns route)
                                                       (47.7% logic, 52.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.990ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.488ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B16.T                net (fanout=32)       1.176   regmd/md_wr_inv
    B16.PAD              Tiotp                 1.852   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
    Total                                      4.488ns (2.204ns logic, 2.284ns route)
                                                       (49.1% logic, 50.9% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<7>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<7> (B16.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.499ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.384ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B16.T                net (fanout=32)       0.572   regmd/md_wr_inv
    B16.PAD              Tiotp                 1.143   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
    Total                                      2.384ns (1.275ns logic, 1.109ns route)
                                                       (53.5% logic, 46.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.492ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.379ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
```

```
    Total                                     1.138ns (0.353ns logic, 0.785ns route)
                                                      (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B16.T                net (fanout=32)       0.572   regmd/md_wr_inv
    B16.PAD              Tiotp                 1.143   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
    Total                                     2.379ns (1.292ns logic, 1.087ns route)
                                                      (54.3% logic, 45.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.928ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_7 (FF)
  Destination:          d<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.784ns (Levels of Logic = 1)
  Clock Path Delay:     1.169ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      0.585   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.169ns (0.353ns logic, 0.816ns route)
                                                      (30.2% logic, 69.8% route)

  Minimum Data Path at Fast Process Corner: regmd/md_7 to d<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y64.CMUX    Tshcko                0.147   regmd/md<17>
                                                       regmd/md_7
    B16.O                net (fanout=2)        0.494   regmd/md<7>
    B16.PAD              Tioop                 1.143   d<7>
                                                       d_7_IOBUF/OBUFT
                                                       d<7>
    -------------------------------------------------  ---------------------------
```

```
    Total                                     1.784ns (1.290ns logic, 0.494ns route)
                                                      (72.3% logic, 27.7% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<7>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.795ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_7 (SLICE_X36Y64.C2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.205ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<7> (PAD)
  Destination:          regmd/md_7 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.939ns (Levels of Logic = 2)
  Clock Path Delay:     1.169ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<7> to regmd/md_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B16.I                Tiopi                 0.385   d<7>
                                                       d<7>
                                                       d_7_IOBUF/IBUF
    SLICE_X36Y64.C2      net (fanout=1)        1.542   N113
    SLICE_X36Y64.CLK     Tas                   0.012   regmd/md<17>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT301
                                                       regmd/md_7
    -------------------------------------------------  ---------------------------
    Total                                     1.939ns (0.397ns logic, 1.542ns route)
                                                      (20.5% logic, 79.5% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      0.585   clk_BUFGP
    -------------------------------------------------  ---------------------------
```

```
    Total                                     1.169ns (0.353ns logic, 0.816ns route)
                                                      (30.2% logic, 69.8% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<7>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_7 (SLICE_X36Y64.C2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.802ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<7> (PAD)
  Destination:          regmd/md_7 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.356ns (Levels of Logic = 2)
  Clock Path Delay:     2.529ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<7> to regmd/md_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B16.I                Tiopi                 0.533   d<7>
                                                       d<7>
                                                       d_7_IOBUF/IBUF
    SLICE_X36Y64.C2      net (fanout=1)        1.964   N113
    SLICE_X36Y64.CLK     Tah         (-Th)     0.141   regmd/md<17>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT301
                                                       regmd/md_7
    -------------------------------------------------  ---------------------------
    Total                                     2.356ns (0.392ns logic, 1.964ns route)
                                                      (16.6% logic, 83.4% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X36Y64.CLK     net (fanout=368)      1.427   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.529ns (0.622ns logic, 1.907ns route)
                                                      (24.6% logic, 75.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<6>" OFFSET = OUT 4 ns AFTER COMP "clk";
```

For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.137ns.

Paths for end point d<6> (C16.PAD), 9 paths

Slack (slowest paths): -3.137ns (requirement - (clock arrival + clock path + data path + uncertainty))
  Source: regir/ir_28 (FF)
  Destination: d<6> (PAD)
  Source Clock: clk_BUFGP rising at 0.000ns
  Requirement: 4.000ns
  Data Path Delay: 4.635ns (Levels of Logic = 3)
  Clock Path Delay: 2.477ns (Levels of Logic = 2)
  Clock Uncertainty: 0.025ns

  Clock Uncertainty: 0.025ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ): 0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):   0.000ns
    Phase Error (PE):   0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location   Delay type   Delay(ns) Physical Resource
                                                       Logical Resource(s)
    --- -------------------
    D12.I   Tiopi   0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0   net (fanout=1)   0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O   Tbgcko_O   0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK   net (fanout=368)   1.375   clk_BUFGP
    --- ---------------------------
    Total   2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<6>
    Location   Delay type   Delay(ns) Physical Resource
                                                       Logical Resource(s)
    --- -------------------
    SLICE_X24Y61.BQ   Tcko   0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5   net (fanout=39)   0.360   regir/ir<28>
    SLICE_X25Y61.C   Tilo   0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6   net (fanout=3)   0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D   Tilo   0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C16.T   net (fanout=32)   1.178   regmd/md_wr_inv
    C16.PAD   Tiotp   1.851   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    --- ---------------------------
    Total   4.635ns (2.240ns logic, 2.395ns route)
                                                       (48.3% logic, 51.7% route)

```
Slack (slowest paths):  -3.093ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.586ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C16.T                net (fanout=32)       1.178   regmd/md_wr_inv
    C16.PAD              Tiotp                 1.851   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    -------------------------------------------------  ---------------------------
    Total                                      4.586ns (2.187ns logic, 2.399ns route)
                                                       (47.7% logic, 52.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.991ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.489ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C16.T                net (fanout=32)       1.178   regmd/md_wr_inv
    C16.PAD              Tiotp                 1.851   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    -------------------------------------------------  ---------------------------
    Total                                      4.489ns (2.203ns logic, 2.286ns route)
                                                       (49.1% logic, 50.9% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<6>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<6> (C16.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.514ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.399ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C16.T                net (fanout=32)       0.588   regmd/md_wr_inv
    C16.PAD              Tiotp                 1.142   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    -------------------------------------------------  ---------------------------
    Total                                      2.399ns (1.274ns logic, 1.125ns route)
                                                       (53.1% logic, 46.9% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.507ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.394ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)
```

```
  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C16.T                net (fanout=32)       0.588   regmd/md_wr_inv
    C16.PAD              Tiotp                 1.142   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    -------------------------------------------------  ---------------------------
    Total                                      2.394ns (1.291ns logic, 1.103ns route)
                                                       (53.9% logic, 46.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.968ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_6 (FF)
  Destination:          d<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.836ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_6 to d<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y56.DMUX    Tshcko                0.129   regmd/md<5>
                                                       regmd/md_6
    C16.O                net (fanout=2)        0.565   regmd/md<6>
    C16.PAD              Tioop                 1.142   d<6>
                                                       d_6_IOBUF/OBUFT
                                                       d<6>
    -------------------------------------------------  ---------------------------
    Total                                      1.836ns (1.271ns logic, 0.565ns route)
                                                       (69.2% logic, 30.8% route)
```

```
--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<6>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.786ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_6 (SLICE_X35Y56.D1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.214ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<6> (PAD)
  Destination:          regmd/md_6 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.918ns (Levels of Logic = 2)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<6> to regmd/md_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C16.I                Tiopi                 0.384   d<6>
                                                       d<6>
                                                       d_6_IOBUF/IBUF
    SLICE_X35Y56.D1      net (fanout=1)        1.512   N114
    SLICE_X35Y56.CLK     Tas                   0.022   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT291
                                                       regmd/md_6
    -------------------------------------------------  ---------------------------
    Total                                      1.918ns (0.406ns logic, 1.512ns route)
                                                       (21.2% logic, 78.8% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)
```

```
--------------------------------------------------------------------------------

Hold Paths: COMP "d<6>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_6 (SLICE_X35Y56.D1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.735ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<6> (PAD)
  Destination:          regmd/md_6 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.270ns (Levels of Logic = 2)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<6> to regmd/md_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C16.I                Tiopi                 0.532   d<6>
                                                       d<6>
                                                       d_6_IOBUF/IBUF
    SLICE_X35Y56.D1      net (fanout=1)        1.852   N114
    SLICE_X35Y56.CLK     Tah         (-Th)     0.114   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT291
                                                       regmd/md_6
    -------------------------------------------------  ---------------------------
    Total                                      2.270ns (0.418ns logic, 1.852ns route)
                                                       (18.4% logic, 81.6% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      1.408   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<5>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
```

```
 1 timing error detected.
 Minimum allowable offset is   8.010ns.
--------------------------------------------------------------------------------

Paths for end point d<5> (C22.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -4.010ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      5.508ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C22.T                net (fanout=32)       2.034   regmd/md_wr_inv
    C22.PAD              Tiotp                 1.868   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    -------------------------------------------------  ---------------------------
    Total                                      5.508ns (2.257ns logic, 3.251ns route)
                                                       (41.0% logic, 59.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.966ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
```

```
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      5.459ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C22.T                net (fanout=32)       2.034   regmd/md_wr_inv
    C22.PAD              Tiotp                 1.868   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    -------------------------------------------------  ---------------------------
    Total                                      5.459ns (2.204ns logic, 3.255ns route)
                                                       (40.4% logic, 59.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.864ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      5.362ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C22.T                net (fanout=32)       2.034   regmd/md_wr_inv
    C22.PAD              Tiotp                 1.868   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    -------------------------------------------------  ---------------------------
    Total                                      5.362ns (2.220ns logic, 3.142ns route)
                                                       (41.4% logic, 58.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<5>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<5> (C22.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  4.152ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      3.037ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C22.T                net (fanout=32)       1.212   regmd/md_wr_inv
    C22.PAD              Tiotp                 1.156   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    -------------------------------------------------  ---------------------------
    Total                                      3.037ns (1.288ns logic, 1.749ns route)
                                                       (42.4% logic, 57.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  4.145ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      3.032ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ------------------------------------------------  ------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C22.T                net (fanout=32)       1.212   regmd/md_wr_inv
    C22.PAD              Tiotp                 1.156   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    ------------------------------------------------  --------------------------
    Total                                      3.032ns (1.305ns logic, 1.727ns route)
                                                       (43.0% logic, 57.0% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.402ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_5 (FF)
  Destination:          d<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.270ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  ------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_5 to d<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  ------------------
    SLICE_X35Y56.DQ      Tcko                  0.098   regmd/md<5>
                                                       regmd/md_5
    C22.O                net (fanout=2)        1.016   regmd/md<5>
    C22.PAD              Tioop                 1.156   d<5>
                                                       d_5_IOBUF/OBUFT
                                                       d<5>
    ------------------------------------------------  --------------------------
    Total                                      2.270ns (1.254ns logic, 1.016ns route)
                                                       (55.2% logic, 44.8% route)

--------------------------------------------------------------------------------

================================================================================
```

```
Timing constraint: COMP "d<5>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.425ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_5 (SLICE_X35Y56.D2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.575ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<5> (PAD)
  Destination:          regmd/md_5 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.557ns (Levels of Logic = 2)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<5> to regmd/md_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C22.I                Tiopi                 0.401   d<5>
                                                       d<5>
                                                       d_5_IOBUF/IBUF
    SLICE_X35Y56.D2      net (fanout=1)        1.127   N115
    SLICE_X35Y56.CLK     Tas                   0.029   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT281
                                                       regmd/md_5
    -------------------------------------------------  ---------------------------
    Total                                      1.557ns (0.430ns logic, 1.127ns route)
                                                       (27.6% logic, 72.4% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<5>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
```

```
--------------------------------------------------------------------------------

Paths for end point regmd/md_5 (SLICE_X35Y56.D2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.411ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<5> (PAD)
  Destination:          regmd/md_5 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      1.946ns (Levels of Logic = 2)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<5> to regmd/md_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C22.I                Tiopi                 0.546   d<5>
                                                       d<5>
                                                       d_5_IOBUF/IBUF
    SLICE_X35Y56.D2      net (fanout=1)        1.478   N115
    SLICE_X35Y56.CLK     Tah         (-Th)     0.078   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT281
                                                       regmd/md_5
    -------------------------------------------------  ---------------------------
    Total                                      1.946ns (0.468ns logic, 1.478ns route)
                                                       (24.0% logic, 76.0% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      1.408   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<4>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   8.031ns.
--------------------------------------------------------------------------------
```

```
Paths for end point d<4> (E21.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -4.031ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      5.529ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E21.T                net (fanout=32)       2.080   regmd/md_wr_inv
    E21.PAD              Tiotp                 1.843   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    -------------------------------------------------  ---------------------------
    Total                                      5.529ns (2.232ns logic, 3.297ns route)
                                                       (40.4% logic, 59.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.987ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
```

```
  Data Path Delay:      5.480ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E21.T                net (fanout=32)       2.080   regmd/md_wr_inv
    E21.PAD              Tiotp                 1.843   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    -------------------------------------------------  ---------------------------
    Total                                      5.480ns (2.179ns logic, 3.301ns route)
                                                       (39.8% logic, 60.2% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.885ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      5.383ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)     1.375   clk_BUFGP
    ---------------------------------------------  ---------------------------
    Total                                     2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                 0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)      0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                 0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)       0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                 0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E21.T                net (fanout=32)      2.080   regmd/md_wr_inv
    E21.PAD              Tiotp                1.843   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    ---------------------------------------------  ---------------------------
    Total                                     5.383ns (2.195ns logic, 3.188ns route)
                                                       (40.8% logic, 59.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<4>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<4> (E21.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  4.170ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      3.055ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E21.T                net (fanout=32)       1.251   regmd/md_wr_inv
    E21.PAD              Tiotp                 1.135   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    ------------------------------------------------  ---------------------------
    Total                                      3.055ns (1.267ns logic, 1.788ns route)
                                                       (41.5% logic, 58.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  4.163ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      3.050ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
```

```
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    E21.T                net (fanout=32)       1.251   regmd/md_wr_inv
    E21.PAD              Tiotp                 1.135   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    -------------------------------------------------  ---------------------------
    Total                                      3.050ns (1.284ns logic, 1.766ns route)
                                                       (42.1% logic, 57.9% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.245ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_4 (FF)
  Destination:          d<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.128ns (Levels of Logic = 1)
  Clock Path Delay:     1.142ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y56.CLK     net (fanout=368)      0.558   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.142ns (0.353ns logic, 0.789ns route)
                                                       (30.9% logic, 69.1% route)

  Minimum Data Path at Fast Process Corner: regmd/md_4 to d<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y56.CMUX    Tshcko                0.128   regmd/md<3>
                                                       regmd/md_4
    E21.O                net (fanout=2)        0.865   regmd/md<4>
    E21.PAD              Tioop                 1.135   d<4>
                                                       d_4_IOBUF/OBUFT
                                                       d<4>
    -------------------------------------------------  ---------------------------
    Total                                      2.128ns (1.263ns logic, 0.865ns route)
                                                       (59.4% logic, 40.6% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<4>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).
```

```
 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.199ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_4 (SLICE_X27Y56.C2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.801ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<4> (PAD)
  Destination:          regmd/md_4 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.316ns (Levels of Logic = 2)
  Clock Path Delay:     1.142ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<4> to regmd/md_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E21.I                Tiopi                 0.376   d<4>
                                                       d<4>
                                                       d_4_IOBUF/IBUF
    SLICE_X27Y56.C2      net (fanout=1)        0.917   N116
    SLICE_X27Y56.CLK     Tas                   0.023   regmd/md<3>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT271
                                                       regmd/md_4
    -------------------------------------------------  ---------------------------
    Total                                      1.316ns (0.399ns logic, 0.917ns route)
                                                       (30.3% logic, 69.7% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y56.CLK     net (fanout=368)      0.558   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.142ns (0.353ns logic, 0.789ns route)
                                                       (30.9% logic, 69.1% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<4>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_4 (SLICE_X27Y56.C2), 1 path
```

```
--------------------------------------------------------------------------------
Slack (hold path):      0.121ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<4> (PAD)
  Destination:          regmd/md_4 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      1.632ns (Levels of Logic = 2)
  Clock Path Delay:     2.486ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<4> to regmd/md_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    E21.I                Tiopi                 0.525   d<4>
                                                       d<4>
                                                       d_4_IOBUF/IBUF
    SLICE_X27Y56.C2      net (fanout=1)        1.217   N116
    SLICE_X27Y56.CLK     Tah         (-Th)     0.110   regmd/md<3>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT271
                                                       regmd/md_4
    -------------------------------------------------  ---------------------------
    Total                                      1.632ns (0.415ns logic, 1.217ns route)
                                                       (25.4% logic, 74.6% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y56.CLK     net (fanout=368)      1.384   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.486ns (0.622ns logic, 1.864ns route)
                                                       (25.0% logic, 75.0% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<3>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.175ns.
--------------------------------------------------------------------------------

Paths for end point d<3> (B13.PAD), 9 paths
--------------------------------------------------------------------------------
```

```
Slack (slowest paths):  -3.175ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.673ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B13.T                net (fanout=32)       1.214   regmd/md_wr_inv
    B13.PAD              Tiotp                 1.853   d<3>
                                                       d_3_IOBUF/OBUFT
                                                       d<3>
    -------------------------------------------------  ---------------------------
    Total                                      4.673ns (2.242ns logic, 2.431ns route)
                                                       (48.0% logic, 52.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.131ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.624ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B13.T                net (fanout=32)       1.214   regmd/md_wr_inv
    B13.PAD              Tiotp                 1.853   d<3>
                                                       d_3_IOBUF/OBUFT
                                                       d<3>
    -------------------------------------------------  ---------------------------
    Total                                      4.624ns (2.189ns logic, 2.435ns route)
                                                       (47.3% logic, 52.7% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.029ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.527ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
```

```
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B13.T                net (fanout=32)       1.214   regmd/md_wr_inv
    B13.PAD              Tiotp                 1.853   d<3>
                                                       d_3_IOBUF/OBUFT
                                                       d<3>
    ------------------------------------------------  --------------------------
    Total                                      4.527ns (2.205ns logic, 2.322ns route)
                                                       (48.7% logic, 51.3% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<3>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<3> (B13.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.539ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.424ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
```

```
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B13.T                net (fanout=32)       0.611   regmd/md_wr_inv
    B13.PAD              Tiotp                 1.144   d<3>
                                                       d_3_IOBUF/OBUFT
                                                       d<3>
    ------------------------------------------------  --------------------------
    Total                                      2.424ns (1.276ns logic, 1.148ns route)
                                                       (52.6% logic, 47.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.532ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.419ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
```

```
    B13.T               net (fanout=32)       0.611   regmd/md_wr_inv
    B13.PAD             Tiotp                 1.144   d<3>
                                                      d_3_IOBUF/OBUFT
                                                      d<3>
    ------------------------------------------------  --------------------------
    Total                                     2.419ns (1.293ns logic, 1.126ns route)
                                                      (53.5% logic, 46.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.124ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_3 (FF)
  Destination:          d<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.007ns (Levels of Logic = 1)
  Clock Path Delay:     1.142ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_3
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I               Tiopi                 0.320   clk
                                                      clk
                                                      clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0    net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O     Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                      clk_BUFGP/BUFG
    SLICE_X27Y56.CLK    net (fanout=368)      0.558   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                     1.142ns (0.353ns logic, 0.789ns route)
                                                      (30.9% logic, 69.1% route)

  Minimum Data Path at Fast Process Corner: regmd/md_3 to d<3>
    Location            Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y56.CQ     Tcko                  0.098   regmd/md<3>
                                                      regmd/md_3
    B13.O               net (fanout=2)        0.765   regmd/md<3>
    B13.PAD             Tioop                 1.144   d<3>
                                                      d_3_IOBUF/OBUFT
                                                      d<3>
    ------------------------------------------------  --------------------------
    Total                                     2.007ns (1.242ns logic, 0.765ns route)
                                                      (61.9% logic, 38.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<3>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
```

```
 Minimum allowable offset is   0.617ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_3 (SLICE_X27Y56.C1), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.383ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<3> (PAD)
  Destination:          regmd/md_3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.734ns (Levels of Logic = 2)
  Clock Path Delay:     1.142ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<3> to regmd/md_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B13.I                Tiopi                 0.386   d<3>
                                                       d<3>
                                                       d_3_IOBUF/IBUF
    SLICE_X27Y56.C1      net (fanout=1)        1.318   N117
    SLICE_X27Y56.CLK     Tas                   0.030   regmd/md<3>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT261
                                                       regmd/md_3
    -------------------------------------------------  ---------------------------
    Total                                      1.734ns (0.416ns logic, 1.318ns route)
                                                       (24.0% logic, 76.0% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y56.CLK     net (fanout=368)      0.558   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.142ns (0.353ns logic, 0.789ns route)
                                                       (30.9% logic, 69.1% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<3>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_3 (SLICE_X27Y56.C1), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.678ns (requirement - (clock path + clock arrival + uncertainty -
data path))
```

```
  Source:               d<3> (PAD)
  Destination:          regmd/md_3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.189ns (Levels of Logic = 2)
  Clock Path Delay:     2.486ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<3> to regmd/md_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B13.I                Tiopi                 0.534   d<3>
                                                       d<3>
                                                       d_3_IOBUF/IBUF
    SLICE_X27Y56.C1      net (fanout=1)        1.730   N117
    SLICE_X27Y56.CLK     Tah         (-Th)     0.075   regmd/md<3>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT261
                                                       regmd/md_3
    -------------------------------------------------  ---------------------------
    Total                                      2.189ns (0.459ns logic, 1.730ns route)
                                                       (21.0% logic, 79.0% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y56.CLK     net (fanout=368)      1.384   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.486ns (0.622ns logic, 1.864ns route)
                                                       (25.0% logic, 75.0% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<2>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.081ns.
--------------------------------------------------------------------------------

Paths for end point d<2> (B19.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.081ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
```

```
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.579ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B19.T                net (fanout=32)       1.095   regmd/md_wr_inv
    B19.PAD              Tiotp                 1.878   d<2>
                                                       d_2_IOBUF/OBUFT
                                                       d<2>
    -------------------------------------------------  ---------------------------
    Total                                      4.579ns (2.267ns logic, 2.312ns route)
                                                       (49.5% logic, 50.5% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.037ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.530ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B19.T                net (fanout=32)       1.095   regmd/md_wr_inv
    B19.PAD              Tiotp                 1.878   d<2>
                                                       d_2_IOBUF/OBUFT
                                                       d<2>
    -------------------------------------------------  ---------------------------
    Total                                      4.530ns (2.214ns logic, 2.316ns route)
                                                       (48.9% logic, 51.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.935ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.433ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B19.T                net (fanout=32)       1.095   regmd/md_wr_inv
    B19.PAD              Tiotp                 1.878   d<2>
                                                       d_2_IOBUF/OBUFT
                                                       d<2>
    -------------------------------------------------  ---------------------------
    Total                                      4.433ns (2.230ns logic, 2.203ns route)
                                                       (50.3% logic, 49.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<2>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<2> (B19.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.492ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.377ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
```

```
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B19.T                net (fanout=32)       0.543   regmd/md_wr_inv
    B19.PAD              Tiotp                 1.165   d<2>
                                                       d_2_IOBUF/OBUFT
                                                       d<2>
    -------------------------------------------------  ---------------------------
    Total                                      2.377ns (1.297ns logic, 1.080ns route)
                                                       (54.6% logic, 45.4% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.485ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.372ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    B19.T                net (fanout=32)       0.543   regmd/md_wr_inv
    B19.PAD              Tiotp                 1.165   d<2>
                                                       d_2_IOBUF/OBUFT
```

```
                                                       d<2>
    ---------------------------------------------  --------------------------
    Total                                    2.372ns (1.314ns logic, 1.058ns route)
                                                       (55.4% logic, 44.6% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  2.984ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_2 (FF)
  Destination:          d<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.855ns (Levels of Logic = 1)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      0.570   clk_BUFGP
    ---------------------------------------------  --------------------------
    Total                                    1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regmd/md_2 to d<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    SLICE_X35Y58.CMUX    Tshcko                0.128   regmd/md<29>
                                                       regmd/md_2
    B19.O                net (fanout=2)        0.562   regmd/md<2>
    B19.PAD              Tioop                 1.165   d<2>
                                                       d_2_IOBUF/OBUFT
                                                       d<2>
    ---------------------------------------------  --------------------------
    Total                                    1.855ns (1.293ns logic, 0.562ns route)
                                                       (69.7% logic, 30.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<2>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.872ns.
--------------------------------------------------------------------------------
```

```
Paths for end point regmd/md_2 (SLICE_X35Y58.C2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.128ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<2> (PAD)
  Destination:          regmd/md_2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.001ns (Levels of Logic = 2)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<2> to regmd/md_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B19.I                Tiopi                 0.411   d<2>
                                                       d<2>
                                                       d_2_IOBUF/IBUF
    SLICE_X35Y58.C2      net (fanout=1)        1.567   N118
    SLICE_X35Y58.CLK     Tas                   0.023   regmd/md<29>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT231
                                                       regmd/md_2
    -------------------------------------------------  ---------------------------
    Total                                      2.001ns (0.434ns logic, 1.567ns route)
                                                       (21.7% logic, 78.3% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      0.570   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<2>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_2 (SLICE_X35Y58.C2), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.847ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<2> (PAD)
  Destination:          regmd/md_2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
```

```
  Requirement:          1.000ns
  Data Path Delay:      2.378ns (Levels of Logic = 2)
  Clock Path Delay:     2.506ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<2> to regmd/md_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B19.I                Tiopi                 0.555   d<2>
                                                       d<2>
                                                       d_2_IOBUF/IBUF
    SLICE_X35Y58.C2      net (fanout=1)        1.933   N118
    SLICE_X35Y58.CLK     Tah         (-Th)     0.110   regmd/md<29>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT231
                                                       regmd/md_2
    -------------------------------------------------  ---------------------------
    Total                                      2.378ns (0.445ns logic, 1.933ns route)
                                                       (18.7% logic, 81.3% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y58.CLK     net (fanout=368)      1.404   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.506ns (0.622ns logic, 1.884ns route)
                                                       (24.8% logic, 75.2% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<1>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.067ns.
--------------------------------------------------------------------------------

Paths for end point d<1> (A19.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.067ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
```

```
  Data Path Delay:      4.565ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A19.T                net (fanout=32)       1.079   regmd/md_wr_inv
    A19.PAD              Tiotp                 1.880   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    -------------------------------------------------  ---------------------------
    Total                                      4.565ns (2.269ns logic, 2.296ns route)
                                                       (49.7% logic, 50.3% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.023ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.516ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)       1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A19.T                net (fanout=32)       1.079   regmd/md_wr_inv
    A19.PAD              Tiotp                 1.880   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    -------------------------------------------------  ---------------------------
    Total                                      4.516ns (2.216ns logic, 2.300ns route)
                                                       (49.1% logic, 50.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -2.921ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.419ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
```

```
    ------------------------------------------------  --------------------------
    Total                                          2.477ns (0.622ns logic, 1.855ns route)
                                                           (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A19.T                net (fanout=32)       1.079   regmd/md_wr_inv
    A19.PAD              Tiotp                 1.880   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    ------------------------------------------------  --------------------------
    Total                                          4.419ns (2.232ns logic, 2.187ns route)
                                                           (50.5% logic, 49.5% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<1>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<1> (A19.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.483ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.368ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                          1.140ns (0.353ns logic, 0.787ns route)
                                                           (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<1>
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A19.T                net (fanout=32)       0.532   regmd/md_wr_inv
    A19.PAD              Tiotp                 1.167   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    -------------------------------------------------  ---------------------------
    Total                                      2.368ns (1.299ns logic, 1.069ns route)
                                                       (54.9% logic, 45.1% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.476ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.363ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    A19.T                net (fanout=32)       0.532   regmd/md_wr_inv
    A19.PAD              Tiotp                 1.167   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    -------------------------------------------------  ---------------------------
    Total                                      2.363ns (1.316ns logic, 1.047ns route)
```

```
                                                          (55.7% logic, 44.3% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.017ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_1 (FF)
  Destination:          d<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.890ns (Levels of Logic = 1)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regmd/md_1 to d<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y60.AQ      Tcko                  0.098   regmd/md<1>
                                                       regmd/md_1
    A19.O                net (fanout=2)        0.625   regmd/md<1>
    A19.PAD              Tioop                 1.167   d<1>
                                                       d_1_IOBUF/OBUFT
                                                       d<1>
    -------------------------------------------------  ---------------------------
    Total                                      1.890ns (1.265ns logic, 0.625ns route)
                                                       (66.9% logic, 33.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<1>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.920ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_1 (SLICE_X35Y60.A4), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.080ns (requirement - (data path - clock path - clock arrival +
```

```
uncertainty))
  Source:               d<1> (PAD)
  Destination:          regmd/md_1 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      2.047ns (Levels of Logic = 2)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<1> to regmd/md_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A19.I                Tiopi                 0.413   d<1>
                                                       d<1>
                                                       d_1_IOBUF/IBUF
    SLICE_X35Y60.A4      net (fanout=1)        1.603   N119
    SLICE_X35Y60.CLK     Tas                   0.031   regmd/md<1>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT121
                                                       regmd/md_1
    -------------------------------------------------  ---------------------------
    Total                                      2.047ns (0.444ns logic, 1.603ns route)
                                                       (21.7% logic, 78.3% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<1>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_1 (SLICE_X35Y60.A4), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.909ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<1> (PAD)
  Destination:          regmd/md_1 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.437ns (Levels of Logic = 2)
  Clock Path Delay:     2.503ns (Levels of Logic = 2)
```

```
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<1> to regmd/md_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    A19.I                Tiopi                 0.557   d<1>
                                                       d<1>
                                                       d_1_IOBUF/IBUF
    SLICE_X35Y60.A4      net (fanout=1)        1.955   N119
    SLICE_X35Y60.CLK     Tah         (-Th)     0.075   regmd/md<1>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT121
                                                       regmd/md_1
    -------------------------------------------------  ---------------------------
    Total                                      2.437ns (0.482ns logic, 1.955ns route)
                                                       (19.8% logic, 80.2% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y60.CLK     net (fanout=368)      1.401   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.503ns (0.622ns logic, 1.881ns route)
                                                       (24.9% logic, 75.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "d<0>" OFFSET = OUT 4 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 9 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.202ns.
--------------------------------------------------------------------------------

Paths for end point d<0> (C18.PAD), 9 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -3.202ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.700ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C18.T                net (fanout=32)       1.234   regmd/md_wr_inv
    C18.PAD              Tiotp                 1.860   d<0>
                                                       d_0_IOBUF/OBUFT
                                                       d<0>
    -------------------------------------------------  ---------------------------
    Total                                      4.700ns (2.249ns logic, 2.451ns route)
                                                       (47.9% logic, 52.1% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.158ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.651ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)       1.380   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       2.482ns (0.622ns logic, 1.860ns route)
                                                        (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                   0.283   control1/state_FSM_FFd2
                                                        control1/state_FSM_FFd1
    SLICE_X36Y61.D1      net (fanout=36)        1.221   control1/state_FSM_FFd1
    SLICE_X36Y61.D       Tilo                   0.053   regmd/md_wr_inv
                                                        regmd/md_wr_inv1
    C18.T                net (fanout=32)        1.234   regmd/md_wr_inv
    C18.PAD              Tiotp                  1.860   d<0>
                                                        d_0_IOBUF/OBUFT
                                                        d<0>
    ---------------------------------------------------  ---------------------------
    Total                                       4.651ns (2.196ns logic, 2.455ns route)
                                                        (47.2% logic, 52.8% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -3.056ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          4.000ns
  Data Path Delay:      4.554ns (Levels of Logic = 3)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)       1.375   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       2.477ns (0.622ns logic, 1.855ns route)
                                                        (25.1% logic, 74.9% route)
```

```
  Maximum Data Path at Slow Process Corner: regir/ir_27 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X36Y61.D6      net (fanout=3)        0.857   control1/Mmux_c1_out1132
    SLICE_X36Y61.D       Tilo                  0.053   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C18.T                net (fanout=32)       1.234   regmd/md_wr_inv
    C18.PAD              Tiotp                 1.860   d<0>
                                                       d_0_IOBUF/OBUFT
                                                       d<0>
    -------------------------------------------------  ---------------------------
    Total                                      4.554ns (2.212ns logic, 2.342ns route)
                                                       (48.6% logic, 51.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "d<0>" OFFSET = OUT 4 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point d<0> (C18.PAD), 9 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.557ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.442ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X36Y61.D4      net (fanout=39)       0.537   regir/ir<30>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C18.T                net (fanout=32)       0.623   regmd/md_wr_inv
    C18.PAD              Tiotp                 1.150   d<0>
                                                       d_0_IOBUF/OBUFT
                                                       d<0>
    ------------------------------------------------  --------------------------
    Total                                      2.442ns (1.282ns logic, 1.160ns route)
                                                       (52.5% logic, 47.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.550ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.437ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X36Y61.D5      net (fanout=40)       0.515   regir/ir<31>
    SLICE_X36Y61.D       Tilo                  0.034   regmd/md_wr_inv
                                                       regmd/md_wr_inv1
    C18.T                net (fanout=32)       0.623   regmd/md_wr_inv
    C18.PAD              Tiotp                 1.150   d<0>
                                                       d_0_IOBUF/OBUFT
                                                       d<0>
    ------------------------------------------------  --------------------------
    Total                                      2.437ns (1.299ns logic, 1.138ns route)
                                                       (53.3% logic, 46.7% route)

--------------------------------------------------------------------------------
```

```
Delay (fastest paths):  3.037ns (clock arrival + clock path + data path - uncertainty)
  Source:               regmd/md_0 (FF)
  Destination:          d<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.905ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regmd/md_0 to d<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X35Y56.AQ      Tcko                  0.098   regmd/md<5>
                                                       regmd/md_0
    C18.O                net (fanout=2)        0.657   regmd/md<0>
    C18.PAD              Tioop                 1.150   d<0>
                                                       d_0_IOBUF/OBUFT
                                                       d<0>
    -------------------------------------------------  ---------------------------
    Total                                      1.905ns (1.248ns logic, 0.657ns route)
                                                       (65.5% logic, 34.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "d<0>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.733ns.
--------------------------------------------------------------------------------

Paths for end point regmd/md_0 (SLICE_X35Y56.A4), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.267ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               d<0> (PAD)
  Destination:          regmd/md_0 (FF)
```

```
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.865ns (Levels of Logic = 2)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: d<0> to regmd/md_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C18.I                Tiopi                 0.393   d<0>
                                                       d<0>
                                                       d_0_IOBUF/IBUF
    SLICE_X35Y56.A4      net (fanout=1)        1.441   N120
    SLICE_X35Y56.CLK     Tas                   0.031   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT110
                                                       regmd/md_0
    -------------------------------------------------  ---------------------------
    Total                                      1.865ns (0.424ns logic, 1.441ns route)
                                                       (22.7% logic, 77.3% route)

  Minimum Clock Path at Fast Process Corner: clk to regmd/md_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

--------------------------------------------------------------------------------

Hold Paths: COMP "d<0>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point regmd/md_0 (SLICE_X35Y56.A4), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.754ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               d<0> (PAD)
  Destination:          regmd/md_0 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.289ns (Levels of Logic = 2)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: d<0> to regmd/md_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    C18.I                Tiopi                 0.540   d<0>
                                                       d<0>
                                                       d_0_IOBUF/IBUF
    SLICE_X35Y56.A4      net (fanout=1)        1.824   N120
    SLICE_X35Y56.CLK     Tah         (-Th)     0.075   regmd/md<5>

regmd/Mmux_md[31]_bus_in[31]_mux_1_OUT110
                                                       regmd/md_0
    -------------------------------------------------  ---------------------------
    Total                                      2.289ns (0.465ns logic, 1.824ns route)
                                                       (20.3% logic, 79.7% route)

  Maximum Clock Path at Slow Process Corner: clk to regmd/md_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X35Y56.CLK     net (fanout=368)      1.408   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "done" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk"
"RISING";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 8 paths analyzed, 5 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   0.903ns.
--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd2 (SLICE_X26Y61.B2), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     2.097ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.087ns (Levels of Logic = 3)
  Clock Path Delay:     2.209ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: done to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.528   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.D1      net (fanout=6)        1.504   done_IBUF
    SLICE_X26Y56.CMUX    Topdc                 0.274   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_F
                                                       control1/state_FSM_FFd2-In22
    SLICE_X26Y61.B2      net (fanout=2)        0.771   control1/state_FSM_FFd2-In22
    SLICE_X26Y61.CLK     Tas                   0.010   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2-In2
                                                       control1/state_FSM_FFd2
    -------------------------------------------------  ---------------------------
    Total                                      3.087ns (0.812ns logic, 2.275ns route)
                                                       (26.3% logic, 73.7% route)

  Minimum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.525   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.438   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.066   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.180   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.209ns (0.591ns logic, 1.618ns route)
                                                       (26.8% logic, 73.2% route)

--------------------------------------------------------------------------------
Slack (setup path):     2.329ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.785ns (Levels of Logic = 3)
  Clock Path Delay:     1.139ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: done to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.352   done
```

```
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.C6      net (fanout=6)        0.778   done_IBUF
    SLICE_X26Y56.CMUX    Tilo                  0.169   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_G
                                                       control1/state_FSM_FFd2-In22
    SLICE_X26Y61.B2      net (fanout=2)        0.477   control1/state_FSM_FFd2-In22
    SLICE_X26Y61.CLK     Tas                   0.009   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2-In2
                                                       control1/state_FSM_FFd2
    ---------------------------------------------------  ---------------------------
    Total                                      1.785ns (0.530ns logic, 1.255ns route)
                                                       (29.7% logic, 70.3% route)

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      0.555   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.139ns (0.353ns logic, 0.786ns route)
                                                       (31.0% logic, 69.0% route)

--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd3 (SLICE_X27Y60.C6), 3 paths
--------------------------------------------------------------------------------
Slack (setup path):     2.146ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.966ns (Levels of Logic = 4)
  Clock Path Delay:     1.137ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    H16.I                Tiopi                 0.352   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.D1      net (fanout=6)        0.992   done_IBUF
    SLICE_X26Y56.CMUX    Topdc                 0.167   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_F
                                                       control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D3      net (fanout=2)        0.337   control1/state_FSM_FFd2-In22
```

```
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.045   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tas                   0.030   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
    Total                                      1.966ns (0.592ns logic, 1.374ns route)
                                                       (30.1% logic, 69.9% route)

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      0.553   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.137ns (0.353ns logic, 0.784ns route)
                                                       (31.0% logic, 69.0% route)

--------------------------------------------------------------------------------
Slack (setup path):     2.358ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.754ns (Levels of Logic = 4)
  Clock Path Delay:     1.137ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.352   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.C6      net (fanout=6)        0.778   done_IBUF
    SLICE_X26Y56.CMUX    Tilo                  0.169   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_G
                                                       control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D3      net (fanout=2)        0.337   control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.045   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tas                   0.030   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
```

```
    Total                                     1.754ns (0.594ns logic, 1.160ns route)
                                                      (33.9% logic, 66.1% route)

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      0.553   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.137ns (0.353ns logic, 0.784ns route)
                                                      (31.0% logic, 69.0% route)

--------------------------------------------------------------------------------
Slack (setup path):     2.572ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.540ns (Levels of Logic = 3)
  Clock Path Delay:     1.137ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.352   done
                                                       done
                                                       done_IBUF
    SLICE_X27Y60.D2      net (fanout=6)        1.070   done_IBUF
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.045   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tas                   0.030   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
    Total                                     1.540ns (0.425ns logic, 1.115ns route)
                                                      (27.6% logic, 72.4% route)

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      0.553   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.137ns (0.353ns logic, 0.784ns route)
                                                       (31.0% logic, 69.0% route)

--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd1 (SLICE_X26Y61.A2), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     2.202ns (requirement - (data path - clock path - clock arrival +
uncertainty))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd1 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      1.912ns (Levels of Logic = 3)
  Clock Path Delay:     1.139ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Fast Process Corner: done to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.352   done
                                                       done
                                                       done_IBUF
    SLICE_X24Y57.D4      net (fanout=6)        0.963   done_IBUF
    SLICE_X24Y57.CMUX    Topdc                 0.167   srcalu/c<11>3
                                                       control1/state_FSM_FFd1-In3_F
                                                       control1/state_FSM_FFd1-In3
    SLICE_X26Y61.A2      net (fanout=1)        0.419   control1/state_FSM_FFd1-In3
    SLICE_X26Y61.CLK     Tas                   0.011   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1-In6
                                                       control1/state_FSM_FFd1
    -------------------------------------------------  ---------------------------
    Total                                      1.912ns (0.530ns logic, 1.382ns route)
                                                       (27.7% logic, 72.3% route)

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      0.555   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.139ns (0.353ns logic, 0.786ns route)
                                                       (31.0% logic, 69.0% route)
```

```
--------------------------------------------------------------------------------

Hold Paths: COMP "done" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd2 (SLICE_X26Y61.B6), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.144ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      1.651ns (Levels of Logic = 2)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y61.B6      net (fanout=6)        1.263   done_IBUF
    SLICE_X26Y61.CLK     Tah         (-Th)     0.116   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2-In2
                                                       control1/state_FSM_FFd2
    -------------------------------------------------  ---------------------------
    Total                                      1.651ns (0.388ns logic, 1.263ns route)
                                                       (23.5% logic, 76.5% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd3 (SLICE_X27Y60.C6), 3 paths
--------------------------------------------------------------------------------
Slack (hold path):      0.397ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
```

```
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      1.901ns (Levels of Logic = 3)
  Clock Path Delay:     2.479ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
                                                       done_IBUF
    SLICE_X27Y60.D2      net (fanout=6)        1.358   done_IBUF
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.071   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tah         (-Th)     0.075   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
    Total                                      1.901ns (0.472ns logic, 1.429ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      1.377   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.479ns (0.622ns logic, 1.857ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------
Slack (hold path):      0.679ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.183ns (Levels of Logic = 4)
  Clock Path Delay:     2.479ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.C6      net (fanout=6)        0.964   done_IBUF
    SLICE_X26Y56.CMUX    Tilo                  0.224   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_G
                                                       control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D3      net (fanout=2)        0.452   control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.071   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tah         (-Th)     0.075   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
    Total                                      2.183ns (0.696ns logic, 1.487ns route)
                                                       (31.9% logic, 68.1% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      1.377   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.479ns (0.622ns logic, 1.857ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------
Slack (hold path):      1.001ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd3 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.505ns (Levels of Logic = 4)
  Clock Path Delay:     2.479ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
```

```
                                                       done_IBUF
    SLICE_X26Y56.D1      net (fanout=6)        1.289   done_IBUF
    SLICE_X26Y56.CMUX    Topdc                 0.221   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_F
                                                       control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D3      net (fanout=2)        0.452   control1/state_FSM_FFd2-In22
    SLICE_X27Y60.D       Tilo                  0.043   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In1
    SLICE_X27Y60.C6      net (fanout=1)        0.071   control1/state_FSM_FFd3-In1
    SLICE_X27Y60.CLK     Tah         (-Th)     0.075   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3-In5
                                                       control1/state_FSM_FFd3
    -------------------------------------------------  ---------------------------
    Total                                      2.505ns (0.693ns logic, 1.812ns route)
                                                       (27.7% logic, 72.3% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      1.377   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.479ns (0.622ns logic, 1.857ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------

Paths for end point control1/state_FSM_FFd2 (SLICE_X26Y61.B2), 2 paths
--------------------------------------------------------------------------------
Slack (hold path):      0.712ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.219ns (Levels of Logic = 3)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.C6      net (fanout=6)        0.964   done_IBUF
    SLICE_X26Y56.CMUX    Tilo                  0.224   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_G
```

```
                                                       control1/state_FSM_FFd2-In22
    SLICE_X26Y61.B2      net (fanout=2)        0.643   control1/state_FSM_FFd2-In22
    SLICE_X26Y61.CLK     Tah         (-Th)     0.116   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2-In2
                                                       control1/state_FSM_FFd2
    -------------------------------------------------  ---------------------------
    Total                                      2.219ns (0.612ns logic, 1.607ns route)
                                                       (27.6% logic, 72.4% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------
Slack (hold path):      1.034ns (requirement - (clock path + clock arrival + uncertainty -
data path))
  Source:               done (PAD)
  Destination:          control1/state_FSM_FFd2 (FF)
  Destination Clock:    clk_BUFGP rising at 0.000ns
  Requirement:          1.000ns
  Data Path Delay:      2.541ns (Levels of Logic = 3)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: done to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    H16.I                Tiopi                 0.504   done
                                                       done
                                                       done_IBUF
    SLICE_X26Y56.D1      net (fanout=6)        1.289   done_IBUF
    SLICE_X26Y56.CMUX    Topdc                 0.221   control1/state_FSM_FFd2-In22
                                                       control1/state_FSM_FFd2-In22_F
                                                       control1/state_FSM_FFd2-In22
    SLICE_X26Y61.B2      net (fanout=2)        0.643   control1/state_FSM_FFd2-In22
    SLICE_X26Y61.CLK     Tah         (-Th)     0.116   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2-In2
                                                       control1/state_FSM_FFd2
    -------------------------------------------------  ---------------------------
    Total                                      2.541ns (0.609ns logic, 1.932ns route)
                                                       (24.0% logic, 76.0% route)

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd2
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<31>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.590ns.
--------------------------------------------------------------------------------

Paths for end point address<31> (L18.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.590ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_31 (FF)
  Destination:          address<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.053ns (Levels of Logic = 1)
  Clock Path Delay:     2.512ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y47.CLK      net (fanout=368)      1.410   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.512ns (0.622ns logic, 1.890ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_31 to address<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------  ------------------
    SLICE_X0Y47.AQ       Tcko                  0.283   regma/address<31>
                                                       regma/address_31
    L18.O                net (fanout=1)        0.953   regma/address<31>
    L18.PAD              Tioop                 1.817   address<31>
                                                       address_31_OBUF
                                                       address<31>
    ----------------------------------------------  ---------------------------
    Total                                      3.053ns (2.100ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<31>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<31> (L18.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.789ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_31 (FF)
  Destination:          address<31> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.657ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------  ------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y47.CLK      net (fanout=368)      0.573   clk_BUFGP
    ----------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_31 to address<31>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------  ------------------
    SLICE_X0Y47.AQ       Tcko                  0.115   regma/address<31>
                                                       regma/address_31
    L18.O                net (fanout=1)        0.429   regma/address<31>
    L18.PAD              Tioop                 1.113   address<31>
                                                       address_31_OBUF
                                                       address<31>
    ----------------------------------------------  ---------------------------
    Total                                      1.657ns (1.228ns logic, 0.429ns route)
                                                       (74.1% logic, 25.9% route)
```

```
--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<30>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.610ns.
--------------------------------------------------------------------------------

Paths for end point address<30> (J22.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.610ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_30 (FF)
  Destination:          address<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.071ns (Levels of Logic = 1)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y43.CLK      net (fanout=368)      1.412   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

  Maximum Data Path at Slow Process Corner: regma/address_30 to address<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y43.AQ       Tcko                  0.283   regma/address<30>
                                                       regma/address_30
    J22.O                net (fanout=1)        0.953   regma/address<30>
    J22.PAD              Tioop                 1.835   address<30>
                                                       address_30_OBUF
                                                       address<30>
    -------------------------------------------------  ---------------------------
    Total                                      3.071ns (2.118ns logic, 0.953ns route)
                                                       (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<30>" OFFSET = OUT 3 ns AFTER COMP "clk";
```

```
--------------------------------------------------------------------------------

Paths for end point address<30> (J22.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.806ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_30 (FF)
  Destination:          address<30> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.673ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y43.CLK      net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_30 to address<30>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y43.AQ       Tcko                  0.115   regma/address<30>
                                                       regma/address_30
    J22.O                net (fanout=1)        0.429   regma/address<30>
    J22.PAD              Tioop                 1.129   address<30>
                                                       address_30_OBUF
                                                       address<30>
    -------------------------------------------------  ---------------------------
    Total                                      1.673ns (1.244ns logic, 0.429ns route)
                                                       (74.4% logic, 25.6% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<29>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.607ns.
--------------------------------------------------------------------------------

Paths for end point address<29> (H20.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.607ns (requirement - (clock arrival + clock path + data path +
```

```
uncertainty))
  Source:               regma/address_29 (FF)
  Destination:          address<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.070ns (Levels of Logic = 1)
  Clock Path Delay:     2.512ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y46.CLK      net (fanout=368)      1.410   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.512ns (0.622ns logic, 1.890ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_29 to address<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y46.BQ       Tcko                  0.283   regma/address<29>
                                                       regma/address_29
    H20.O                net (fanout=1)        0.961   regma/address<29>
    H20.PAD              Tioop                 1.826   address<29>
                                                       address_29_OBUF
                                                       address<29>
    -------------------------------------------------  ---------------------------
    Total                                      3.070ns (2.109ns logic, 0.961ns route)
                                                       (68.7% logic, 31.3% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<29>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<29> (H20.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.801ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_29 (FF)
  Destination:          address<29> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.669ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y46.CLK      net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_29 to address<29>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y46.BQ       Tcko                  0.115   regma/address<29>
                                                       regma/address_29
    H20.O                net (fanout=1)        0.433   regma/address<29>
    H20.PAD              Tioop                 1.121   address<29>
                                                       address_29_OBUF
                                                       address<29>
    -------------------------------------------------  ---------------------------
    Total                                      1.669ns (1.236ns logic, 0.433ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<28>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.600ns.
--------------------------------------------------------------------------------

Paths for end point address<28> (H21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.600ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_28 (FF)
  Destination:          address<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.064ns (Levels of Logic = 1)
  Clock Path Delay:     2.511ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Clock Path at Slow Process Corner: clk to regma/address_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y48.CLK      net (fanout=368)      1.409   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.511ns (0.622ns logic, 1.889ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_28 to address<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y48.AQ       Tcko                  0.283   regma/address<28>
                                                       regma/address_28
    H21.O                net (fanout=1)        0.953   regma/address<28>
    H21.PAD              Tioop                 1.828   address<28>
                                                       address_28_OBUF
                                                       address<28>
    -------------------------------------------------  ---------------------------
    Total                                      3.064ns (2.111ns logic, 0.953ns route)
                                                       (68.9% logic, 31.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<28>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<28> (H21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.799ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_28 (FF)
  Destination:          address<28> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.667ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
```

```
    SLICE_X0Y48.CLK      net (fanout=368)      0.573   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_28 to address<28>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X0Y48.AQ       Tcko                  0.115   regma/address<28>
                                                       regma/address_28
    H21.O                net (fanout=1)        0.429   regma/address<28>
    H21.PAD              Tioop                 1.123   address<28>
                                                       address_28_OBUF
                                                       address<28>
    ------------------------------------------------  ---------------------------
    Total                                      1.667ns (1.238ns logic, 0.429ns route)
                                                       (74.3% logic, 25.7% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<27>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.540ns.
--------------------------------------------------------------------------------

Paths for end point address<27> (H18.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.540ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_27 (FF)
  Destination:          address<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.006ns (Levels of Logic = 1)
  Clock Path Delay:     2.509ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y50.CLK      net (fanout=368)      1.407   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      2.509ns (0.622ns logic, 1.887ns route)
```

```
                                                        (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_27 to address<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y50.AQ       Tcko                  0.246   regma/address<27>
                                                       regma/address_27
    H18.O                net (fanout=1)        0.953   regma/address<27>
    H18.PAD              Tioop                 1.807   address<27>
                                                       address_27_OBUF
                                                       address<27>
    -------------------------------------------------  ---------------------------
    Total                                      3.006ns (2.053ns logic, 0.953ns route)
                                                       (68.3% logic, 31.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<27>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<27> (H18.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.762ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_27 (FF)
  Destination:          address<27> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.632ns (Levels of Logic = 1)
  Clock Path Delay:     1.155ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y50.CLK      net (fanout=368)      0.571   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.155ns (0.353ns logic, 0.802ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_27 to address<27>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y50.AQ       Tcko                  0.098   regma/address<27>
                                                       regma/address_27
    H18.O                net (fanout=1)        0.429   regma/address<27>
    H18.PAD              Tioop                 1.105   address<27>
                                                       address_27_OBUF
```

```
                                                       address<27>
    ---------------------------------------------------  ---------------------------
    Total                                          1.632ns (1.203ns logic, 0.429ns route)
                                                           (73.7% logic, 26.3% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<26>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.610ns.
--------------------------------------------------------------------------------

Paths for end point address<26> (G21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.610ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_26 (FF)
  Destination:          address<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.075ns (Levels of Logic = 1)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y49.CLK      net (fanout=368)      1.408   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_26 to address<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X0Y49.AQ       Tcko                  0.283   regma/address<26>
                                                       regma/address_26
    G21.O                net (fanout=1)        0.953   regma/address<26>
    G21.PAD              Tioop                 1.839   address<26>
                                                       address_26_OBUF
                                                       address<26>
    ---------------------------------------------------  ---------------------------
    Total                                      3.075ns (2.122ns logic, 0.953ns route)
```

```
                                                        (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<26>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<26> (G21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.806ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_26 (FF)
  Destination:          address<26> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.675ns (Levels of Logic = 1)
  Clock Path Delay:     1.156ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_26
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y49.CLK      net (fanout=368)      0.572   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.156ns (0.353ns logic, 0.803ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_26 to address<26>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y49.AQ       Tcko                  0.115   regma/address<26>
                                                       regma/address_26
    G21.O                net (fanout=1)        0.429   regma/address<26>
    G21.PAD              Tioop                 1.131   address<26>
                                                       address_26_OBUF
                                                       address<26>
    -------------------------------------------------  ---------------------------
    Total                                      1.675ns (1.246ns logic, 0.429ns route)
                                                       (74.4% logic, 25.6% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<25>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.588ns.
```

```
--------------------------------------------------------------------------------

Paths for end point address<25> (L19.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.588ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_25 (FF)
  Destination:          address<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.051ns (Levels of Logic = 1)
  Clock Path Delay:     2.512ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y46.CLK      net (fanout=368)     1.410   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.512ns (0.622ns logic, 1.890ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_25 to address<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y46.AQ       Tcko                 0.283   regma/address<29>
                                                       regma/address_25
    L19.O                net (fanout=1)       0.953   regma/address<25>
    L19.PAD              Tioop                1.815   address<25>
                                                       address_25_OBUF
                                                       address<25>
    -------------------------------------------------  ---------------------------
    Total                                     3.051ns (2.098ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<25>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<25> (L19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.787ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_25 (FF)
  Destination:          address<25> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.655ns (Levels of Logic = 1)
```

```
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_25
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y46.CLK      net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_25 to address<25>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y46.AQ       Tcko                  0.115   regma/address<29>
                                                       regma/address_25
    L19.O                net (fanout=1)        0.429   regma/address<25>
    L19.PAD              Tioop                 1.111   address<25>
                                                       address_25_OBUF
                                                       address<25>
    -------------------------------------------------  ---------------------------
    Total                                      1.655ns (1.226ns logic, 0.429ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<24>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.614ns.
--------------------------------------------------------------------------------

Paths for end point address<24> (F21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.614ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_24 (FF)
  Destination:          address<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.089ns (Levels of Logic = 1)
  Clock Path Delay:     2.500ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y55.CLK      net (fanout=368)      1.398   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.500ns (0.622ns logic, 1.878ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_24 to address<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y55.AQ       Tcko                  0.283   regma/address<24>
                                                       regma/address_24
    F21.O                net (fanout=1)        0.953   regma/address<24>
    F21.PAD              Tioop                 1.853   address<24>
                                                       address_24_OBUF
                                                       address<24>
    -------------------------------------------------  ---------------------------
    Total                                      3.089ns (2.136ns logic, 0.953ns route)
                                                       (69.1% logic, 30.9% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<24>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<24> (F21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.813ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_24 (FF)
  Destination:          address<24> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.687ns (Levels of Logic = 1)
  Clock Path Delay:     1.151ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_24
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
```

```
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y55.CLK      net (fanout=368)      0.567   clk_BUFGP
    ------------------------------------------------  --------------------------
    Total                                      1.151ns (0.353ns logic, 0.798ns route)
                                                       (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_24 to address<24>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X0Y55.AQ       Tcko                  0.115   regma/address<24>
                                                       regma/address_24
    F21.O                net (fanout=1)        0.429   regma/address<24>
    F21.PAD              Tioop                 1.143   address<24>
                                                       address_24_OBUF
                                                       address<24>
    ------------------------------------------------  --------------------------
    Total                                      1.687ns (1.258ns logic, 0.429ns route)
                                                       (74.6% logic, 25.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<23>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.543ns.
--------------------------------------------------------------------------------

Paths for end point address<23> (H17.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.543ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_23 (FF)
  Destination:          address<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.011ns (Levels of Logic = 1)
  Clock Path Delay:     2.507ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y51.CLK      net (fanout=368)      1.405   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.507ns (0.622ns logic, 1.885ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_23 to address<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X1Y51.AQ       Tcko                  0.246   regma/address<23>
                                                       regma/address_23
    H17.O                net (fanout=1)        0.953   regma/address<23>
    H17.PAD              Tioop                 1.812   address<23>
                                                       address_23_OBUF
                                                       address<23>
    ---------------------------------------------------  ---------------------------
    Total                                      3.011ns (2.058ns logic, 0.953ns route)
                                                       (68.3% logic, 31.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<23>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<23> (H17.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.765ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_23 (FF)
  Destination:          address<23> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.636ns (Levels of Logic = 1)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_23
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y51.CLK      net (fanout=368)      0.570   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_23 to address<23>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
```

```
    SLICE_X1Y51.AQ       Tcko                  0.098   regma/address<23>
                                                       regma/address_23
    H17.O                net (fanout=1)        0.429   regma/address<23>
    H17.PAD              Tioop                 1.109   address<23>
                                                       address_23_OBUF
                                                       address<23>
    -------------------------------------------------  ---------------------------
    Total                                      1.636ns (1.207ns logic, 0.429ns route)
                                                       (73.8% logic, 26.2% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<22>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.580ns.
--------------------------------------------------------------------------------

Paths for end point address<22> (F22.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.580ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_22 (FF)
  Destination:          address<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.053ns (Levels of Logic = 1)
  Clock Path Delay:     2.502ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y54.CLK      net (fanout=368)      1.400   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.502ns (0.622ns logic, 1.880ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_22 to address<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y54.AQ       Tcko                  0.246   regma/address<22>
                                                       regma/address_22
    F22.O                net (fanout=1)        0.953   regma/address<22>
```

```
    F22.PAD              Tioop                 1.854   address<22>
                                                        address_22_OBUF
                                                        address<22>
    -------------------------------------------------  ---------------------------
    Total                                      3.053ns (2.100ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<22>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<22> (F22.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.797ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_22 (FF)
  Destination:          address<22> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.671ns (Levels of Logic = 1)
  Clock Path Delay:     1.151ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_22
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y54.CLK      net (fanout=368)      0.567   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.151ns (0.353ns logic, 0.798ns route)
                                                       (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_22 to address<22>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y54.AQ       Tcko                  0.098   regma/address<22>
                                                       regma/address_22
    F22.O                net (fanout=1)        0.429   regma/address<22>
    F22.PAD              Tioop                 1.144   address<22>
                                                       address_22_OBUF
                                                       address<22>
    -------------------------------------------------  ---------------------------
    Total                                      1.671ns (1.242ns logic, 0.429ns route)
                                                       (74.3% logic, 25.7% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<21>" OFFSET = OUT 3 ns AFTER COMP "clk";
```

For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.584ns.

Paths for end point address<21> (K20.PAD), 1 path

Slack (slowest paths): -2.584ns (requirement - (clock arrival + clock path + data path + uncertainty))
  Source: regma/address_21 (FF)
  Destination: address<21> (PAD)
  Source Clock: clk_BUFGP rising at 0.000ns
  Requirement: 3.000ns
  Data Path Delay: 3.053ns (Levels of Logic = 1)
  Clock Path Delay: 2.506ns (Levels of Logic = 2)
  Clock Uncertainty: 0.025ns

  Clock Uncertainty: 0.025ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ): 0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):   0.000ns
    Phase Error (PE):   0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_21
    Location   Delay type   Delay(ns) Physical Resource
                                                       Logical Resource(s)
    --- -------------------
    D12.I   Tiopi   0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0   net (fanout=1)   0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O   Tbgcko_O   0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y52.CLK   net (fanout=368)   1.404   clk_BUFGP
    --- ---------------------------
    Total   2.506ns (0.622ns logic, 1.884ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_21 to address<21>
    Location   Delay type   Delay(ns) Physical Resource
                                                       Logical Resource(s)
    --- -------------------
    SLICE_X0Y52.AQ   Tcko   0.283   regma/address<21>
                                                       regma/address_21
    K20.O   net (fanout=1)   0.953   regma/address<21>
    K20.PAD   Tioop   1.817   address<21>
                                                       address_21_OBUF
                                                       address<21>
    --- ---------------------------
    Total   3.053ns (2.100ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

Fastest Paths: COMP "address<21>" OFFSET = OUT 3 ns AFTER COMP "clk";

Paths for end point address<21> (K20.PAD), 1 path

```
Delay (fastest paths):  2.785ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_21 (FF)
  Destination:          address<21> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.657ns (Levels of Logic = 1)
  Clock Path Delay:     1.153ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_21
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y52.CLK      net (fanout=368)      0.569   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.153ns (0.353ns logic, 0.800ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_21 to address<21>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y52.AQ       Tcko                  0.115   regma/address<21>
                                                       regma/address_21
    K20.O                net (fanout=1)        0.429   regma/address<21>
    K20.PAD              Tioop                 1.113   address<21>
                                                       address_21_OBUF
                                                       address<21>
    -------------------------------------------------  ---------------------------
    Total                                      1.657ns (1.228ns logic, 0.429ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<20>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.545ns.
--------------------------------------------------------------------------------

Paths for end point address<20> (J20.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.545ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_20 (FF)
  Destination:          address<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
```

```
  Requirement:          3.000ns
  Data Path Delay:      3.017ns (Levels of Logic = 1)
  Clock Path Delay:     2.503ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y53.CLK      net (fanout=368)      1.401   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.503ns (0.622ns logic, 1.881ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_20 to address<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y53.AQ       Tcko                  0.246   regma/address<20>
                                                       regma/address_20
    J20.O                net (fanout=1)        0.953   regma/address<20>
    J20.PAD              Tioop                 1.818   address<20>
                                                       address_20_OBUF
                                                       address<20>
    -------------------------------------------------  ---------------------------
    Total                                      3.017ns (2.064ns logic, 0.953ns route)
                                                       (68.4% logic, 31.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<20>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<20> (J20.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.768ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_20 (FF)
  Destination:          address<20> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.641ns (Levels of Logic = 1)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Clock Path at Fast Process Corner: clk to regma/address_20
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y53.CLK      net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_20 to address<20>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y53.AQ       Tcko                  0.098   regma/address<20>
                                                       regma/address_20
    J20.O                net (fanout=1)        0.429   regma/address<20>
    J20.PAD              Tioop                 1.114   address<20>
                                                       address_20_OBUF
                                                       address<20>
    -------------------------------------------------  ---------------------------
    Total                                      1.641ns (1.212ns logic, 0.429ns route)
                                                       (73.9% logic, 26.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<19>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.671ns.
--------------------------------------------------------------------------------

Paths for end point address<19> (G19.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.671ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_19 (FF)
  Destination:          address<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.134ns (Levels of Logic = 1)
  Clock Path Delay:     2.512ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X0Y73.CLK      net (fanout=368)       1.410   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                       2.512ns (0.622ns logic, 1.890ns route)
                                                        (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_19 to address<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    SLICE_X0Y73.DQ       Tcko                   0.283   regma/address<19>
                                                        regma/address_19
    G19.O                net (fanout=1)         1.038   regma/address<19>
    G19.PAD              Tioop                  1.813   address<19>
                                                        address_19_OBUF
                                                        address<19>
    ----------------------------------------------------  ---------------------------
    Total                                       3.134ns (2.096ns logic, 1.038ns route)
                                                        (66.9% logic, 33.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<19>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<19> (G19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.832ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_19 (FF)
  Destination:          address<19> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.700ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_19
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  ------------------
    D12.I                Tiopi                  0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X0Y73.CLK      net (fanout=368)       0.573   clk_BUFGP
    ----------------------------------------------------  ---------------------------
    Total                                       1.157ns (0.353ns logic, 0.804ns route)
                                                        (30.5% logic, 69.5% route)
```

```
  Minimum Data Path at Fast Process Corner: regma/address_19 to address<19>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y73.DQ       Tcko                  0.115   regma/address<19>
                                                       regma/address_19
    G19.O                net (fanout=1)        0.475   regma/address<19>
    G19.PAD              Tioop                 1.110   address<19>
                                                       address_19_OBUF
                                                       address<19>
    -------------------------------------------------  ---------------------------
    Total                                      1.700ns (1.225ns logic, 0.475ns route)
                                                       (72.1% logic, 27.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<18>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.562ns.
--------------------------------------------------------------------------------

Paths for end point address<18> (E19.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.562ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_18 (FF)
  Destination:          address<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.035ns (Levels of Logic = 1)
  Clock Path Delay:     2.502ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y65.CLK      net (fanout=368)      1.400   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.502ns (0.622ns logic, 1.880ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_18 to address<18>
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X1Y65.CQ       Tcko                  0.246   regma/address<18>
                                                       regma/address_18
    E19.O                net (fanout=1)        0.953   regma/address<18>
    E19.PAD              Tioop                 1.836   address<18>
                                                       address_18_OBUF
                                                       address<18>
    ---------------------------------------------------  ---------------------------
    Total                                      3.035ns (2.082ns logic, 0.953ns route)
                                                       (68.6% logic, 31.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<18>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<18> (E19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.783ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_18 (FF)
  Destination:          address<18> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.657ns (Levels of Logic = 1)
  Clock Path Delay:     1.151ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_18
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y65.CLK      net (fanout=368)      0.567   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.151ns (0.353ns logic, 0.798ns route)
                                                       (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_18 to address<18>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X1Y65.CQ       Tcko                  0.098   regma/address<18>
                                                       regma/address_18
    E19.O                net (fanout=1)        0.430   regma/address<18>
    E19.PAD              Tioop                 1.129   address<18>
                                                       address_18_OBUF
                                                       address<18>
    ---------------------------------------------------  ---------------------------
    Total                                      1.657ns (1.227ns logic, 0.430ns route)
                                                       (74.0% logic, 26.0% route)
```

```
--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<17>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.634ns.
--------------------------------------------------------------------------------

Paths for end point address<17> (B21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.634ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_17 (FF)
  Destination:          address<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.096ns (Levels of Logic = 1)
  Clock Path Delay:     2.513ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y74.CLK      net (fanout=368)      1.411   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.513ns (0.622ns logic, 1.891ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_17 to address<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y74.AQ       Tcko                  0.283   regma/address<17>
                                                       regma/address_17
    B21.O                net (fanout=1)        0.953   regma/address<17>
    B21.PAD              Tioop                 1.860   address<17>
                                                       address_17_OBUF
                                                       address<17>
    -------------------------------------------------  ---------------------------
    Total                                      3.096ns (2.143ns logic, 0.953ns route)
                                                       (69.2% logic, 30.8% route)

--------------------------------------------------------------------------------
```

```
Fastest Paths: COMP "address<17>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<17> (B21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.825ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_17 (FF)
  Destination:          address<17> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.693ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y74.CLK      net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_17 to address<17>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y74.AQ       Tcko                  0.115   regma/address<17>
                                                       regma/address_17
    B21.O                net (fanout=1)        0.429   regma/address<17>
    B21.PAD              Tioop                 1.149   address<17>
                                                       address_17_OBUF
                                                       address<17>
    -------------------------------------------------  ---------------------------
    Total                                      1.693ns (1.264ns logic, 0.429ns route)
                                                       (74.7% logic, 25.3% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<16>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.612ns.
--------------------------------------------------------------------------------

Paths for end point address<16> (B22.PAD), 1 path
--------------------------------------------------------------------------------
```

```
Slack (slowest paths):  -2.612ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_16 (FF)
  Destination:          address<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.078ns (Levels of Logic = 1)
  Clock Path Delay:     2.509ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y69.CLK      net (fanout=368)      1.407   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.509ns (0.622ns logic, 1.887ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_16 to address<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y69.AQ       Tcko                  0.246   regma/address<16>
                                                       regma/address_16
    B22.O                net (fanout=1)        0.953   regma/address<16>
    B22.PAD              Tioop                 1.879   address<16>
                                                       address_16_OBUF
                                                       address<16>
    -------------------------------------------------  ---------------------------
    Total                                      3.078ns (2.125ns logic, 0.953ns route)
                                                       (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<16>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<16> (B22.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.823ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_16 (FF)
  Destination:          address<16> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.693ns (Levels of Logic = 1)
  Clock Path Delay:     1.155ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_16
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y69.CLK      net (fanout=368)      0.571   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.155ns (0.353ns logic, 0.802ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_16 to address<16>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y69.AQ       Tcko                  0.098   regma/address<16>
                                                       regma/address_16
    B22.O                net (fanout=1)        0.429   regma/address<16>
    B22.PAD              Tioop                 1.166   address<16>
                                                       address_16_OBUF
                                                       address<16>
    -------------------------------------------------  ---------------------------
    Total                                      1.693ns (1.264ns logic, 0.429ns route)
                                                       (74.7% logic, 25.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<15>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.575ns.
--------------------------------------------------------------------------------

Paths for end point address<15> (J17.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.575ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_15 (FF)
  Destination:          address<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.040ns (Levels of Logic = 1)
  Clock Path Delay:     2.510ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_15
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y70.CLK      net (fanout=368)      1.408   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.510ns (0.622ns logic, 1.888ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_15 to address<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y70.AQ       Tcko                  0.283   regma/address<15>
                                                       regma/address_15
    J17.O                net (fanout=1)        0.953   regma/address<15>
    J17.PAD              Tioop                 1.804   address<15>
                                                       address_15_OBUF
                                                       address<15>
    -------------------------------------------------  ---------------------------
    Total                                      3.040ns (2.087ns logic, 0.953ns route)
                                                       (68.7% logic, 31.3% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<15>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<15> (J17.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.777ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_15 (FF)
  Destination:          address<15> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.646ns (Levels of Logic = 1)
  Clock Path Delay:     1.156ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_15
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
```

```
                                                       clk_BUFGP/BUFG
    SLICE_X0Y70.CLK      net (fanout=368)      0.572   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.156ns (0.353ns logic, 0.803ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_15 to address<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X0Y70.AQ       Tcko                  0.115   regma/address<15>
                                                       regma/address_15
    J17.O                net (fanout=1)        0.429   regma/address<15>
    J17.PAD              Tioop                 1.102   address<15>
                                                       address_15_OBUF
                                                       address<15>
    ---------------------------------------------------  ---------------------------
    Total                                      1.646ns (1.217ns logic, 0.429ns route)
                                                       (73.9% logic, 26.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<14>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.563ns.
--------------------------------------------------------------------------------

Paths for end point address<14> (D19.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.563ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_14 (FF)
  Destination:          address<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.038ns (Levels of Logic = 1)
  Clock Path Delay:     2.500ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y64.CLK      net (fanout=368)      1.398   clk_BUFGP
    ---------------------------------------------------  ---------------------------
```

```
    Total                                     2.500ns (0.622ns logic, 1.878ns route)
                                                      (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_14 to address<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y64.CQ       Tcko                  0.246   regma/address<14>
                                                       regma/address_14
    D19.O                net (fanout=1)        0.953   regma/address<14>
    D19.PAD              Tioop                 1.839   address<14>
                                                       address_14_OBUF
                                                       address<14>
    -------------------------------------------------  ---------------------------
    Total                                     3.038ns (2.085ns logic, 0.953ns route)
                                                      (68.6% logic, 31.4% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<14>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<14> (D19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.786ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_14 (FF)
  Destination:          address<14> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.660ns (Levels of Logic = 1)
  Clock Path Delay:     1.151ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_14
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y64.CLK      net (fanout=368)      0.567   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.151ns (0.353ns logic, 0.798ns route)
                                                      (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_14 to address<14>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y64.CQ       Tcko                  0.098   regma/address<14>
                                                       regma/address_14
    D19.O                net (fanout=1)        0.430   regma/address<14>
    D19.PAD              Tioop                 1.132   address<14>
```

```
                                                       address_14_OBUF
                                                       address<14>
    ---------------------------------------------  ---------------------------
    Total                                    1.660ns (1.230ns logic, 0.430ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<13>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.546ns.
--------------------------------------------------------------------------------

Paths for end point address<13> (K17.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.546ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_13 (FF)
  Destination:          address<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.018ns (Levels of Logic = 1)
  Clock Path Delay:     2.503ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y66.CLK      net (fanout=368)      1.401   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.503ns (0.622ns logic, 1.881ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_13 to address<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y66.BQ       Tcko                  0.246   regma/address<13>
                                                       regma/address_13
    K17.O                net (fanout=1)        0.959   regma/address<13>
    K17.PAD              Tioop                 1.813   address<13>
                                                       address_13_OBUF
                                                       address<13>
    -------------------------------------------------  ---------------------------
```

```
    Total                                     3.018ns (2.059ns logic, 0.959ns route)
                                                      (68.2% logic, 31.8% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<13>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<13> (K17.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.765ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_13 (FF)
  Destination:          address<13> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.638ns (Levels of Logic = 1)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y66.CLK      net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_13 to address<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y66.BQ       Tcko                  0.098   regma/address<13>
                                                       regma/address_13
    K17.O                net (fanout=1)        0.431   regma/address<13>
    K17.PAD              Tioop                 1.109   address<13>
                                                       address_13_OBUF
                                                       address<13>
    -------------------------------------------------  ---------------------------
    Total                                      1.638ns (1.207ns logic, 0.431ns route)
                                                       (73.7% logic, 26.3% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<12>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
```

```
 Minimum allowable offset is   5.544ns.
--------------------------------------------------------------------------------

Paths for end point address<12> (L17.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.544ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_12 (FF)
  Destination:          address<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.016ns (Levels of Logic = 1)
  Clock Path Delay:     2.503ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y66.CLK      net (fanout=368)      1.401   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.503ns (0.622ns logic, 1.881ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_12 to address<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y66.AQ       Tcko                  0.246   regma/address<13>
                                                       regma/address_12
    L17.O                net (fanout=1)        0.953   regma/address<12>
    L17.PAD              Tioop                 1.817   address<12>
                                                       address_12_OBUF
                                                       address<12>
    -------------------------------------------------  ---------------------------
    Total                                      3.016ns (2.063ns logic, 0.953ns route)
                                                       (68.4% logic, 31.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<12>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<12> (L17.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.767ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_12 (FF)
  Destination:          address<12> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
```

```
  Data Path Delay:      1.640ns (Levels of Logic = 1)
  Clock Path Delay:     1.152ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_12
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y66.CLK      net (fanout=368)      0.568   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.152ns (0.353ns logic, 0.799ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_12 to address<12>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y66.AQ       Tcko                  0.098   regma/address<13>
                                                       regma/address_12
    L17.O                net (fanout=1)        0.429   regma/address<12>
    L17.PAD              Tioop                 1.113   address<12>
                                                       address_12_OBUF
                                                       address<12>
    -------------------------------------------------  ---------------------------
    Total                                      1.640ns (1.211ns logic, 0.429ns route)
                                                       (73.8% logic, 26.2% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<11>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.626ns.
--------------------------------------------------------------------------------

Paths for end point address<11> (B20.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.626ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_11 (FF)
  Destination:          address<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.087ns (Levels of Logic = 1)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y78.CLK      net (fanout=368)      1.412   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

  Maximum Data Path at Slow Process Corner: regma/address_11 to address<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y78.BQ       Tcko                  0.283   regma/address<11>
                                                       regma/address_11
    B20.O                net (fanout=1)        0.959   regma/address<11>
    B20.PAD              Tioop                 1.845   address<11>
                                                       address_11_OBUF
                                                       address<11>
    -------------------------------------------------  ---------------------------
    Total                                      3.087ns (2.128ns logic, 0.959ns route)
                                                       (68.9% logic, 31.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<11>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<11> (B20.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.816ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_11 (FF)
  Destination:          address<11> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.683ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_11
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y78.CLK      net (fanout=368)      0.574   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_11 to address<11>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X0Y78.BQ       Tcko                  0.115   regma/address<11>
                                                       regma/address_11
    B20.O                net (fanout=1)        0.431   regma/address<11>
    B20.PAD              Tioop                 1.137   address<11>
                                                       address_11_OBUF
                                                       address<11>
    ------------------------------------------------  ---------------------------
    Total                                      1.683ns (1.252ns logic, 0.431ns route)
                                                       (74.4% logic, 25.6% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<10>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.590ns.
--------------------------------------------------------------------------------

Paths for end point address<10> (F18.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.590ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_10 (FF)
  Destination:          address<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.051ns (Levels of Logic = 1)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y76.CLK      net (fanout=368)      1.412   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

  Maximum Data Path at Slow Process Corner: regma/address_10 to address<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X0Y76.AQ       Tcko                  0.283   regma/address<10>
                                                       regma/address_10
    F18.O                net (fanout=1)        0.953   regma/address<10>
    F18.PAD              Tioop                 1.815   address<10>
                                                       address_10_OBUF
                                                       address<10>
    ---------------------------------------------------  ---------------------------
    Total                                      3.051ns (2.098ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<10>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<10> (F18.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.788ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_10 (FF)
  Destination:          address<10> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.655ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_10
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y76.CLK      net (fanout=368)      0.574   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_10 to address<10>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------  ------------------
    SLICE_X0Y76.AQ       Tcko                  0.115   regma/address<10>
                                                       regma/address_10
    F18.O                net (fanout=1)        0.429   regma/address<10>
    F18.PAD              Tioop                 1.111   address<10>
                                                       address_10_OBUF
                                                       address<10>
    ----------------------------------------------  ------------------------
    Total                                      1.655ns (1.226ns logic, 0.429ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<9>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.622ns.
--------------------------------------------------------------------------------

Paths for end point address<9> (C20.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.622ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_9 (FF)
  Destination:          address<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.083ns (Levels of Logic = 1)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------  ------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y77.CLK      net (fanout=368)      1.412   clk_BUFGP
    ----------------------------------------------  ------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

  Maximum Data Path at Slow Process Corner: regma/address_9 to address<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------  ------------------
    SLICE_X0Y77.BQ       Tcko                  0.283   regma/address<9>
                                                       regma/address_9
```

```
    C20.O                net (fanout=1)        0.959   regma/address<9>
    C20.PAD              Tioop                 1.841   address<9>
                                                       address_9_OBUF
                                                       address<9>
    ---------------------------------------------------  ---------------------------
    Total                                      3.083ns (2.124ns logic, 0.959ns route)
                                                       (68.9% logic, 31.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<9>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<9> (C20.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.812ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_9 (FF)
  Destination:          address<9> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.679ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_9
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y77.CLK      net (fanout=368)      0.574   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_9 to address<9>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X0Y77.BQ       Tcko                  0.115   regma/address<9>
                                                       regma/address_9
    C20.O                net (fanout=1)        0.431   regma/address<9>
    C20.PAD              Tioop                 1.133   address<9>
                                                       address_9_OBUF
                                                       address<9>
    ---------------------------------------------------  ---------------------------
    Total                                      1.679ns (1.248ns logic, 0.431ns route)
                                                       (74.3% logic, 25.7% route)

--------------------------------------------------------------------------------

================================================================================
```

```
Timing constraint: COMP "address<8>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.586ns.
--------------------------------------------------------------------------------

Paths for end point address<8> (G18.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.586ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_8 (FF)
  Destination:          address<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.047ns (Levels of Logic = 1)
  Clock Path Delay:     2.514ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y77.CLK      net (fanout=368)      1.412   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.514ns (0.622ns logic, 1.892ns route)
                                                       (24.7% logic, 75.3% route)

  Maximum Data Path at Slow Process Corner: regma/address_8 to address<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y77.AQ       Tcko                  0.283   regma/address<9>
                                                       regma/address_8
    G18.O                net (fanout=1)        0.953   regma/address<8>
    G18.PAD              Tioop                 1.811   address<8>
                                                       address_8_OBUF
                                                       address<8>
    -------------------------------------------------  ---------------------------
    Total                                      3.047ns (2.094ns logic, 0.953ns route)
                                                       (68.7% logic, 31.3% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<8>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<8> (G18.PAD), 1 path
```

```
--------------------------------------------------------------------------------
Delay (fastest paths):  2.785ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_8 (FF)
  Destination:          address<8> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.652ns (Levels of Logic = 1)
  Clock Path Delay:     1.158ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_8
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y77.CLK      net (fanout=368)      0.574   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.158ns (0.353ns logic, 0.805ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_8 to address<8>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y77.AQ       Tcko                  0.115   regma/address<9>
                                                       regma/address_8
    G18.O                net (fanout=1)        0.429   regma/address<8>
    G18.PAD              Tioop                 1.108   address<8>
                                                       address_8_OBUF
                                                       address<8>
    -------------------------------------------------  ---------------------------
    Total                                      1.652ns (1.223ns logic, 0.429ns route)
                                                       (74.0% logic, 26.0% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<7>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.580ns.
--------------------------------------------------------------------------------

Paths for end point address<7> (K19.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.580ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_7 (FF)
  Destination:          address<7> (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.057ns (Levels of Logic = 1)
  Clock Path Delay:     2.498ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y63.CLK      net (fanout=368)      1.396   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.498ns (0.622ns logic, 1.876ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_7 to address<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y63.AQ       Tcko                  0.283   regma/address<7>
                                                       regma/address_7
    K19.O                net (fanout=1)        0.953   regma/address<7>
    K19.PAD              Tioop                 1.821   address<7>
                                                       address_7_OBUF
                                                       address<7>
    -------------------------------------------------  ---------------------------
    Total                                      3.057ns (2.104ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<7>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<7> (K19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.785ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_7 (FF)
  Destination:          address<7> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.660ns (Levels of Logic = 1)
  Clock Path Delay:     1.150ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Minimum Clock Path at Fast Process Corner: clk to regma/address_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y63.CLK      net (fanout=368)      0.566   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.150ns (0.353ns logic, 0.797ns route)
                                                       (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_7 to address<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y63.AQ       Tcko                  0.115   regma/address<7>
                                                       regma/address_7
    K19.O                net (fanout=1)        0.429   regma/address<7>
    K19.PAD              Tioop                 1.116   address<7>
                                                       address_7_OBUF
                                                       address<7>
    -------------------------------------------------  ---------------------------
    Total                                      1.660ns (1.231ns logic, 0.429ns route)
                                                       (74.2% logic, 25.8% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<6>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.605ns.
--------------------------------------------------------------------------------

Paths for end point address<6> (E22.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.605ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_6 (FF)
  Destination:          address<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.082ns (Levels of Logic = 1)
  Clock Path Delay:     2.498ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_6
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.552   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.070   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X0Y56.CLK      net (fanout=368)       1.396   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       2.498ns (0.622ns logic, 1.876ns route)
                                                        (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_6 to address<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X0Y56.AQ       Tcko                   0.283   regma/address<6>
                                                        regma/address_6
    E22.O                net (fanout=1)         0.953   regma/address<6>
    E22.PAD              Tioop                  1.846   address<6>
                                                        address_6_OBUF
                                                        address<6>
    ---------------------------------------------------  ---------------------------
    Total                                       3.082ns (2.129ns logic, 0.953ns route)
                                                        (69.1% logic, 30.9% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<6>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<6> (E22.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.807ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_6 (FF)
  Destination:          address<6> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.682ns (Levels of Logic = 1)
  Clock Path Delay:     1.150ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_6
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                  0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)         0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O               0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X0Y56.CLK      net (fanout=368)       0.566   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                       1.150ns (0.353ns logic, 0.797ns route)
```

```
                                                        (30.7% logic, 69.3% route)

  Minimum Data Path at Fast Process Corner: regma/address_6 to address<6>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y56.AQ       Tcko                  0.115   regma/address<6>
                                                       regma/address_6
    E22.O                net (fanout=1)        0.429   regma/address<6>
    E22.PAD              Tioop                 1.138   address<6>
                                                       address_6_OBUF
                                                       address<6>
    -------------------------------------------------  ---------------------------
    Total                                      1.682ns (1.253ns logic, 0.429ns route)
                                                       (74.5% logic, 25.5% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<5>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.587ns.
--------------------------------------------------------------------------------

Paths for end point address<5> (E20.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.587ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_5 (FF)
  Destination:          address<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.071ns (Levels of Logic = 1)
  Clock Path Delay:     2.491ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y60.CLK      net (fanout=368)      1.389   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.491ns (0.622ns logic, 1.869ns route)
                                                       (25.0% logic, 75.0% route)

  Maximum Data Path at Slow Process Corner: regma/address_5 to address<5>
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y60.AQ       Tcko                  0.283   regma/address<5>
                                                       regma/address_5
    E20.O                net (fanout=1)        0.953   regma/address<5>
    E20.PAD              Tioop                 1.835   address<5>
                                                       address_5_OBUF
                                                       address<5>
    -------------------------------------------------  ---------------------------
    Total                                      3.071ns (2.118ns logic, 0.953ns route)
                                                       (69.0% logic, 31.0% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<5>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<5> (E20.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.792ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_5 (FF)
  Destination:          address<5> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.672ns (Levels of Logic = 1)
  Clock Path Delay:     1.145ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_5
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y60.CLK      net (fanout=368)      0.561   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.145ns (0.353ns logic, 0.792ns route)
                                                       (30.8% logic, 69.2% route)

  Minimum Data Path at Fast Process Corner: regma/address_5 to address<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y60.AQ       Tcko                  0.115   regma/address<5>
                                                       regma/address_5
    E20.O                net (fanout=1)        0.429   regma/address<5>
    E20.PAD              Tioop                 1.128   address<5>
                                                       address_5_OBUF
                                                       address<5>
    -------------------------------------------------  ---------------------------
    Total                                      1.672ns (1.243ns logic, 0.429ns route)
```

```
                                                       (74.3% logic, 25.7% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<4>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.612ns.
--------------------------------------------------------------------------------

Paths for end point address<4> (D22.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.612ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_4 (FF)
  Destination:          address<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.093ns (Levels of Logic = 1)
  Clock Path Delay:     2.494ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y58.CLK      net (fanout=368)      1.392   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.494ns (0.622ns logic, 1.872ns route)
                                                       (24.9% logic, 75.1% route)

  Maximum Data Path at Slow Process Corner: regma/address_4 to address<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y58.AQ       Tcko                  0.283   regma/address<4>
                                                       regma/address_4
    D22.O                net (fanout=1)        0.953   regma/address<4>
    D22.PAD              Tioop                 1.857   address<4>
                                                       address_4_OBUF
                                                       address<4>
    -------------------------------------------------  ---------------------------
    Total                                      3.093ns (2.140ns logic, 0.953ns route)
                                                       (69.2% logic, 30.8% route)

--------------------------------------------------------------------------------
```

```
Fastest Paths: COMP "address<4>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<4> (D22.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.814ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_4 (FF)
  Destination:          address<4> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.692ns (Levels of Logic = 1)
  Clock Path Delay:     1.147ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y58.CLK      net (fanout=368)     0.563   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     1.147ns (0.353ns logic, 0.794ns route)
                                                       (30.8% logic, 69.2% route)

  Minimum Data Path at Fast Process Corner: regma/address_4 to address<4>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y58.AQ       Tcko                 0.115   regma/address<4>
                                                       regma/address_4
    D22.O                net (fanout=1)       0.429   regma/address<4>
    D22.PAD              Tioop                1.148   address<4>
                                                       address_4_OBUF
                                                       address<4>
    -------------------------------------------------  ---------------------------
    Total                                     1.692ns (1.263ns logic, 0.429ns route)
                                                       (74.6% logic, 25.4% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<3>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.592ns.
--------------------------------------------------------------------------------

Paths for end point address<3> (F19.PAD), 1 path
```

```
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.592ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_3 (FF)
  Destination:          address<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.055ns (Levels of Logic = 1)
  Clock Path Delay:     2.512ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y72.CLK      net (fanout=368)      1.410   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.512ns (0.622ns logic, 1.890ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_3 to address<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y72.AQ       Tcko                  0.283   regma/address<3>
                                                       regma/address_3
    F19.O                net (fanout=1)        0.953   regma/address<3>
    F19.PAD              Tioop                 1.819   address<3>
                                                       address_3_OBUF
                                                       address<3>
    -------------------------------------------------  ---------------------------
    Total                                      3.055ns (2.102ns logic, 0.953ns route)
                                                       (68.8% logic, 31.2% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<3>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<3> (F19.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.790ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_3 (FF)
  Destination:          address<3> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.658ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y72.CLK      net (fanout=368)      0.573   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_3 to address<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y72.AQ       Tcko                  0.115   regma/address<3>
                                                       regma/address_3
    F19.O                net (fanout=1)        0.429   regma/address<3>
    F19.PAD              Tioop                 1.114   address<3>
                                                       address_3_OBUF
                                                       address<3>
    -------------------------------------------------  ---------------------------
    Total                                      1.658ns (1.229ns logic, 0.429ns route)
                                                       (74.1% logic, 25.9% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<2>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.544ns.
--------------------------------------------------------------------------------

Paths for end point address<2> (J18.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.544ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_2 (FF)
  Destination:          address<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.008ns (Levels of Logic = 1)
  Clock Path Delay:     2.511ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y71.CLK      net (fanout=368)      1.409   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.511ns (0.622ns logic, 1.889ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_2 to address<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X1Y71.CQ       Tcko                  0.246   regma/address<2>
                                                       regma/address_2
    J18.O                net (fanout=1)        0.953   regma/address<2>
    J18.PAD              Tioop                 1.809   address<2>
                                                       address_2_OBUF
                                                       address<2>
    -------------------------------------------------  ---------------------------
    Total                                      3.008ns (2.055ns logic, 0.953ns route)
                                                       (68.3% logic, 31.7% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<2>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<2> (J18.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.766ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_2 (FF)
  Destination:          address<2> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.634ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y71.CLK      net (fanout=368)      0.573   clk_BUFGP
    ---------------------------------------------------  ---------------------------
    Total                                      1.157ns (0.353ns logic, 0.804ns route)
                                                       (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_2 to address<2>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X1Y71.CQ       Tcko                  0.098   regma/address<2>
                                                       regma/address_2
    J18.O                net (fanout=1)        0.430   regma/address<2>
    J18.PAD              Tioop                 1.106   address<2>
                                                       address_2_OBUF
                                                       address<2>
    ---------------------------------------------------  ---------------------------
    Total                                      1.634ns (1.204ns logic, 0.430ns route)
                                                       (73.7% logic, 26.3% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "address<1>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.606ns.
--------------------------------------------------------------------------------

Paths for end point address<1> (A21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.606ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_1 (FF)
  Destination:          address<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.068ns (Levels of Logic = 1)
  Clock Path Delay:     2.513ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y75.CLK      net (fanout=368)      1.411   clk_BUFGP
```

```
    ----------------------------------------------------  --------------------------
    Total                                           2.513ns (0.622ns logic, 1.891ns route)
                                                            (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_1 to address<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X1Y75.CQ       Tcko                  0.246   regma/address<1>
                                                       regma/address_1
    A21.O                net (fanout=1)        0.953   regma/address<1>
    A21.PAD              Tioop                 1.869   address<1>
                                                       address_1_OBUF
                                                       address<1>
    ----------------------------------------------------  --------------------------
    Total                                           3.068ns (2.115ns logic, 0.953ns route)
                                                            (68.9% logic, 31.1% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<1>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<1> (A21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.818ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_1 (FF)
  Destination:          address<1> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.686ns (Levels of Logic = 1)
  Clock Path Delay:     1.157ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X1Y75.CLK      net (fanout=368)      0.573   clk_BUFGP
    ----------------------------------------------------  --------------------------
    Total                                           1.157ns (0.353ns logic, 0.804ns route)
                                                            (30.5% logic, 69.5% route)

  Minimum Data Path at Fast Process Corner: regma/address_1 to address<1>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X1Y75.CQ       Tcko                  0.098   regma/address<1>
                                                       regma/address_1
    A21.O                net (fanout=1)        0.430   regma/address<1>
```

```
    A21.PAD              Tioop                 1.158   address<1>
                                                        address_1_OBUF
                                                        address<1>
    ------------------------------------------------  --------------------------
    Total                                      1.686ns (1.256ns logic, 0.430ns route)
                                                        (74.5% logic, 25.5% route)

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: COMP "address<0>" OFFSET = OUT 3 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 1 path analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   5.648ns.
--------------------------------------------------------------------------------

Paths for end point address<0> (C21.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  -2.648ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regma/address_0 (FF)
  Destination:          address<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          3.000ns
  Data Path Delay:      3.116ns (Levels of Logic = 1)
  Clock Path Delay:     2.507ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regma/address_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y68.CLK      net (fanout=368)      1.405   clk_BUFGP
    -------------------------------------------------  --------------------------
    Total                                      2.507ns (0.622ns logic, 1.885ns route)
                                                       (24.8% logic, 75.2% route)

  Maximum Data Path at Slow Process Corner: regma/address_0 to address<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y68.AQ       Tcko                  0.283   regma/address<0>
                                                       regma/address_0
    C21.O                net (fanout=1)        0.953   regma/address<0>
    C21.PAD              Tioop                 1.880   address<0>
                                                       address_0_OBUF
                                                       address<0>
```

```
    ------------------------------------------------  ------------------------
    Total                                           3.116ns (2.163ns logic, 0.953ns route)
                                                            (69.4% logic, 30.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "address<0>" OFFSET = OUT 3 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point address<0> (C21.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  2.840ns (clock arrival + clock path + data path - uncertainty)
  Source:               regma/address_0 (FF)
  Destination:          address<0> (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.711ns (Levels of Logic = 1)
  Clock Path Delay:     1.154ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regma/address_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X0Y68.CLK      net (fanout=368)      0.570   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.154ns (0.353ns logic, 0.801ns route)
                                                       (30.6% logic, 69.4% route)

  Minimum Data Path at Fast Process Corner: regma/address_0 to address<0>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X0Y68.AQ       Tcko                  0.115   regma/address<0>
                                                       regma/address_0
    C21.O                net (fanout=1)        0.429   regma/address<0>
    C21.PAD              Tioop                 1.167   address<0>
                                                       address_0_OBUF
                                                       address<0>
    -------------------------------------------------  ---------------------------
    Total                                      1.711ns (1.282ns logic, 0.429ns route)
                                                       (74.9% logic, 25.1% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "read" OFFSET = OUT 2 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 10 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
```

```
 1 timing error detected.
 Minimum allowable offset is   7.211ns.
--------------------------------------------------------------------------------

Paths for end point read (D20.PAD), 10 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -5.211ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          read (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.704ns (Levels of Logic = 4)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd1 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X25Y62.A5      net (fanout=36)       0.279   control1/state_FSM_FFd1
    SLICE_X25Y62.A       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out181_SW0
    SLICE_X25Y62.B3      net (fanout=1)        0.272   N70
    SLICE_X25Y62.B       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out181
    SLICE_X25Y62.C5      net (fanout=4)        0.261   control1/Mmux_c1_out181
    SLICE_X25Y62.C       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out182
    D20.O                net (fanout=1)        1.605   md_rd
    D20.PAD              Tioop                 1.845   read
                                                       read_OBUF
                                                       read
    -------------------------------------------------  ---------------------------
    Total                                      4.704ns (2.287ns logic, 2.417ns route)
                                                       (48.6% logic, 51.4% route)
```

```
--------------------------------------------------------------------------------
Slack (slowest paths):  -5.173ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               control1/state_FSM_FFd2 (FF)
  Destination:          read (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.666ns (Levels of Logic = 4)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.482ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      1.380   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.482ns (0.622ns logic, 1.860ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: control1/state_FSM_FFd2 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.BQ      Tcko                  0.283   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd2
    SLICE_X25Y62.A6      net (fanout=35)       0.241   control1/state_FSM_FFd2
    SLICE_X25Y62.A       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out181_SW0
    SLICE_X25Y62.B3      net (fanout=1)        0.272   N70
    SLICE_X25Y62.B       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out181
    SLICE_X25Y62.C5      net (fanout=4)        0.261   control1/Mmux_c1_out181
    SLICE_X25Y62.C       Tilo                  0.053   regir/ir<24>
                                                       control1/Mmux_c1_out182
    D20.O                net (fanout=1)        1.605   md_rd
    D20.PAD              Tioop                 1.845   read
                                                       read_OBUF
                                                       read
    -------------------------------------------------  ---------------------------
    Total                                      4.666ns (2.287ns logic, 2.379ns route)
                                                       (49.0% logic, 51.0% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -5.117ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_31 (FF)
  Destination:          read (PAD)
```

```
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.613ns (Levels of Logic = 3)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.479ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)     1.377   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                     2.479ns (0.622ns logic, 1.857ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_31 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                 0.283   regir/ir<26>
                                                       regir/ir_31
    SLICE_X25Y62.B2      net (fanout=40)      0.513   regir/ir<31>
    SLICE_X25Y62.B       Tilo                 0.053   regir/ir<24>
                                                       control1/Mmux_c1_out181
    SLICE_X25Y62.C5      net (fanout=4)       0.261   control1/Mmux_c1_out181
    SLICE_X25Y62.C       Tilo                 0.053   regir/ir<24>
                                                       control1/Mmux_c1_out182
    D20.O                net (fanout=1)       1.605   md_rd
    D20.PAD              Tioop                1.845   read
                                                       read_OBUF
                                                       read
    -------------------------------------------------  ---------------------------
    Total                                     4.613ns (2.234ns logic, 2.379ns route)
                                                       (48.4% logic, 51.6% route)

--------------------------------------------------------------------------------

Fastest Paths: COMP "read" OFFSET = OUT 2 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point read (D20.PAD), 10 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.517ns (clock arrival + clock path + data path - uncertainty)
  Source:               control1/state_FSM_FFd1 (FF)
  Destination:          read (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.403ns (Levels of Logic = 2)
  Clock Path Delay:     1.139ns (Levels of Logic = 2)
```

```
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      0.555   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.139ns (0.353ns logic, 0.786ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: control1/state_FSM_FFd1 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.AQ      Tcko                  0.115   control1/state_FSM_FFd2
                                                       control1/state_FSM_FFd1
    SLICE_X25Y62.C1      net (fanout=36)       0.250   control1/state_FSM_FFd1
    SLICE_X25Y62.C       Tilo                  0.034   regir/ir<24>
                                                       control1/Mmux_c1_out182
    D20.O                net (fanout=1)        0.867   md_rd
    D20.PAD              Tioop                 1.137   read
                                                       read_OBUF
                                                       read
    -------------------------------------------------  ---------------------------
    Total                                      2.403ns (1.286ns logic, 1.117ns route)
                                                       (53.5% logic, 46.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.495ns (clock arrival + clock path + data path - uncertainty)
  Source:               control1/state_FSM_FFd3 (FF)
  Destination:          read (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.383ns (Levels of Logic = 2)
  Clock Path Delay:     1.137ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
```

```
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      0.553   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.137ns (0.353ns logic, 0.784ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: control1/state_FSM_FFd3 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y60.CQ      Tcko                  0.098   control1/state_FSM_FFd3
                                                        control1/state_FSM_FFd3
    SLICE_X25Y62.C4      net (fanout=36)       0.247   control1/state_FSM_FFd3
    SLICE_X25Y62.C       Tilo                  0.034   regir/ir<24>
                                                        control1/Mmux_c1_out182
    D20.O                net (fanout=1)        0.867   md_rd
    D20.PAD              Tioop                 1.137   read
                                                        read_OBUF
                                                        read
    -------------------------------------------------  ---------------------------
    Total                                      2.383ns (1.269ns logic, 1.114ns route)
                                                       (53.3% logic, 46.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.491ns (clock arrival + clock path + data path - uncertainty)
  Source:               control1/state_FSM_FFd2 (FF)
  Destination:          read (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.377ns (Levels of Logic = 2)
  Clock Path Delay:     1.139ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                        clk
                                                        clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                        clk_BUFGP/BUFG
    SLICE_X26Y61.CLK     net (fanout=368)      0.555   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.139ns (0.353ns logic, 0.786ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: control1/state_FSM_FFd2 to read
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X26Y61.BQ      Tcko                  0.115   control1/state_FSM_FFd2
```

```
                                                       control1/state_FSM_FFd2
    SLICE_X25Y62.C3      net (fanout=35)       0.224   control1/state_FSM_FFd2
    SLICE_X25Y62.C       Tilo                  0.034   regir/ir<24>
                                                       control1/Mmux_c1_out182
    D20.O                net (fanout=1)        0.867   md_rd
    D20.PAD              Tioop                 1.137   read
                                                       read_OBUF
                                                       read
    ------------------------------------------------  ---------------------------
    Total                                      2.377ns (1.286ns logic, 1.091ns route)
                                                       (54.1% logic, 45.9% route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: COMP "write" OFFSET = OUT 2 ns AFTER COMP "clk";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 8 paths analyzed, 1 endpoint analyzed, 1 failing endpoint
 1 timing error detected.
 Minimum allowable offset is   7.228ns.
--------------------------------------------------------------------------------

Paths for end point write (J19.PAD), 8 paths
--------------------------------------------------------------------------------
Slack (slowest paths):  -5.228ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_28 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.726ns (Levels of Logic = 3)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_28
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_28 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    SLICE_X24Y61.BQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_28
    SLICE_X25Y61.C5      net (fanout=39)       0.360   regir/ir<28>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X27Y61.D2      net (fanout=3)        0.486   control1/Mmux_c1_out1132
    SLICE_X27Y61.D       Tilo                  0.053   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
    J19.O                net (fanout=1)        1.685   md_wr
    J19.PAD              Tioop                 1.806   write
                                                       write_OBUF
                                                       write
    -------------------------------------------------  ---------------------------
    Total                                      4.726ns (2.195ns logic, 2.531ns route)
                                                       (46.4% logic, 53.6% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -5.082ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_27 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.580ns (Levels of Logic = 3)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_27
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X25Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_27 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X25Y61.BQ      Tcko                  0.246   regir/ir_29_1
                                                       regir/ir_27
    SLICE_X25Y61.C4      net (fanout=35)       0.251   regir/ir<27>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X27Y61.D2      net (fanout=3)        0.486   control1/Mmux_c1_out1132
    SLICE_X27Y61.D       Tilo                  0.053   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
```

```
    J19.O                net (fanout=1)        1.685   md_wr
    J19.PAD              Tioop                 1.806   write
                                                       write_OBUF
                                                       write
    ------------------------------------------------  ---------------------------
    Total                                      4.580ns (2.158ns logic, 2.422ns route)
                                                       (47.1% logic, 52.9% route)

--------------------------------------------------------------------------------
Slack (slowest paths):  -5.005ns (requirement - (clock arrival + clock path + data path +
uncertainty))
  Source:               regir/ir_29 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Requirement:          2.000ns
  Data Path Delay:      4.503ns (Levels of Logic = 3)(Component delays alone exceeds
constraint)
  Clock Path Delay:     2.477ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Clock Path at Slow Process Corner: clk to regir/ir_29
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.552   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.480   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.070   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y61.CLK     net (fanout=368)      1.375   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      2.477ns (0.622ns logic, 1.855ns route)
                                                       (25.1% logic, 74.9% route)

  Maximum Data Path at Slow Process Corner: regir/ir_29 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y61.DQ      Tcko                  0.283   regir/ir<29>
                                                       regir/ir_29
    SLICE_X25Y61.C6      net (fanout=40)       0.137   regir/ir<29>
    SLICE_X25Y61.C       Tilo                  0.053   regir/ir_29_1
                                                       control1/Mmux_c1_out11321
    SLICE_X27Y61.D2      net (fanout=3)        0.486   control1/Mmux_c1_out1132
    SLICE_X27Y61.D       Tilo                  0.053   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
    J19.O                net (fanout=1)        1.685   md_wr
    J19.PAD              Tioop                 1.806   write
                                                       write_OBUF
                                                       write
    -------------------------------------------------  ---------------------------
    Total                                      4.503ns (2.195ns logic, 2.308ns route)
                                                       (48.7% logic, 51.3% route)
```

```
--------------------------------------------------------------------------------

Fastest Paths: COMP "write" OFFSET = OUT 2 ns AFTER COMP "clk";
--------------------------------------------------------------------------------

Paths for end point write (J19.PAD), 8 paths
--------------------------------------------------------------------------------
Delay (fastest paths):  3.424ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_30 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.309ns (Levels of Logic = 2)
  Clock Path Delay:     1.140ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_30
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y62.CLK     net (fanout=368)      0.556   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.140ns (0.353ns logic, 0.787ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_30 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X27Y62.CQ      Tcko                  0.098   regir/ir_28_1
                                                       regir/ir_30
    SLICE_X27Y61.D4      net (fanout=39)       0.188   regir/ir<30>
    SLICE_X27Y61.D       Tilo                  0.034   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
    J19.O                net (fanout=1)        0.885   md_wr
    J19.PAD              Tioop                 1.104   write
                                                       write_OBUF
                                                       write
    -------------------------------------------------  ---------------------------
    Total                                      2.309ns (1.236ns logic, 1.073ns route)
                                                       (53.5% logic, 46.5% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.420ns (clock arrival + clock path + data path - uncertainty)
  Source:               regir/ir_31 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.307ns (Levels of Logic = 2)
  Clock Path Delay:     1.138ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns
```

```
  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to regir/ir_31
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X24Y62.CLK     net (fanout=368)      0.554   clk_BUFGP
    -------------------------------------------------  ---------------------------
    Total                                      1.138ns (0.353ns logic, 0.785ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: regir/ir_31 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y62.AQ      Tcko                  0.115   regir/ir<26>
                                                       regir/ir_31
    SLICE_X27Y61.D5      net (fanout=40)       0.169   regir/ir<31>
    SLICE_X27Y61.D       Tilo                  0.034   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
    J19.O                net (fanout=1)        0.885   md_wr
    J19.PAD              Tioop                 1.104   write
                                                       write_OBUF
                                                       write
    -------------------------------------------------  ---------------------------
    Total                                      2.307ns (1.253ns logic, 1.054ns route)
                                                       (54.3% logic, 45.7% route)

--------------------------------------------------------------------------------
Delay (fastest paths):  3.364ns (clock arrival + clock path + data path - uncertainty)
  Source:               control1/state_FSM_FFd3 (FF)
  Destination:          write (PAD)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Data Path Delay:      2.252ns (Levels of Logic = 2)
  Clock Path Delay:     1.137ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Clock Path at Fast Process Corner: clk to control1/state_FSM_FFd3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.320   clk
                                                       clk
                                                       clk_BUFGP/IBUFG
```

```
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.231   clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.033   clk_BUFGP/BUFG
                                                       clk_BUFGP/BUFG
    SLICE_X27Y60.CLK     net (fanout=368)      0.553   clk_BUFGP
    ------------------------------------------------  ---------------------------
    Total                                      1.137ns (0.353ns logic, 0.784ns route)
                                                       (31.0% logic, 69.0% route)

  Minimum Data Path at Fast Process Corner: control1/state_FSM_FFd3 to write
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X27Y60.CQ      Tcko                  0.098   control1/state_FSM_FFd3
                                                       control1/state_FSM_FFd3
    SLICE_X27Y61.D6      net (fanout=36)       0.131   control1/state_FSM_FFd3
    SLICE_X27Y61.D       Tilo                  0.034   regfile1/reg0<30>
                                                       control1/Mmux_md_wr31
    J19.O                net (fanout=1)        0.885   md_wr
    J19.PAD              Tioop                 1.104   write
                                                       write_OBUF
                                                       write
    ------------------------------------------------  ---------------------------
    Total                                      2.252ns (1.236ns logic, 1.016ns route)
                                                       (54.9% logic, 45.1% route)

--------------------------------------------------------------------------------


67 constraints not met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock clk
------------+------------+------------+------------+------------+------------------+--------
+
            |Max Setup to|  Process   |Max Hold to |  Process   |                  |
Clock  |
Source      | clk (edge) |   Corner   | clk (edge) |   Corner   |Internal Clock(s) |
Phase  |
------------+------------+------------+------------+------------+------------------+--------
+
d<0>        |    0.733(R)|      FAST  |    0.246(R)|      SLOW  |clk_BUFGP         |
0.000|
d<1>        |    0.920(R)|      FAST  |    0.091(R)|      SLOW  |clk_BUFGP         |
0.000|
d<2>        |    0.872(R)|      FAST  |    0.153(R)|      SLOW  |clk_BUFGP         |
0.000|
d<3>        |    0.617(R)|      FAST  |    0.322(R)|      SLOW  |clk_BUFGP         |
0.000|
d<4>        |    0.199(R)|      FAST  |    0.879(R)|      SLOW  |clk_BUFGP         |
0.000|
d<5>        |    0.425(R)|      FAST  |    0.589(R)|      SLOW  |clk_BUFGP         |
0.000|
d<6>        |    0.786(R)|      FAST  |    0.265(R)|      SLOW  |clk_BUFGP         |
0.000|
d<7>        |    0.795(R)|      FAST  |    0.198(R)|      SLOW  |clk_BUFGP         |
0.000|
d<8>        |    0.955(R)|      FAST  |    0.002(R)|      SLOW  |clk_BUFGP         |
```

```
0.000|
d<9>        |    0.819(R)|      FAST  |    0.195(R)|      SLOW  |clk_BUFGP         |
0.000|
d<10>       |    0.869(R)|      FAST  |    0.158(R)|      SLOW  |clk_BUFGP         |
0.000|
d<11>       |    0.860(R)|      FAST  |    0.147(R)|      SLOW  |clk_BUFGP         |
0.000|
d<12>       |    0.890(R)|      FAST  |    0.104(R)|      SLOW  |clk_BUFGP         |
0.000|
d<13>       |    0.881(R)|      FAST  |    0.081(R)|      SLOW  |clk_BUFGP         |
0.000|
d<14>       |    0.805(R)|      FAST  |    0.139(R)|      SLOW  |clk_BUFGP         |
0.000|
d<15>       |    0.887(R)|      FAST  |    0.101(R)|      SLOW  |clk_BUFGP         |
0.000|
d<16>       |    0.851(R)|      FAST  |    0.154(R)|      SLOW  |clk_BUFGP         |
0.000|
d<17>       |    0.993(R)|      FAST  |    0.052(R)|      SLOW  |clk_BUFGP         |
0.000|
d<18>       |    0.791(R)|      FAST  |    0.209(R)|      SLOW  |clk_BUFGP         |
0.000|
d<19>       |    0.904(R)|      FAST  |    0.066(R)|      SLOW  |clk_BUFGP         |
0.000|
d<20>       |    0.968(R)|      FAST  |    0.036(R)|      SLOW  |clk_BUFGP         |
0.000|
d<21>       |    0.872(R)|      FAST  |    0.125(R)|      SLOW  |clk_BUFGP         |
0.000|
d<22>       |    1.004(R)|      FAST  |   -0.066(R)|      SLOW  |clk_BUFGP         |
0.000|
d<23>       |    1.045(R)|      FAST  |   -0.114(R)|      SLOW  |clk_BUFGP         |
0.000|
d<24>       |    0.798(R)|      FAST  |    0.220(R)|      SLOW  |clk_BUFGP         |
0.000|
d<25>       |    1.256(R)|      FAST  |   -0.314(R)|      SLOW  |clk_BUFGP         |
0.000|
d<26>       |    0.919(R)|      FAST  |    0.057(R)|      SLOW  |clk_BUFGP         |
0.000|
d<27>       |    0.688(R)|      FAST  |    0.326(R)|      SLOW  |clk_BUFGP         |
0.000|
d<28>       |    0.924(R)|      FAST  |    0.065(R)|      SLOW  |clk_BUFGP         |
0.000|
d<29>       |    0.963(R)|      FAST  |    0.006(R)|      SLOW  |clk_BUFGP         |
0.000|
d<30>       |    1.929(R)|      SLOW  |   -0.999(R)|      SLOW  |clk_BUFGP         |
0.000|
d<31>       |    0.942(R)|      FAST  |    0.061(R)|      SLOW  |clk_BUFGP         |
0.000|
done        |    0.903(R)|      SLOW  |    0.856(R)|      SLOW  |clk_BUFGP         |
0.000|
------------+------------+------------+------------+------------+------------------+--------
+

Clock clk to Pad
------------+-----------------+------------+-----------------+------------+-----------------
-+--------+
            |Max (slowest) clk|  Process   |Min (fastest) clk|  Process
|                 | Clock  |
Destination |  (edge) to PAD  |   Corner   |  (edge) to PAD  |   Corner   |Internal
Clock(s) | Phase  |
------------+-----------------+------------+-----------------+------------+-----------------
-+--------+
```

address<0>	5.648(R)	SLOW	2.840(R)	FAST	
clk_BUFGP	0.000				
address<1>	5.606(R)	SLOW	2.818(R)	FAST	
clk_BUFGP	0.000				
address<2>	5.544(R)	SLOW	2.766(R)	FAST	
clk_BUFGP	0.000				
address<3>	5.592(R)	SLOW	2.790(R)	FAST	
clk_BUFGP	0.000				
address<4>	5.612(R)	SLOW	2.814(R)	FAST	
clk_BUFGP	0.000				
address<5>	5.587(R)	SLOW	2.792(R)	FAST	
clk_BUFGP	0.000				
address<6>	5.605(R)	SLOW	2.807(R)	FAST	
clk_BUFGP	0.000				
address<7>	5.580(R)	SLOW	2.785(R)	FAST	
clk_BUFGP	0.000				
address<8>	5.586(R)	SLOW	2.785(R)	FAST	
clk_BUFGP	0.000				
address<9>	5.622(R)	SLOW	2.812(R)	FAST	
clk_BUFGP	0.000				
address<10>	5.590(R)	SLOW	2.788(R)	FAST	
clk_BUFGP	0.000				
address<11>	5.626(R)	SLOW	2.816(R)	FAST	
clk_BUFGP	0.000				
address<12>	5.544(R)	SLOW	2.767(R)	FAST	
clk_BUFGP	0.000				
address<13>	5.546(R)	SLOW	2.765(R)	FAST	
clk_BUFGP	0.000				
address<14>	5.563(R)	SLOW	2.786(R)	FAST	
clk_BUFGP	0.000				
address<15>	5.575(R)	SLOW	2.777(R)	FAST	
clk_BUFGP	0.000				
address<16>	5.612(R)	SLOW	2.823(R)	FAST	
clk_BUFGP	0.000				
address<17>	5.634(R)	SLOW	2.825(R)	FAST	
clk_BUFGP	0.000				
address<18>	5.562(R)	SLOW	2.783(R)	FAST	
clk_BUFGP	0.000				
address<19>	5.671(R)	SLOW	2.832(R)	FAST	
clk_BUFGP	0.000				
address<20>	5.545(R)	SLOW	2.768(R)	FAST	
clk_BUFGP	0.000				
address<21>	5.584(R)	SLOW	2.785(R)	FAST	
clk_BUFGP	0.000				
address<22>	5.580(R)	SLOW	2.797(R)	FAST	
clk_BUFGP	0.000				
address<23>	5.543(R)	SLOW	2.765(R)	FAST	
clk_BUFGP	0.000				
address<24>	5.614(R)	SLOW	2.813(R)	FAST	
clk_BUFGP	0.000				
address<25>	5.588(R)	SLOW	2.787(R)	FAST	
clk_BUFGP	0.000				
address<26>	5.610(R)	SLOW	2.806(R)	FAST	
clk_BUFGP	0.000				
address<27>	5.540(R)	SLOW	2.762(R)	FAST	
clk_BUFGP	0.000				
address<28>	5.600(R)	SLOW	2.799(R)	FAST	
clk_BUFGP	0.000				
address<29>	5.607(R)	SLOW	2.801(R)	FAST	
clk_BUFGP	0.000				
address<30>	5.610(R)	SLOW	2.806(R)	FAST	

|clk_BUFGP | 0.000|
address<31> | 5.590(R)| SLOW | 2.789(R)| FAST
|clk_BUFGP | 0.000|
d<0> | 7.202(R)| SLOW | 3.037(R)| FAST
|clk_BUFGP | 0.000|
d<1> | 7.067(R)| SLOW | 3.017(R)| FAST
|clk_BUFGP | 0.000|
d<2> | 7.081(R)| SLOW | 2.984(R)| FAST
|clk_BUFGP | 0.000|
d<3> | 7.175(R)| SLOW | 3.124(R)| FAST
|clk_BUFGP | 0.000|
d<4> | 8.031(R)| SLOW | 3.245(R)| FAST
|clk_BUFGP | 0.000|
d<5> | 8.010(R)| SLOW | 3.402(R)| FAST
|clk_BUFGP | 0.000|
d<6> | 7.137(R)| SLOW | 2.968(R)| FAST
|clk_BUFGP | 0.000|
d<7> | 7.136(R)| SLOW | 2.928(R)| FAST
|clk_BUFGP | 0.000|
d<8> | 7.229(R)| SLOW | 2.964(R)| FAST
|clk_BUFGP | 0.000|
d<9> | 7.323(R)| SLOW | 2.958(R)| FAST
|clk_BUFGP | 0.000|
d<10> | 7.086(R)| SLOW | 2.967(R)| FAST
|clk_BUFGP | 0.000|
d<11> | 7.440(R)| SLOW | 2.980(R)| FAST
|clk_BUFGP | 0.000|
d<12> | 7.346(R)| SLOW | 2.961(R)| FAST
|clk_BUFGP | 0.000|
d<13> | 7.365(R)| SLOW | 2.959(R)| FAST
|clk_BUFGP | 0.000|
d<14> | 7.456(R)| SLOW | 2.956(R)| FAST
|clk_BUFGP | 0.000|
d<15> | 7.277(R)| SLOW | 2.979(R)| FAST
|clk_BUFGP | 0.000|
d<16> | 7.363(R)| SLOW | 2.973(R)| FAST
|clk_BUFGP | 0.000|
d<17> | 7.037(R)| SLOW | 2.850(R)| FAST
|clk_BUFGP | 0.000|
d<18> | 7.097(R)| SLOW | 2.793(R)| FAST
|clk_BUFGP | 0.000|
d<19> | 7.230(R)| SLOW | 2.904(R)| FAST
|clk_BUFGP | 0.000|
d<20> | 6.920(R)| SLOW | 2.947(R)| FAST
|clk_BUFGP | 0.000|
d<21> | 7.122(R)| SLOW | 2.849(R)| FAST
|clk_BUFGP | 0.000|
d<22> | 7.212(R)| SLOW | 2.844(R)| FAST
|clk_BUFGP | 0.000|
d<23> | 7.007(R)| SLOW | 2.824(R)| FAST
|clk_BUFGP | 0.000|
d<24> | 7.005(R)| SLOW | 2.905(R)| FAST
|clk_BUFGP | 0.000|
d<25> | 7.302(R)| SLOW | 2.952(R)| FAST
|clk_BUFGP | 0.000|
d<26> | 7.259(R)| SLOW | 2.946(R)| FAST
|clk_BUFGP | 0.000|
d<27> | 7.270(R)| SLOW | 2.950(R)| FAST
|clk_BUFGP | 0.000|
d<28> | 7.234(R)| SLOW | 3.012(R)| FAST
|clk_BUFGP | 0.000|

```
d<29>       |         6.917(R)|      SLOW  |         3.010(R)|      FAST
|clk_BUFGP         |   0.000|
d<30>       |         7.028(R)|      SLOW  |         2.962(R)|      FAST
|clk_BUFGP         |   0.000|
d<31>       |         7.127(R)|      SLOW  |         2.980(R)|      FAST
|clk_BUFGP         |   0.000|
read        |         7.211(R)|      SLOW  |         3.491(R)|      FAST
|clk_BUFGP         |   0.000|
write       |         7.228(R)|      SLOW  |         3.364(R)|      FAST
|clk_BUFGP         |   0.000|
------------+-----------------+------------+-----------------+------------+----------------
-+--------+

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    7.211|         |         |         |
---------------+---------+---------+---------+---------+

COMP "d<31>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.003; Ideal Clock Offset To Actual Clock -0.559;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<31>             |    0.942(R)|      FAST  |    0.061(R)|      SLOW  |    2.058|
0.939|        0.559|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.942|         -  |       0.061|         -  |    2.058|
0.939|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<30>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.930; Ideal Clock Offset To Actual Clock 0.464;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<30>             |    1.929(R)|      SLOW  |   -0.999(R)|      SLOW  |    1.071|
1.999|       -0.464|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       1.929|         -  |      -0.999|         -  |    1.071|
1.999|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<29>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.969; Ideal Clock Offset To Actual Clock -0.522;
```

```
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<29>             |    0.963(R)|      FAST  |    0.006(R)|      SLOW  |    2.037|
0.994|        0.522|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.963|         -  |       0.006|         -  |    2.037|
0.994|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<28>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.989; Ideal Clock Offset To Actual Clock -0.571;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<28>             |    0.924(R)|      FAST  |    0.065(R)|      SLOW  |    2.076|
0.935|        0.571|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.924|         -  |       0.065|         -  |    2.076|
0.935|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<27>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.014; Ideal Clock Offset To Actual Clock -0.819;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<27>             |    0.688(R)|      FAST  |    0.326(R)|      SLOW  |    2.312|
0.674|        0.819|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.688|         -  |       0.326|         -  |    2.312|
0.674|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<26>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.976; Ideal Clock Offset To Actual Clock -0.569;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
```

```
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<26>             |    0.919(R)|      FAST  |    0.057(R)|      SLOW  |    2.081|
0.943|        0.569|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.919|         -  |       0.057|         -  |    2.081|
0.943|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<25>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.942; Ideal Clock Offset To Actual Clock -0.215;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<25>             |    1.256(R)|      FAST  |   -0.314(R)|      SLOW  |    1.744|
1.314|        0.215|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       1.256|         -  |      -0.314|         -  |    1.744|
1.314|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<24>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.018; Ideal Clock Offset To Actual Clock -0.711;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<24>             |    0.798(R)|      FAST  |    0.220(R)|      SLOW  |    2.202|
0.780|        0.711|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.798|         -  |       0.220|         -  |    2.202|
0.780|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<23>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.931; Ideal Clock Offset To Actual Clock -0.421;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
```

```
d<23>              |    1.045(R)|      FAST  |   -0.114(R)|      SLOW  |    1.955|
1.114|        0.421|
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       1.045|         -  |      -0.114|         -  |    1.955|
1.114|             |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<22>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.938; Ideal Clock Offset To Actual Clock -0.465;
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
                   |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source             |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<22>              |    1.004(R)|      FAST  |   -0.066(R)|      SLOW  |    1.996|
1.066|        0.465|
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       1.004|         -  |      -0.066|         -  |    1.996|
1.066|             |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<21>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.997; Ideal Clock Offset To Actual Clock -0.627;
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
                   |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source             |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<21>              |    0.872(R)|      FAST  |    0.125(R)|      SLOW  |    2.128|
0.875|        0.627|
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.872|         -  |       0.125|         -  |    2.128|
0.875|             |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<20>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.004; Ideal Clock Offset To Actual Clock -0.534;
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
                   |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source             |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<20>              |    0.968(R)|      FAST  |    0.036(R)|      SLOW  |    2.032|
0.964|        0.534|
-------------------+------------+------------+------------+------------+---------+---------+-
------------+
```

```
Worst Case Summary|       0.968|         -  |       0.036|         -  |    2.032|
0.964|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<19>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.970; Ideal Clock Offset To Actual Clock -0.581;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<19>             |    0.904(R)|      FAST  |    0.066(R)|      SLOW  |    2.096|
0.934|        0.581|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.904|         -  |       0.066|         -  |    2.096|
0.934|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<18>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.000; Ideal Clock Offset To Actual Clock -0.709;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<18>             |    0.791(R)|      FAST  |    0.209(R)|      SLOW  |    2.209|
0.791|        0.709|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.791|         -  |       0.209|         -  |    2.209|
0.791|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<17>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.045; Ideal Clock Offset To Actual Clock -0.530;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<17>             |    0.993(R)|      FAST  |    0.052(R)|      SLOW  |    2.007|
0.948|        0.530|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.993|         -  |       0.052|         -  |    2.007|
0.948|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
```

COMP "d<16>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.005; Ideal Clock Offset To Actual Clock -0.652;

		Process		Process	Setup	Hold	Source Offset
Source	Setup	Corner	Hold	Corner	Slack	Slack	To Center
d<16>	0.851(R)	FAST	0.154(R)	SLOW	2.149	0.846	0.652
Worst Case Summary	0.851	-	0.154	-	2.149	0.846	

COMP "d<15>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.988; Ideal Clock Offset To Actual Clock -0.607;

		Process		Process	Setup	Hold	Source Offset
Source	Setup	Corner	Hold	Corner	Slack	Slack	To Center
d<15>	0.887(R)	FAST	0.101(R)	SLOW	2.113	0.899	0.607
Worst Case Summary	0.887	-	0.101	-	2.113	0.899	

COMP "d<14>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.944; Ideal Clock Offset To Actual Clock -0.667;

		Process		Process	Setup	Hold	Source Offset
Source	Setup	Corner	Hold	Corner	Slack	Slack	To Center
d<14>	0.805(R)	FAST	0.139(R)	SLOW	2.195	0.861	0.667
Worst Case Summary	0.805	-	0.139	-	2.195	0.861	

COMP "d<13>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.962; Ideal Clock Offset To Actual Clock -0.600;

```
------------+
                 |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source           |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
d<13>            |    0.881(R)|      FAST  |    0.081(R)|      SLOW  |    2.119|
0.919|        0.600|
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.881|         -  |       0.081|         -  |    2.119|
0.919|             |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<12>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.994; Ideal Clock Offset To Actual Clock -0.607;
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
                 |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source           |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
d<12>            |    0.890(R)|      FAST  |    0.104(R)|      SLOW  |    2.110|
0.896|        0.607|
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.890|         -  |       0.104|         -  |    2.110|
0.896|             |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<11>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.007; Ideal Clock Offset To Actual Clock -0.644;
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
                 |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source           |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
d<11>            |    0.860(R)|      FAST  |    0.147(R)|      SLOW  |    2.140|
0.853|        0.644|
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.860|         -  |       0.147|         -  |    2.140|
0.853|             |
-----------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<10>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.027; Ideal Clock Offset To Actual Clock -0.644;
-----------------+------------+------------+------------+------------+---------+---------+-
------------+
                 |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source           |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
```

```
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<10>             |    0.869(R)|      FAST  |    0.158(R)|      SLOW  |    2.131|
0.842|        0.644|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.869|         -  |       0.158|         -  |    2.131|
0.842|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<9>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.014; Ideal Clock Offset To Actual Clock -0.688;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<9>              |    0.819(R)|      FAST  |    0.195(R)|      SLOW  |    2.181|
0.805|        0.688|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.819|         -  |       0.195|         -  |    2.181|
0.805|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<8>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.957; Ideal Clock Offset To Actual Clock -0.524;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<8>              |    0.955(R)|      FAST  |    0.002(R)|      SLOW  |    2.045|
0.998|        0.524|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.955|         -  |       0.002|         -  |    2.045|
0.998|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<7>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.993; Ideal Clock Offset To Actual Clock -0.702;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<7>              |    0.795(R)|      FAST  |    0.198(R)|      SLOW  |    2.205|
```

```
0.802|        0.702|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.795|         -  |       0.198|         -  |    2.205|
0.802|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<6>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.051; Ideal Clock Offset To Actual Clock -0.740;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<6>              |    0.786(R)|      FAST  |    0.265(R)|      SLOW  |    2.214|
0.735|        0.740|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.786|         -  |       0.265|         -  |    2.214|
0.735|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<5>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.014; Ideal Clock Offset To Actual Clock -1.082;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<5>              |    0.425(R)|      FAST  |    0.589(R)|      SLOW  |    2.575|
0.411|        1.082|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.425|         -  |       0.589|         -  |    2.575|
0.411|             |
------------------+------------+------------+------------+------------+---------+---------+-
------------+

COMP "d<4>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.078; Ideal Clock Offset To Actual Clock -1.340;
------------------+------------+------------+------------+------------+---------+---------+-
------------+
                  |            |  Process   |            |  Process   |  Setup  |  Hold
|Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack
|  To Center  |
------------------+------------+------------+------------+------------+---------+---------+-
------------+
d<4>              |    0.199(R)|      FAST  |    0.879(R)|      SLOW  |    2.801|
0.121|        1.340|
------------------+------------+------------+------------+------------+---------+---------+-
------------+
Worst Case Summary|       0.199|         -  |       0.879|         -  |    2.801|
```

```
0.121|             |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+

COMP "d<3>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.939; Ideal Clock Offset To Actual Clock -0.853;
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
                 |           |  Process  |           |  Process  |  Setup  |  Hold
|Source Offset|
Source           |   Setup   |   Corner  |    Hold   |   Corner  |  Slack  |  Slack
|  To Center  |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
d<3>             |    0.617(R)|      FAST  |    0.322(R)|      SLOW  |    2.383|
0.678|        0.853|
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
Worst Case Summary|       0.617|         -  |       0.322|         -  |    2.383|
0.678|             |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+

COMP "d<2>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.025; Ideal Clock Offset To Actual Clock -0.641;
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
                 |           |  Process  |           |  Process  |  Setup  |  Hold
|Source Offset|
Source           |   Setup   |   Corner  |    Hold   |   Corner  |  Slack  |  Slack
|  To Center  |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
d<2>             |    0.872(R)|      FAST  |    0.153(R)|      SLOW  |    2.128|
0.847|        0.641|
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
Worst Case Summary|       0.872|         -  |       0.153|         -  |    2.128|
0.847|             |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+

COMP "d<1>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.011; Ideal Clock Offset To Actual Clock -0.586;
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
                 |           |  Process  |           |  Process  |  Setup  |  Hold
|Source Offset|
Source           |   Setup   |   Corner  |    Hold   |   Corner  |  Slack  |  Slack
|  To Center  |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
d<1>             |    0.920(R)|      FAST  |    0.091(R)|      SLOW  |    2.080|
0.909|        0.586|
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
Worst Case Summary|       0.920|         -  |       0.091|         -  |    2.080|
0.909|             |
-----------------+-----------+-----------+-----------+-----------+---------+---------+-
-----------+
```

COMP "d<0>" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 0.979; Ideal Clock Offset To Actual Clock -0.756;

Source	Setup	Process Corner	Hold	Process Corner	Setup Slack	Hold Slack	Source Offset To Center
d<0>	0.733(R)	FAST	0.246(R)	SLOW	2.267	0.754	0.756
Worst Case Summary	0.733	-	0.246	-	2.267	0.754	

COMP "done" OFFSET = IN 3 ns VALID 4 ns BEFORE COMP "clk" "RISING";
Worst Case Data Window 1.759; Ideal Clock Offset To Actual Clock -0.977;

Source	Setup	Process Corner	Hold	Process Corner	Setup Slack	Hold Slack	Source Offset To Center
done	0.903(R)	SLOW	0.856(R)	SLOW	2.097	0.144	0.977
Worst Case Summary	0.903	-	0.856	-	2.097	0.144	

COMP "d<31>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

Process PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<31>	7.127	SLOW	2.980	FAST	0.000

COMP "d<30>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

Process PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)

```
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<30>                                          |        7.028|      SLOW  |
2.962|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<29>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<29>                                          |        6.917|      SLOW  |
3.010|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<28>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<28>                                          |        7.234|      SLOW  |
3.012|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<27>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<27>                                          |        7.270|      SLOW  |
2.950|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<26>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
```

```
---------+--------------+
d<26>                                             |        7.259|      SLOW  |
2.946|      FAST  |         0.000|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<25>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<25>                                             |        7.302|      SLOW  |
2.952|      FAST  |         0.000|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<24>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<24>                                             |        7.005|      SLOW  |
2.905|      FAST  |         0.000|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<23>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<23>                                             |        7.007|      SLOW  |
2.824|      FAST  |         0.000|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<22>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
--------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
```

```
d<22>                                              |        7.212|      SLOW  |
2.844|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<21>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                   |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                                | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<21>                                              |        7.122|      SLOW  |
2.849|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<20>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                   |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                                | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<20>                                              |        6.920|      SLOW  |
2.947|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<19>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                   |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                                | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<19>                                              |        7.230|      SLOW  |
2.904|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "d<18>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                   |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                                | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
d<18>                                              |        7.097|      SLOW  |
```

```
2.793|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "d<17>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
d<17>                                          |        7.037|      SLOW  |
2.850|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "d<16>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
d<16>                                          |        7.363|      SLOW  |
2.973|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "d<15>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
d<15>                                          |        7.277|      SLOW  |
2.979|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "d<14>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
d<14>                                          |        7.456|      SLOW  |
2.956|      FAST  |         0.000|
```

```
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<13>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<13>                                          |        7.365|      SLOW  |
2.959|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<12>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<12>                                          |        7.346|      SLOW  |
2.961|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<11>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<11>                                          |        7.440|      SLOW  |
2.980|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+

COMP "d<10>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+--------------+
d<10>                                          |        7.086|      SLOW  |
2.967|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
```

```
---------+--------------+

COMP "d<9>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
d<9>                                            |        7.323|     SLOW  |
2.958|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "d<8>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
d<8>                                            |        7.229|     SLOW  |
2.964|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "d<7>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
d<7>                                            |        7.136|     SLOW  |
2.928|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "d<6>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
d<6>                                            |        7.137|     SLOW  |
2.968|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
```

COMP "d<5>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<5>	8.010	SLOW	3.402	FAST	0.000

COMP "d<4>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<4>	8.031	SLOW	3.245	FAST	0.000

COMP "d<3>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<3>	7.175	SLOW	3.124	FAST	0.000

COMP "d<2>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<2>	7.081	SLOW	2.984	FAST	0.000

COMP "d<1>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<1>	7.067	SLOW	3.017	FAST	0.000

COMP "d<0>" OFFSET = OUT 4 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
d<0>	7.202	SLOW	3.037	FAST	0.000

COMP "address<31>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
address<31>	5.590	SLOW	2.789	FAST	0.000

COMP "address<30>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;

PAD	Max (slowest) Delay (ns)	Process Corner	Min (fastest) Delay (ns)	Process Corner	Edge Skew (ns)
address<30>	5.610	SLOW	2.806	FAST	0.000

COMP "address<29>" OFFSET = OUT 3 ns AFTER COMP "clk";

```
Bus Skew: 0.000 ns;
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<29>                                     |        5.607|      SLOW  |
2.801|      FAST  |         0.000|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<28>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<28>                                     |        5.600|      SLOW  |
2.799|      FAST  |         0.000|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<27>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<27>                                     |        5.540|      SLOW  |
2.762|      FAST  |         0.000|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<26>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<26>                                     |        5.610|      SLOW  |
2.806|      FAST  |         0.000|
------------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<25>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
```

```
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<25>                                     |        5.588|      SLOW |
2.787|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "address<24>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<24>                                     |        5.614|      SLOW |
2.813|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "address<23>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<23>                                     |        5.543|      SLOW |
2.765|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "address<22>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process  |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner  | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<22>                                     |        5.580|      SLOW |
2.797|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "address<21>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
```

```
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
address<21>                                     |        5.584|      SLOW  |
2.785|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+

COMP "address<20>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
address<20>                                     |        5.545|      SLOW  |
2.768|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+

COMP "address<19>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
address<19>                                     |        5.671|      SLOW  |
2.832|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+

COMP "address<18>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |             |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
address<18>                                     |        5.562|      SLOW  |
2.783|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+

COMP "address<17>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+-------------+
```

```
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<17>                                     |        5.634|      SLOW  |
2.825|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<16>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<16>                                     |        5.612|      SLOW  |
2.823|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<15>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<15>                                     |        5.575|      SLOW  |
2.777|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<14>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<14>                                     |        5.563|      SLOW  |
2.786|      FAST  |         0.000|
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<13>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
```

```
Process   |              |
PAD                                              | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<13>                                      |        5.546|      SLOW  |
2.765|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<12>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                 |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                              | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<12>                                      |        5.544|      SLOW  |
2.767|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<11>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                 |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                              | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<11>                                      |        5.626|      SLOW  |
2.816|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<10>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                 |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                              | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<10>                                      |        5.590|      SLOW  |
2.788|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<9>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                 |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
```

```
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<9>                                        |        5.622|      SLOW  |
2.812|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<8>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<8>                                        |        5.586|      SLOW  |
2.785|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<7>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<7>                                        |        5.580|      SLOW  |
2.785|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<6>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
address<6>                                        |        5.605|      SLOW  |
2.807|      FAST  |         0.000|
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+

COMP "address<5>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-------------------------------------------------+-------------+------------+-------------+---
---------+--------------+
                                                  |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                               | Delay (ns)  |   Corner   | Delay (ns)
```

```
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<5>                                     |        5.587|      SLOW  |
2.792|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<4>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<4>                                     |        5.612|      SLOW  |
2.814|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<3>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<3>                                     |        5.592|      SLOW  |
2.790|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<2>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
address<2>                                     |        5.544|      SLOW  |
2.766|      FAST  |         0.000|
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+

COMP "address<1>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
-----------------------------------------------+------------+-----------+------------+---
---------+-------------+
                                               |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                            | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
```

```
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<1>                                      |        5.606|      SLOW  |
2.818|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "address<0>" OFFSET = OUT 3 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
address<0>                                      |        5.648|      SLOW  |
2.840|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "read" OFFSET = OUT 2 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
read                                            |        7.211|      SLOW  |
3.491|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+

COMP "write" OFFSET = OUT 2 ns AFTER COMP "clk";
Bus Skew: 0.000 ns;
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|
Process   |              |
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)
|   Corner   |Edge Skew (ns)|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+
write                                           |        7.228|      SLOW  |
3.364|      FAST  |         0.000|
------------------------------------------------+-------------+-----------+-------------+---
---------+--------------+


Timing summary:
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Timing errors: 511  Score: 364561  (Setup/Max: 364561, Hold: 0)

Constraints cover 6601943 paths, 0 nets, and 7195 connections

Design statistics:
```

```
   Minimum period:   7.211ns{1}   (Maximum frequency: 138.677MHz)
   Minimum input required time before clock:   1.929ns
   Minimum output required time after clock:   8.031ns


------------------------------------Footnotes-----------------------------------
1)  The minimum period statistic assumes all single cycle delays.

Analysis completed Tue Sep 23 09:55:07 2014
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Trace Settings:
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Trace Settings

Peak Memory Usage: 455 MB
```