CSE 260M Lab 3: State machine coding and simulation

Work in pairs for this assignment

Lab Objectives

- Learn how to code and simulate state machines

Part I: Garage door opener simulation

In class, we discussed the design of a garage door state machine and presented the code for that state machine. Your task for part I of the lab is to create a test bench and simulate that state machine. The code that was presented in class was not fully simulated so it is possible that there are bugs in the code. If you find bugs in the course of your simulations, you must find and fix them.

You are required to create three different simulations that simulate the following state transitions:

Simulation 1) ResetState → opened → closing → closed → opening → opened
Simulation 2) ResetState → closed → opening → pauseUp → closing → closed
Simulation 3) ResetState → pauseDown → opening → opened → closing → closed

For all of the demonstrations, you must show the simulation to the TA and they should verify that the state machine moves through the states and transitions correctly and has the correct output. An example is shown below.
**Part 2: Sequence output state machine design and simulation**

Design the code and test bench for the following problem given on exam 2. You are welcome to use your design or the design given in the solutions.

Write the VHDL that will output the following sequence: 000, 010, 111, 101. The output should change once per clock cycle. Once 101 is reached, the circuit should then start from 000 and repeat.

Write a test bench and simulate 3 full cycles of the sequence.

**Part 3: AB serial state machine design and simulation**

Design the code and test bench for the following problem on exam 2. Design a circuit that will input 2 serial streams of binary data (A and B) and output a 1 if and only if AB = “11” follow by “00”. Each two bits are distinct meaning there is no overlap in the pattern. The output should only be 1 on the comparison of the second bit. Use a Moore FSM. As an example:

A = 10 10 11 01 10 01 00 10 00
B = 00 10 10 01 10 11 00 10 00
Z = 00 01 00 00 01 00 00 01 00

Write a test bench that will input the example A and B serial streams above and result in the correct output shown in Z.

**Part 4: Pattern detector state machine simulation**

Design the code and test bench for a circuit that will input a serial sequence of bits and output a ‘1’ each time the sequence 010 is detected.

A = 00110101000101011010
Z = 00000010100010100001

**Lab 3 Demonstration Rubric**

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