

**Spring Semester 2020**

**CSE463M: Digital Integrated Circuit Design and Architecture**

**Homework #6**

1. **Design a Master-Slave positive-edge clock triggered D Flip Flop.**
2. **Draw the Master-Slave positive-edge clock triggered D Flip Flop schematic in Cadence and print it.**
3. **Create an entire circuit schematic symbol and simulate the transient behavior of**

**the circuit schematic with 100fF load on the output. Print the transient behavior.**

**Transient behavior should show the entire truth table of the Master-Slave**

**positive-edge clock triggered D Flip Flop.**

**c. Draw the layout of the circuit. Perform DRC and LVS on the layout. Print the**

**layout of the circuit, the DRC and the LVS messages.**

**d. Simulate the transient behavior of the circuit layout with 100fF load on the**

**output. Print the transient behavior. Transient behavior should show the entire**

**truth table of the Master-Slave positive-edge clock triggered D Flip Flop. Also the**

**transient behavior of the circuit schematic and the circuit layout should**

**reasonably match.**