

**Spring Semester 2020**

**CSE463M: Digital Integrated Circuit Design and Architecture**

**Homework #5**

1. **Consider the function Y = (AB + C)G + EF**
2. **Implement this function using CMOS logic and draw the circuit in Cadence. Assume that all signals and their respective inverse signals are available to the designer. Print the schematic.**
3. **All transistors in the circuit have W/L = 1.8m/1.8m, VT0n =0.8V, VT0p =-0.9V, k'T0n =110 μA/V2, k'T0p =38 μA /V2. What is the value of the logic threshold when all inputs are connected to VTH?**

**Show all hand calculations and simulate the results in Spice. Print the Spice simulation.**

1. **Simulate the circuit for all possible input transitions and plot the results.**
2. **What is the common Euler path for the pMOS and nMOS network of transistors? Draw the optimized stick-diagram layout.**
3. **Draw the optimized layout in Cadence. Perform DRC and LVS on the layout. Print the layout of the circuit, the DRC and the LVS messages.**
4. **Simulate the circuit layout for all possible input transitions and plot the results and make sure that circuit schematic simulation and layout simulation have matching results.**
5. **Design a 2 to 1 Multiplexer using CMOS Transmission Gates in Cadence.**

**a. Draw the schematic in Cadence and print it.**

**b. Simulate the transient behavior of the circuit for all possible combinations. Print the transient**

**behavior.**

**c. Draw the layout of the circuit. Perform DRC and LVS on the layout. Print the layout of the circuit,**

**the DRC and the LVS messages.**

**d. Simulate the transient behavior of the circuit layout for all possible combinations. Print the**

**transient behavior. Make sure that circuit schematic simulation and layout simulation have**

**matching results.**