

**Spring Semester 2020**

**CSE463M: Digital Integrated Circuit Design and Architecture**

**Homework #4**

1. **2-input CMOS NOR gate design problem (including layout)**

**Design a two input CMOS NOR gate with the following specifications:**

* **logic threshold of VTH = 2.5V when all inputs are connected to VTH**
* **minimum rise time of rise < 2ns for load capacitance of 100fF.**

**Present the following for your homework:**

**a) Show all hand calculations used to get the appropriate size of all transistors.**

**b) Draw the schematic of the two input NOR gate and create a symbol.**

**c) Simulate the NOR gate. Plot the DC characteristics when all inputs are connected together.**

**Plot the transient characteristics for all transitions of the inputs and verify that the**

**specifications were met.**

**d) Draw the layout of the NOR gate. Measure the size of the layout and use the ruler in layout**

**to show the dimensions.**

**e) Run a DRC, extract the layout and LVS the design. Cut and Paste the messages generated in**

**the CIW (the main Cadence window) when the DRC is executed. Print the LVS result – make**

**sure it has successfully passed LVS.**

1. **2-input CMOS NAND gate design problem (including layout)**

**Design a two input CMOS NAND gate with the following specifications:**

* **logic threshold of VTH = 2.5V when all inputs are connected to VTH**
* **minimum fall time of fall < 2ns for load capacitance of 100fF.**

**Repeat the same steps as in Problem 1 and print all results as requested in Problem 1.**