

**Spring Semester 2020**

**CSE463M: Digital Integrated Circuit Design and Architecture**

**Homework #2**

**1) Solve problem 5.1 (inverter design with nMOS and resistor) from Chapter 5 from the textbook. Please show all your work and be neat and circle your answers.**

**2) Solve problem 5.6 (inverter design with nMOS and pMOS) from Chapter 5 from the textbook. Please show all your work and be neat and circle your answers.**

**3) Design suitable circuits in Cadence that will allow you to compute the voltage threshold (Vt), k’ and substrate bias coefficient (γ) for an NMOS transistor. The transistor aspect ratios are W=9um and L=9um. Print the circuits that you design to extract these 3 parameters. Simulate the circuit and print the simulated results. Indicate on your plots how you computed the 3 parameters.**

**4) Repeat the same exercise for a PMOS device. Print all simulations and circuits that you use in order to determine voltage threshold (Vt), k’ and substrate bias coefficient (γ) for the PMOS transistor.**

**5) Inverter design problem (schematic only)**

**Draw a schematic of a CMOS inverter. The power supply of the circuit is 5V, i.e. the source of the PMOS transistor is connected to 5V. Choose minimum size for both length and width of PMOS and NMOS transistors. Save the circuit and print it out. Perform a DC analysis on the circuit by sweeping the input to the inverter from 0V to 5V. Plot the output of the inverter. Label the threshold of the inverter on the plot.**

**6) Inverter design problem (including layout)**

**Follow the wiki tutorial in order to solve the problems bellow and get familiar with Cadence:**

[**https://eda.engineering.wustl.edu/wiki/index.php/Cadence**](https://eda.engineering.wustl.edu/wiki/index.php/Cadence)

**Here is transistor data for AMI Semiconductor 0.5 micron process:**

****

**Problem set:**

**6.1) Design a CMOS inverter that will operate from a 5V power supply (i.e. Vdd=5V) and it has a threshold (Vth) of 3V. Show all hand calculations that allowed you to design this circuit. Use the data in the table above for your calculations.**

**6.2) Design the CMOS inverter from problem 6.1) in Cadence. Print the schematic of the inverter. Simulate the static behavior of the inverter. Make sure that your SPICE simulation indicates that the threshold of the inverter is 3V. If this is not the case, readjust the aspect ratios of your NMOS and/or PMOS in order to have the desired threshold of 3V. Print your SPICE simulation and indicate your Vth on the plot.**

**6.3) Using SPICE and the calculator within the SPICE simulator to compute VIL and VIH. Plot the results and indicate your results on the plot.**

**6.4) Draw the layout of the inverter in Cadence. Print the layout of the device.**

**6.5) Run a Design Rule Check (DRC), extract the layout and LVS the design. Cut and Paste the messages generated in the CIW (the main Cadence window) when the DRC is executed. Print the Layout vs Schematic (LVS) result – make sure it has successfully passed LVS.**