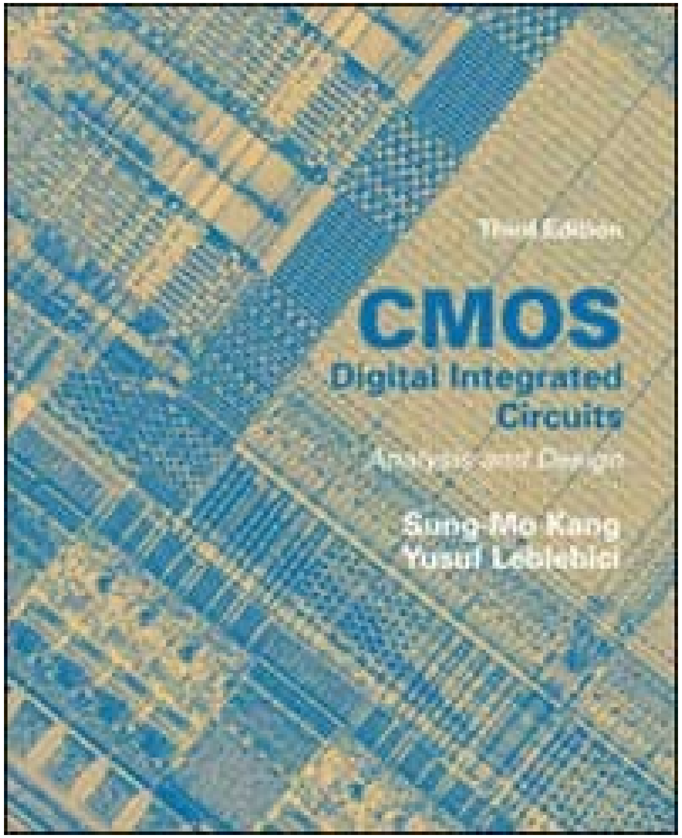
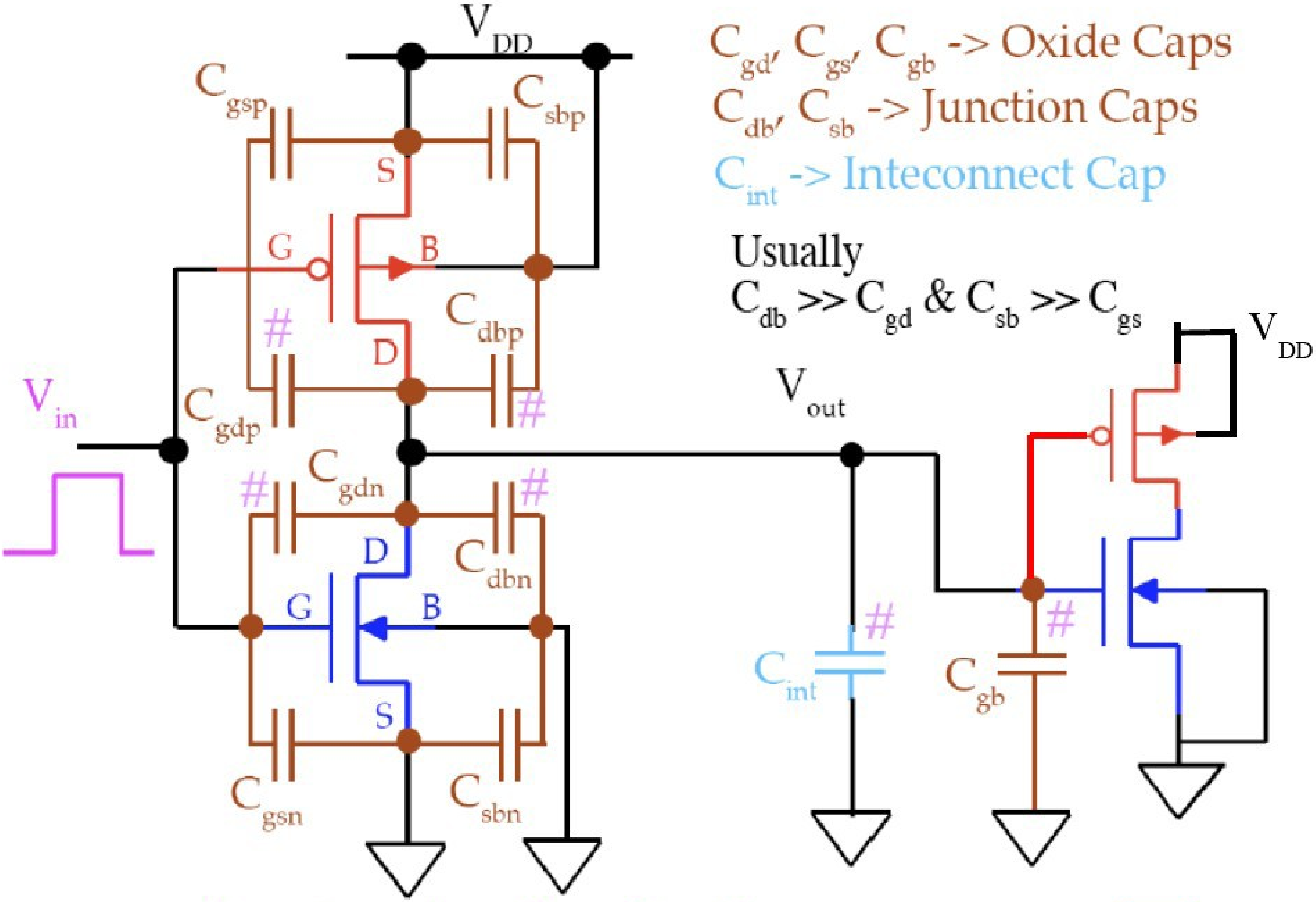
Digital IC Design and Architecture



MOS Inverter Dynamic Behavior



C_{gd}, C_{gs}, C_{gb} -> Oxide Caps

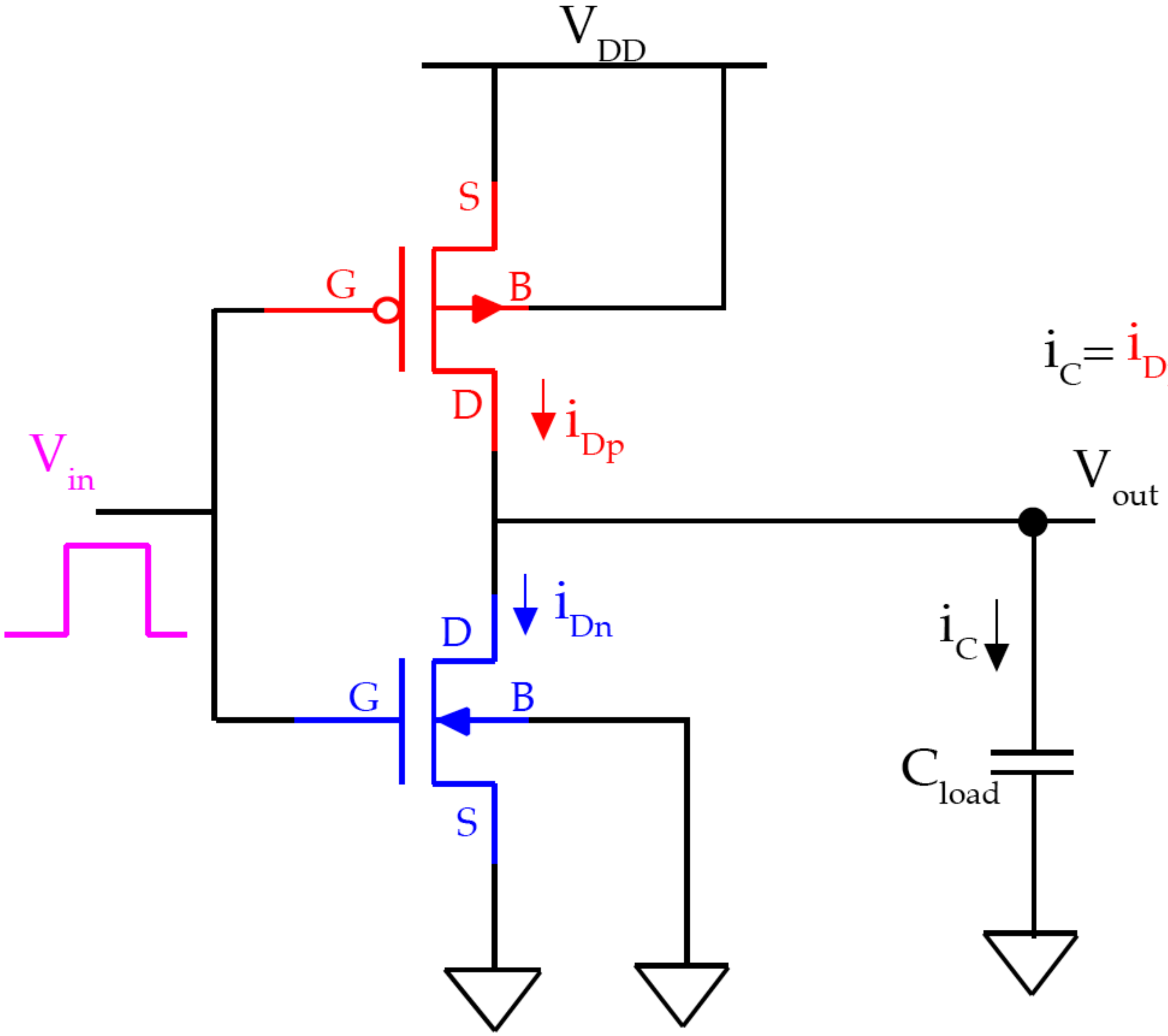
C_{db}, C_{sb} -> Junction Caps

C_{int} -> Inteconnect Cap

Usually
$C_{db} >> C_{gd}$ & $C_{sb} >> C_{gs}$

$$C_{load} = C_{dbn}^{\#} + C_{dbp}^{\#} + C_{gdn}^{\#} + C_{gdp}^{\#} + C_{int}^{\#} + C_{gb}^{\#} \approx C_{dbn} + C_{dbp} + C_{int} + \boxed{C_{gb}}$$

where $\boxed{C_{gb} = C_{gbn} + C_{gbp}}$

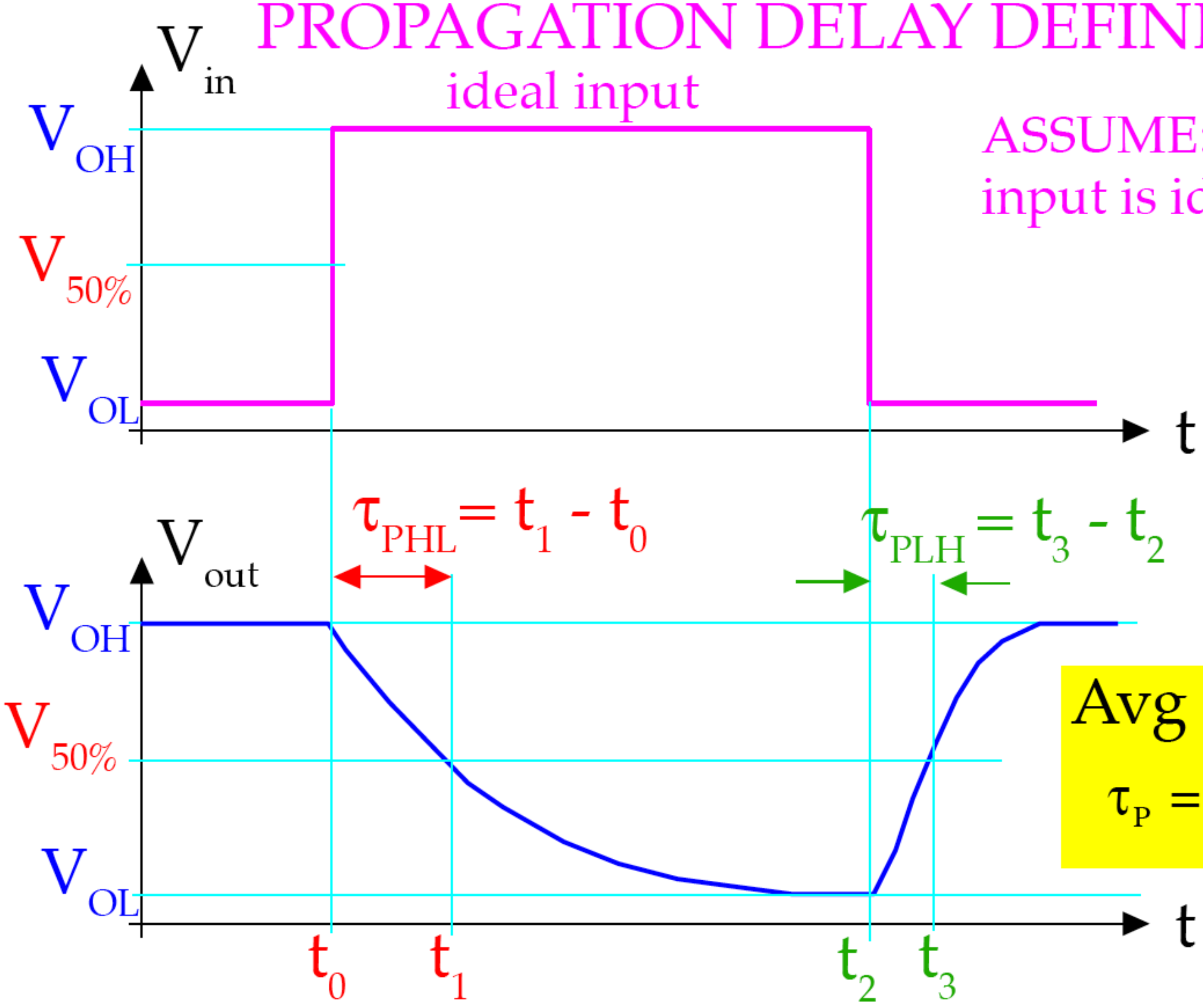


$$i_C = i_{Dp} - i_{Dn}$$

$$C_{load} = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_{gb}$$

PROPAGATION DELAY DEFINITIONS

ASSUME: Initially the input is ideal.



$\tau_{PHL} = t_1 - t_0$

$\tau_{PLH} = t_3 - t_2$

Avg Prop Delay

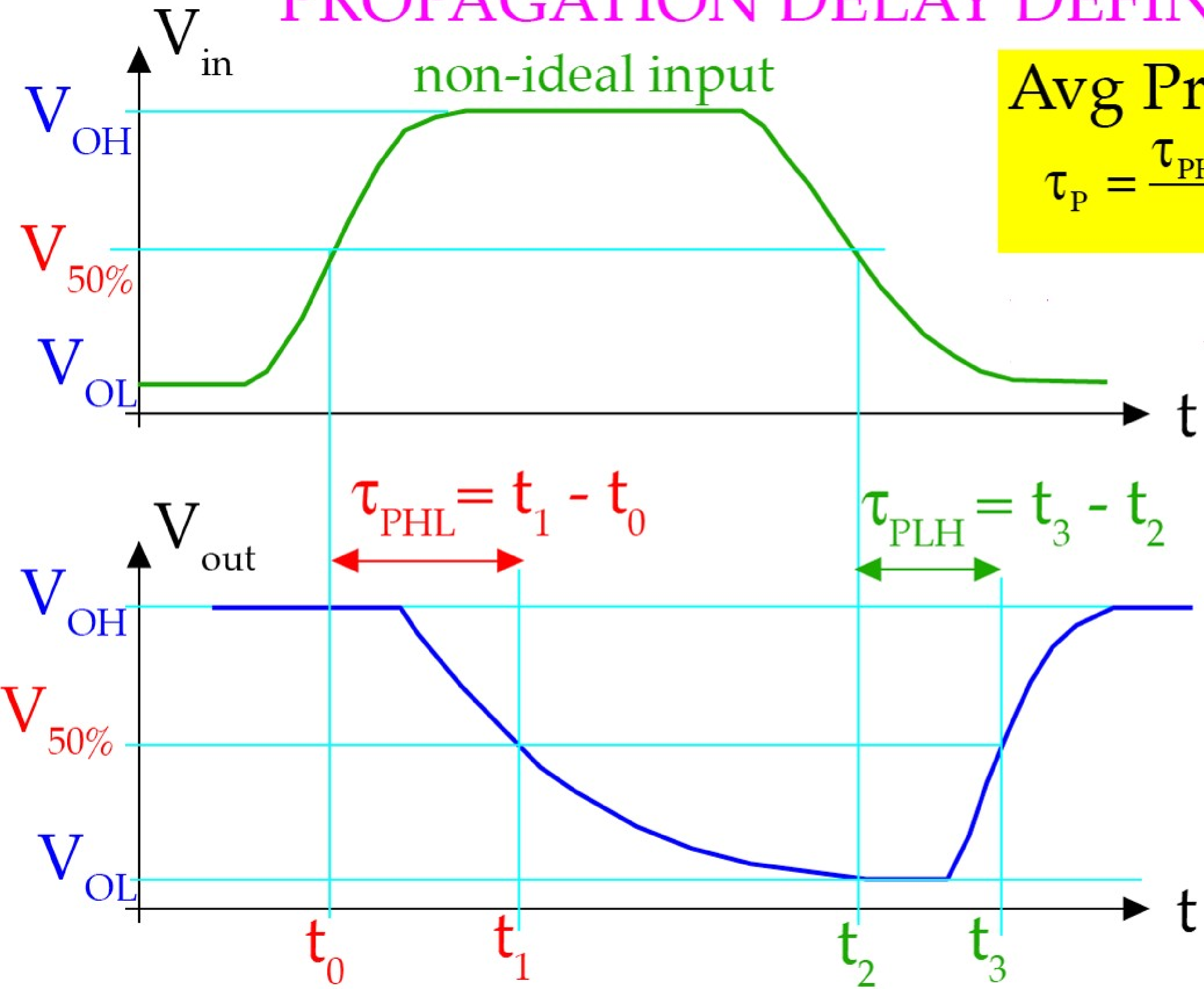
$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

$$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$$

PROPAGATION DELAY DEFINITIONS

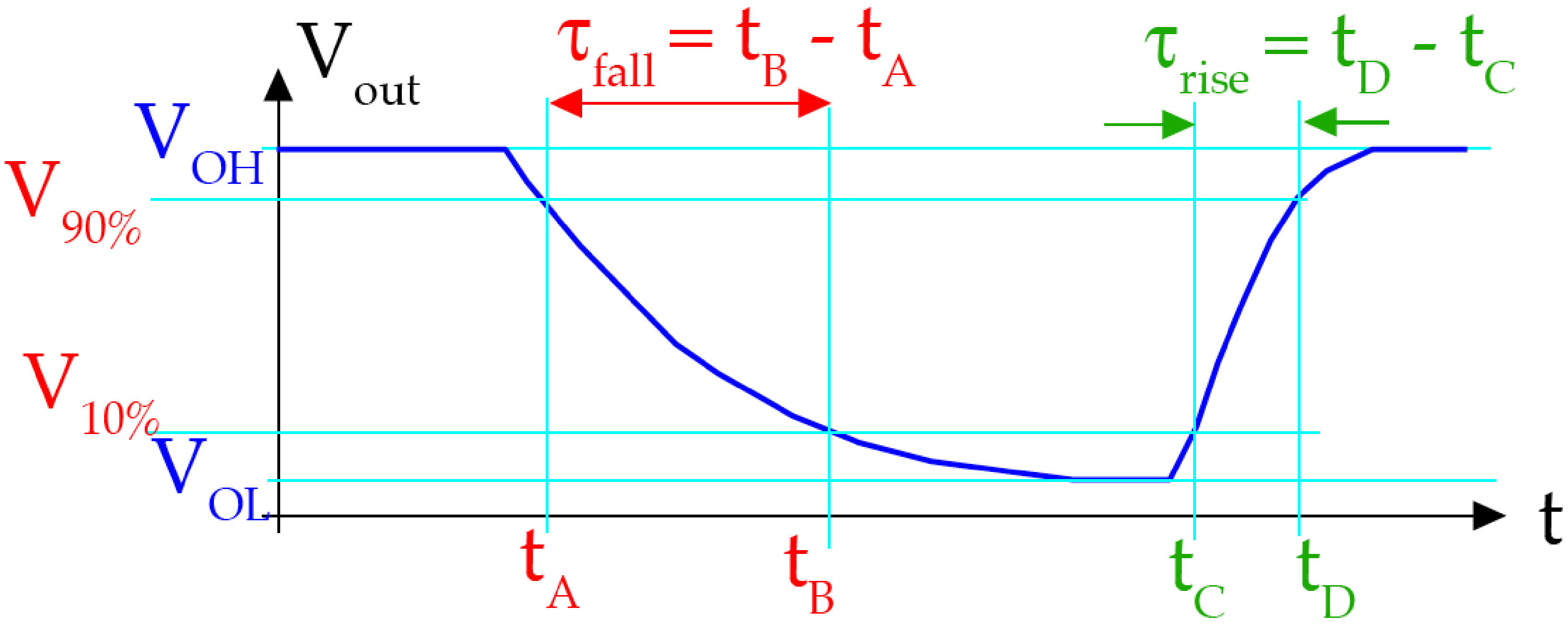
Avg Prop Delay

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$



$$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$$

OUTPUT VOLTAGE RISE & FALL TIMES



$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$

$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

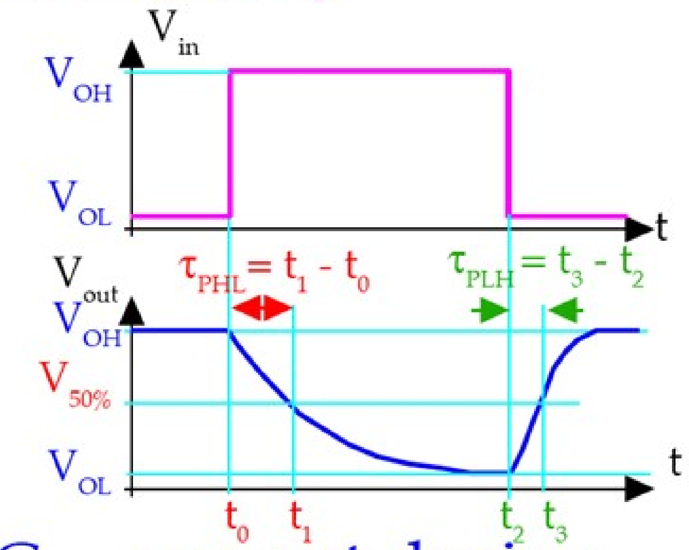
$$\boxed{I = C\frac{\Delta V}{\Delta t}}$$

CALCULATION OF DELAY TIMES

QUICK ESTIMATES:

$$\tau_{PHL} = \frac{C_{load}\,\Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load}\left(V_{OH} - V_{50\%}\right)}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load}\,\Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load}\left(V_{50\%} - V_{OL}\right)}{I_{avg,LH}}$$



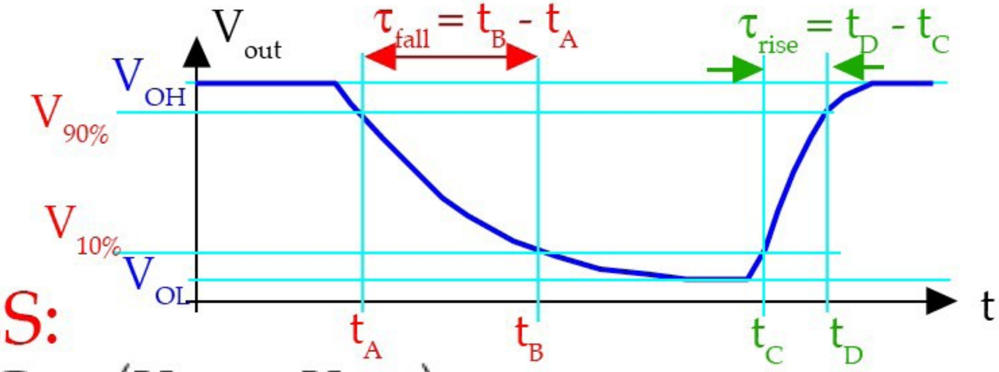
$I_{avg,HL}$ -> approximate average C_{load} current during high-to-low V_{out} transition

$$I_{avg,HL} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{OH}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{50\%}\right)\right]$$

$I_{avg,LH}$ -> approximate average C_{load} current during low-to-high V_{out} transition

$$I_{avg,LH} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{OL}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{50\%}\right)\right]$$

$$i_C = i_{Dp} - i_{Dn}$$



QUICK ESTIMATES:

$$\tau_{fall} = \frac{C_{load}\Delta V_{90-to-10\%}}{I_{avg,90-to-10\%}} = \frac{C_{load}\left(V_{90\%} - V_{10\%}\right)}{I_{avg,90-to-10\%}}$$

$$\tau_{rise} = \frac{C_{load}\Delta V_{10-to-90\%}}{I_{avg,10-to-90\%}} = \frac{C_{load}\left(V_{90\%} - V_{10\%}\right)}{I_{avg,10-to-90\%}}$$

$I_{avg,90\text{-}to\text{-}10\%}$ -> approximate average C_{load} current during 90%-to-10% V_{out} transition

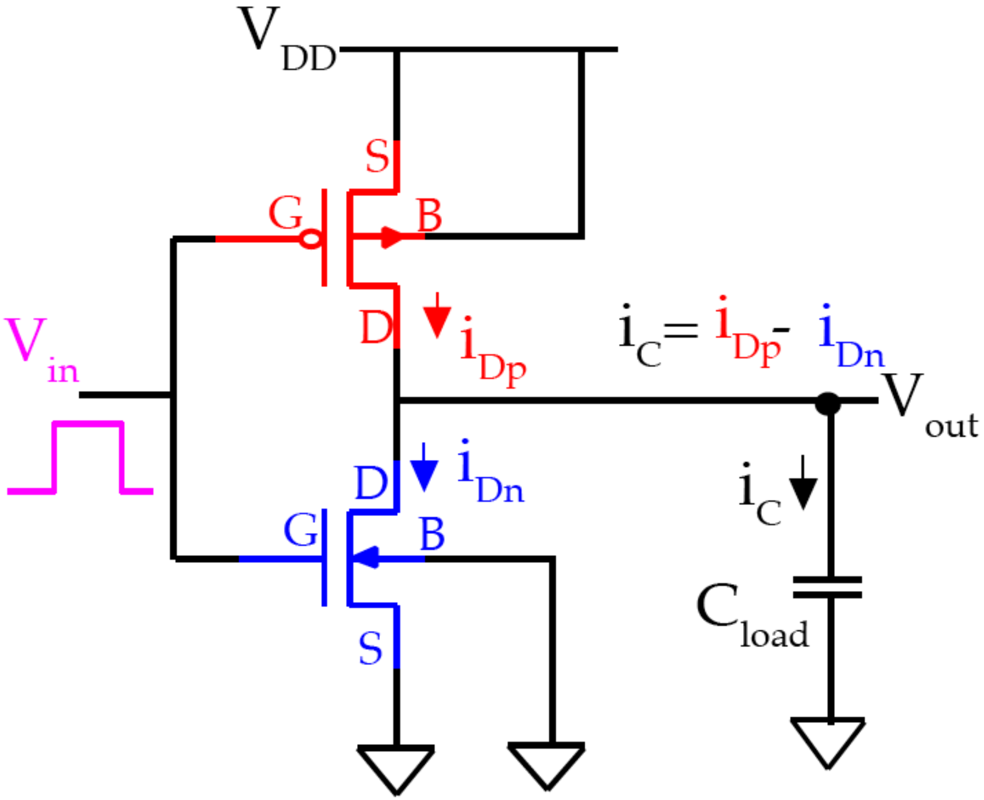
$$I_{avg,90-to-10\%} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{90\%}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{10\%}\right)\right]$$

$I_{avg,10\text{-}to90\%}$ -> approximate average C_{load} current during 10%-to-90% V_{out} transition

$$I_{avg,10-to-90\%} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{10\%}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{90\%}\right)\right]$$

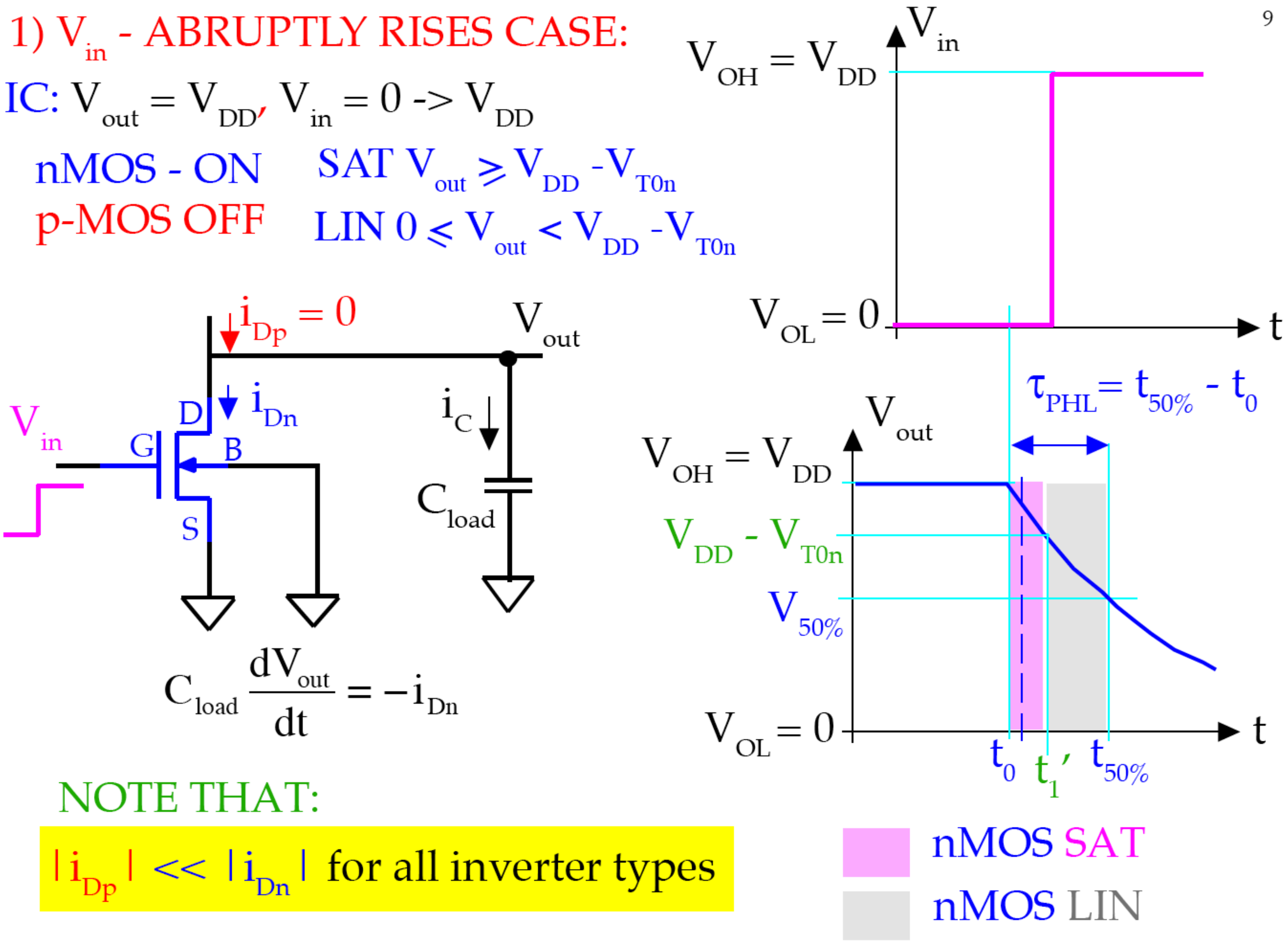
Calculating Propagation Delays By Solving the Circuit Differential Equation

MORE ACCURATE CALCULATION OF τ_{PHL}, τ_{PLH}:



$$i_C = C_{load}\frac{dV_{out}}{dt} = i_{Dp} - i_{Dn}$$

1) Vin – ABRUPTLY RISES CASE -> T*PHL*



1) V_{in} - ABRUPTLY RISES CASE:

IC: $V_{out} = V_{DD}$, $V_{in} = 0 \rightarrow V_{DD}$

nMOS - ON   SAT $V_{out} \geq V_{DD} - V_{T0n}$

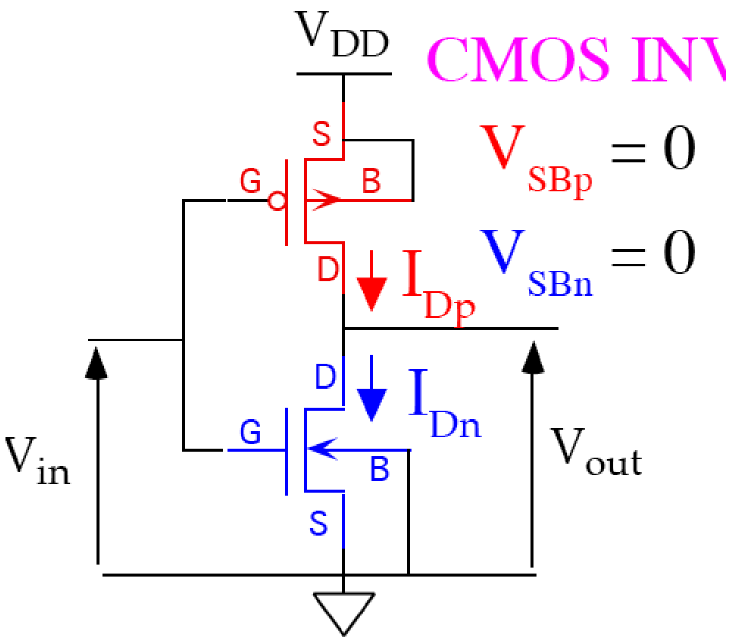
p-MOS OFF   LIN $0 \leq V_{out} < V_{DD} - V_{T0n}$

$$C_{load}\frac{dV_{out}}{dt} = -i_{Dn}$$

NOTE THAT:

$|i_{Dp}| << |i_{Dn}|$ for all inverter types

CMOS Inverter Revisited

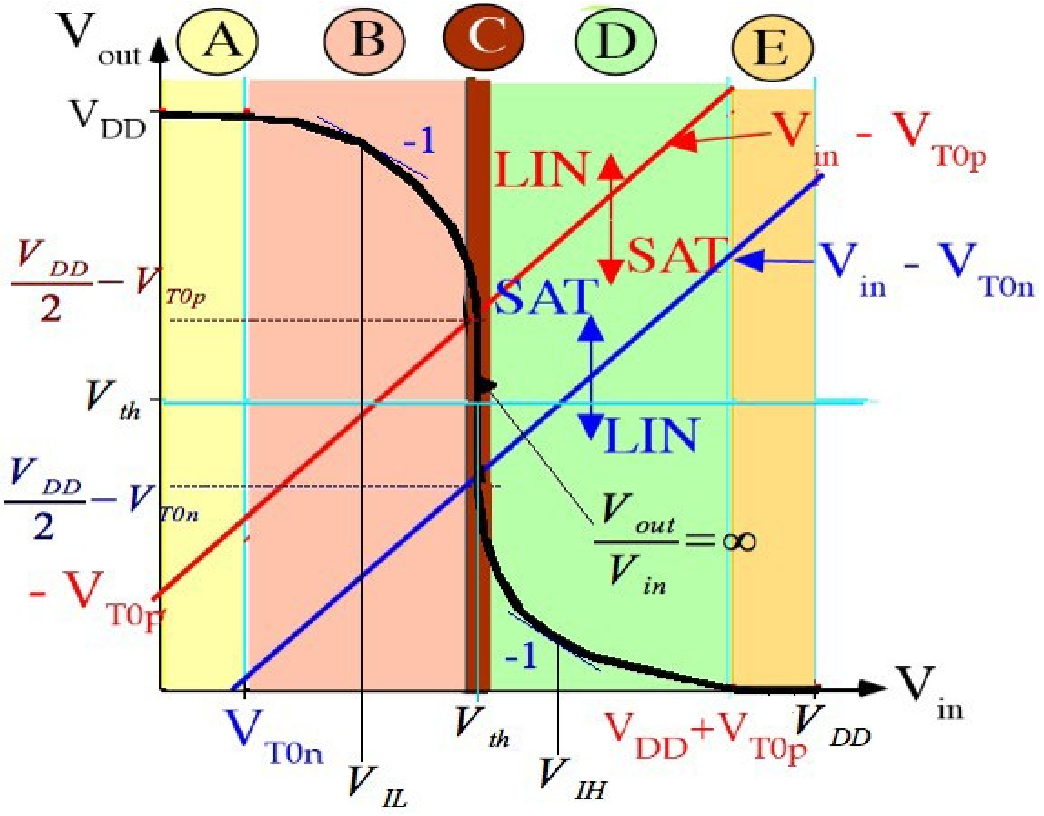


$$V_{SBp} = 0$$

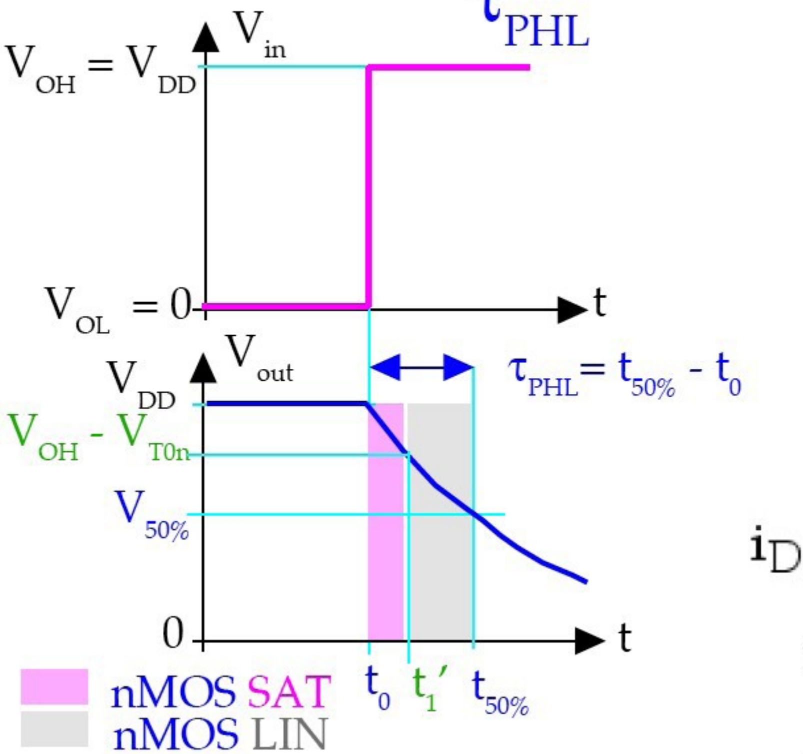
$$V_{SBn} = 0$$

$$V_{in} = V_{GSn} = V_{GSp} + V_{DD}$$

$$V_{out} = V_{DSn} = V_{DSp} + V_{DD}$$



τ_{PHL}



$t_0 < t < t_1'$:

$$i_{Dn} = \frac{k_n}{2}(V_{in} - V_{T0n})^2 = -i_C$$

$$\frac{k_n}{2}(V_{OH} - V_{T0n})^2 = -C_{load}\frac{dV_{out}}{dt}$$

for $V_{OH} - V_{T0n} < V_{out} \le V_{OH}$

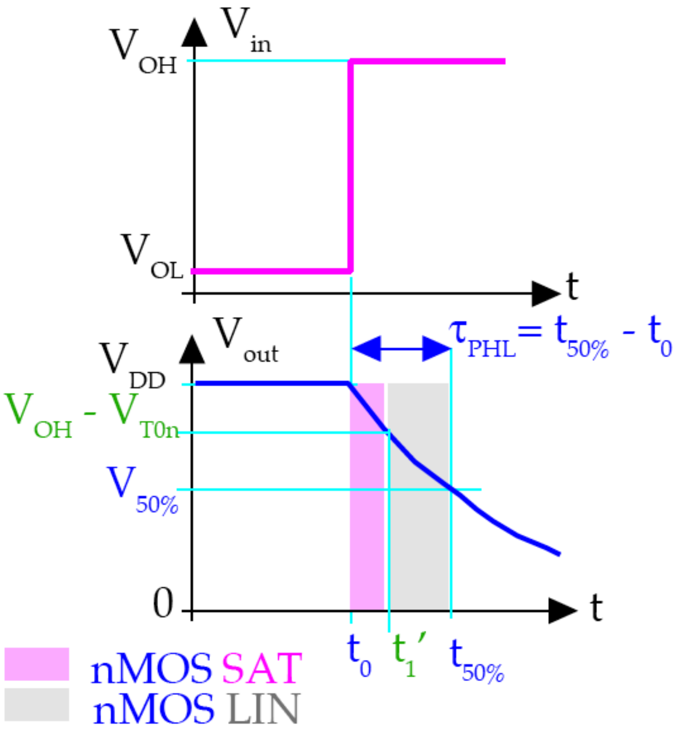
$$i_{Dn} = -C_{load}\frac{dV_{out}}{dt} \Rightarrow \boxed{dt = -\frac{C_{load}}{i_{Dn}}dV_{out}}$$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

Since i_{Dn} is INDEP of V_{out}

$$\int_{t=t_0}^{t=t_1'} dt = -\frac{C_{load}}{\frac{k_n}{2}(V_{OH} - V_{T0n})^2}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} dV_{out}$$

$$\boxed{t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH} - V_{T0n})^2}}$$



$t_1' < t < t_{50\%}$:

$$i_{Dn} = \frac{k_n}{2}\left[2(V_{in} - V_{T0n})V_{out} - V_{out}^2\right]$$

$$= \frac{k_n}{2}\left[2(V_{OH} - V_{T0n})V_{out} - V_{out}^2\right] = -C_{load}\frac{dV_{out}}{dt}$$

for $V_{out} \le V_{OH} - V_{T0n}$

$$\int_{t=t_1'}^{t=t_{50\%}} dt = -C_{load}\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

$$\int_{t=t_1'}^{t=t_{50\%}} dt = -\frac{2C_{load}}{k_n}\boxed{\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}} \left(\frac{1}{2(V_{OH}-V_{T0n})V_{out}-V_{out}^2}\right) dV_{out}}$$

$$\updownarrow$$

$$t_{50\%} - t_1' = -\frac{2C_{load}}{k_n}\boxed{\frac{1}{2(V_{OH}-V_{T0n})}\ln\left(\frac{V_{out}}{2(V_{OH}-V_{T0n})-V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}}$$

$$t_{50\%} - t_1' = -\frac{2\,C_{load}}{k_n}\,\frac{1}{2(V_{OH}-V_{T0n})}\ln\left(\frac{V_{out}}{2(V_{OH}-V_{T0n})-V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}$$

$$\boxed{= \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\ln\left(\frac{2(V_{OH}-V_{T0n})-V_{50\%}}{V_{50\%}}\right)}$$

$$\longrightarrow \quad t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH}-V_{T0n})^2}$$

$$\tau_{PHL} = t_{50\%} - t_1' + t_1' - t_0$$

$$\tau_{PHL} = \frac{2\,C_{load}V_{T0n}}{k_n(V_{OH}-V_{T0n})^2} + \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\ln\left(\frac{2(V_{OH}-V_{T0n})-V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\left[\frac{2\,V_{T0n}}{V_{OH}-V_{T0n}} + \ln\left(\frac{2(V_{OH}-V_{T0n})}{V_{50\%}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n (V_{OH} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{2(V_{OH} - V_{T0n})}{V_{50\%}} - 1 \right) \right]$$

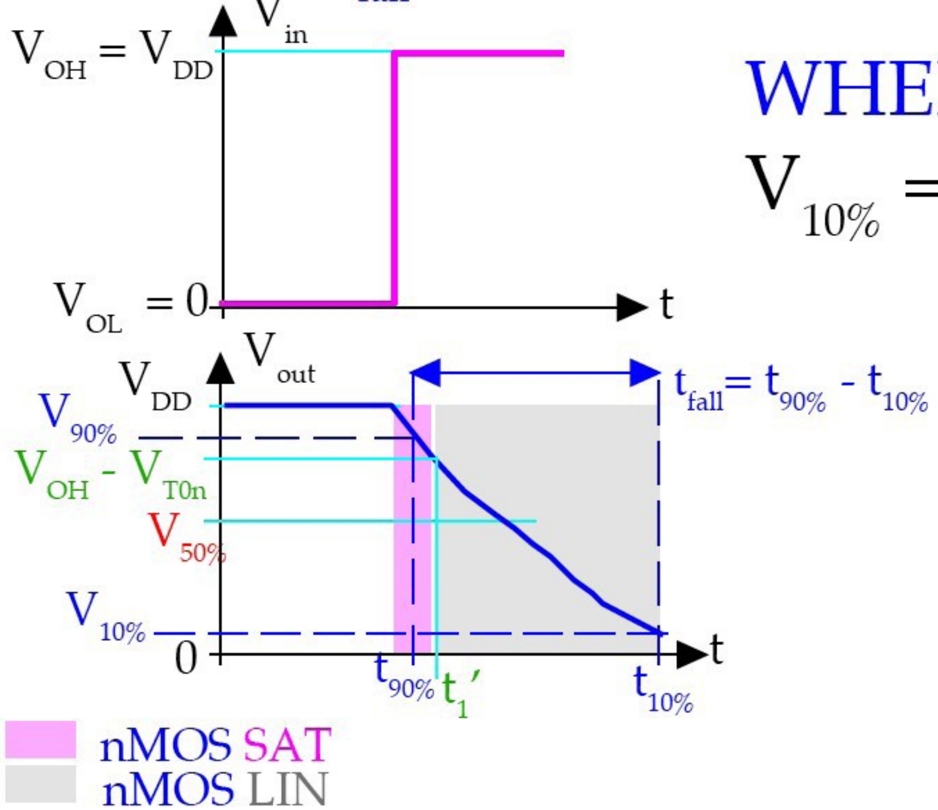
SUBSTITUTING $V_{50\%} = 0.5\,[V_{OL} + V_{OH}]$

$$\tau_{PHL} = \frac{C_{load}}{k_n (V_{OH} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

WHERE for CMOS Inverters $V_{OL} = 0,\ V_{OH} = V_{DD}$

$$\tau_{PHL} = \frac{C_{load}}{k_n (V_{DD} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1 \right) \right]$$

Fall Time: τ_{fall}



WHERE for CMOS Inverters

$V_{10\%} = 0.1V_{DD}$, $V_{90\%} = 0.9V_{DD}$

$$\boxed{\tau_{fall} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T0n}\right)}\left[\frac{2\left(V_{T0n} - 0.1V_{DD}\right)}{V_{DD} - V_{T0n}} + \ln\left(\frac{2\left(V_{DD} - V_{T0n}\right)}{0.1V_{DD}} - 1\right)\right]}$$

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T0n}\right)}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{2\left(V_{DD} - V_{T0n}\right)}{0.5V_{DD}} - 1\right)\right]$$

EXAMPLE 6.1

Consider a CMOS inverter with $C_{load} = 1.0$ pF, where the IV characteristics of the nMOS transitor driver are specified as follows:

$$V_{GSn} = 5 \text{ V and } V_{DSn} \geqslant 4\text{V} \quad \Rightarrow i_{Dn} = i_{Dnsat} = 5 \text{ mA}$$

Assume V_{in} is a step pulse that switches instantaneously from 0 to 5 V. Calculate the delay time necessary for the inverter output to fall from its initial value of 5 V to 2.5 V.

$$V_{50\%} = 0.5\,[V_{OL} + V_{OH}] = 0.5\,[0 + 5 \text{ V}] = 2.5 \text{ V}$$

1. FROM IV DATA: Determine V_{T0n} and k_n

nMOS in SAT => $V_{DSn} = 5\text{V} - V_{T0n} = 4$ V => $V_{T0n} = 1$ V

Using $$i_{Dnsat} = \frac{k_n}{2}(V_{GS} - V_{T0n})^2 = 5 \text{ mA}$$

$$k_n = \frac{2 i_{Dnsat}}{(V_{GS} - V_{T0n})^2} = \frac{2 \times 5\,\text{mA}}{(4\text{ V})^2} = 0.625 \times 10^{-3}\,\text{A}/\text{V}^2$$

2. $t_0 < t < t_1'$:

where $i_{Dn} = I_{Dnsat} = 5mA$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

$V_{OH} - V_{T0n} = 4\ V$

$V_{OH} = 5\ V$

$$t_1' - t_0 = -\frac{C_{load}}{i_{Dnsat}} \int_{V_{out}=5V}^{V_{out}=4V} dV_{out} = -\frac{1pF}{5mA}(-1V) = 0.2nS$$

UNITS $\frac{C_{Load}}{i_{Dnsat}} \Delta V = \frac{F}{A} V = \frac{C/V}{C/s} V = s$

3. $t_1' < t < t_1$:

$$t_1 - t_1' = \frac{C_{load}}{k_n (V_{OH} - V_{T0n})} \ln\left(\frac{2(V_{OH} - V_{T0n}) - V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{1pF}{(0.625x10^{-3}\ A/V^2)(5-1)V} \ln\left(\frac{2(5-1)V - 2.5V}{2.5V}\right)$$

$$= \frac{1x10^{-12}\ F}{(0.625x10^{-3}\ A/V^2)4V} \ln\left(\frac{5.5}{2.5}\right) = 1.26\ ns$$

$$\tau_{PHL} = 0.2\ ns + 1.26\ ns = 1.46\ ns$$

2) V_{in} - ABRUPTLY FALLS CASE:

IC: $V_{out} = V_{OL}$, $V_{in} = V_{OH}$ -> $V_{OL} = 0$

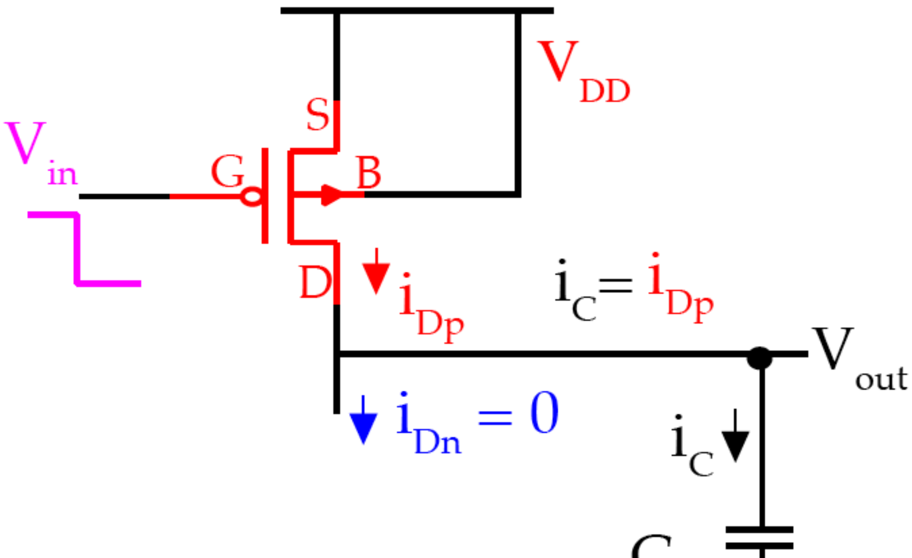
nMOS - OFF

p-MOS ON

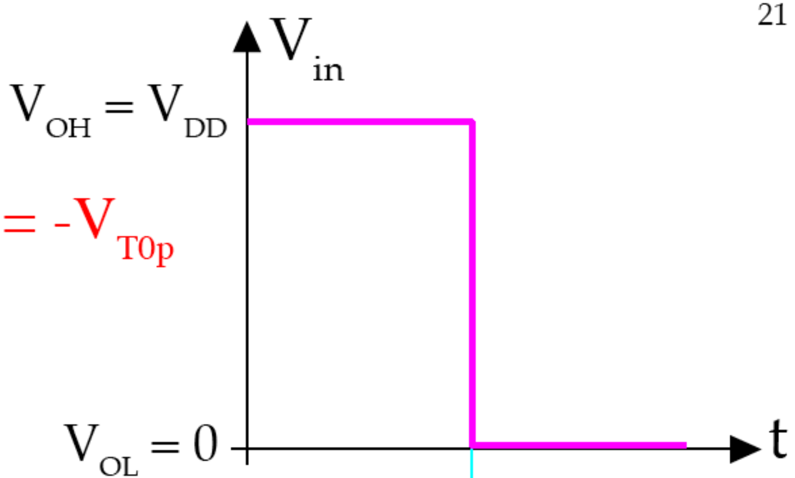
SAT $V_{out} \leq \cancelto{0}{V_{in}} - V_{T0p} = -V_{T0p}$

LIN $V_{out} > -V_{T0p}$

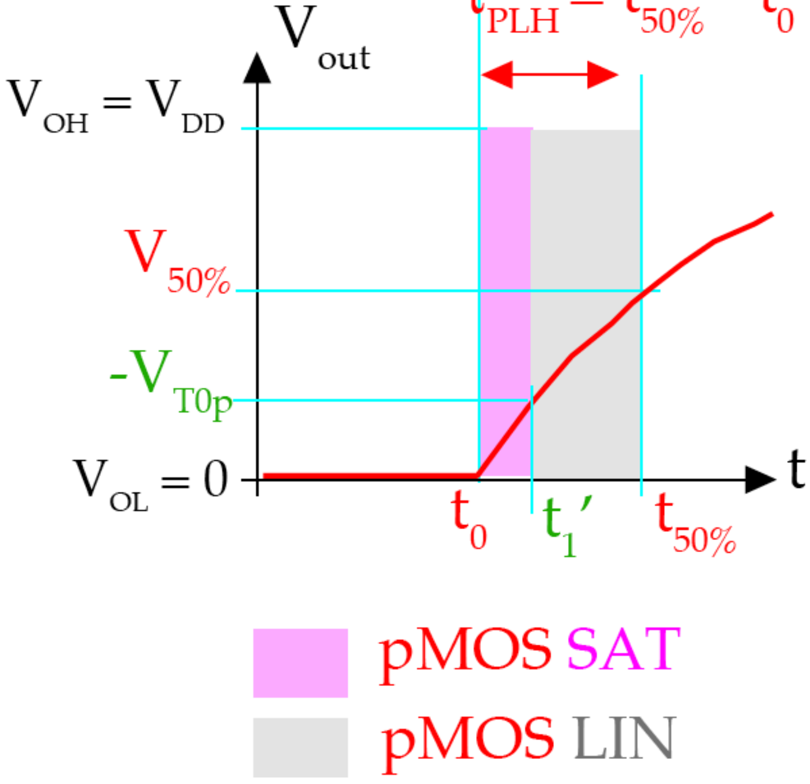
$V_{GS} = V_{in} - V_{DD}$ $V_{DS} = V_{out} - V_{DD}$



$$C_{load} \frac{dV_{out}}{dt} = i_{Dp}$$



$\tau_{PLH} = t_{50\%} - t_0$



$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{OH}-V_{OL}-|V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{OH}-|V_{T0p}|} + \ln\left(\frac{2(V_{OH}-V_{OL}-|V_{T0p}|)}{V_{OH}-V_{50\%}}-1\right)\right]$$

$V_{50\%} = 0.5\,[V_{OL}+V_{OH}]$, FOR CMOS INV: $V_{OL} = 0$, $V_{OH} = V_{DD}$

$$\boxed{\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD}-|V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{4(V_{DD}-|V_{T0p}|)}{V_{DD}}-1\right)\right]}$$

$$\boxed{\tau_{rise} = \frac{C_{load}}{k_p\left(V_{DD}-|V_{T0p}|\right)}\left[\frac{2\left(|V_{T0p}|-0.1V_{DD}\right)}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{2\left(V_{DD}-|V_{T0p}|\right)}{0.1V_{DD}}-1\right)\right]}$$

FOR CMOS INV: $V_{OL} = 0$, $V_{OH} = V_{DD}$

$$\boxed{\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD}-V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD}-V_{T0n}} + \ln\left(\frac{4(V_{DD}-V_{T0n})}{V_{DD}}-1\right)\right]}$$

CONDITIONS FOR Balanced CMOS Inverter Propagation Delays, i.e. $\tau_{PHL} = \tau_{PLH}$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0\,p}|)}\left[\frac{2|V_{T0\,p}|}{V_{DD} - |V_{T0\,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0\,p}|)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0\,n})}\left[\frac{2V_{T0\,n}}{V_{DD} - V_{T0\,n}} + \ln\left(\frac{4(V_{DD} - V_{T0\,n})}{V_{DD}} - 1\right)\right]$$

where $k_n = \mu_n C_{ox} \frac{W_n}{L_n}$ & $k_p = \mu_p C_{ox} \frac{W_p}{L_p}$

FOR $\tau_{PHL} = \tau_{PLH}$

$V_{T0n} = |V_{T0p}|$

$k_n = k_p$ or $\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n}$

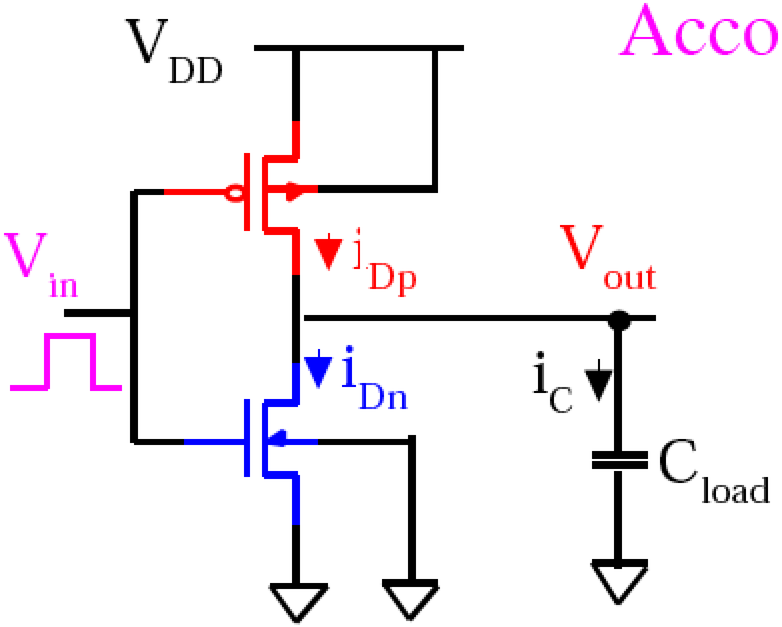
OBSERVATIONS

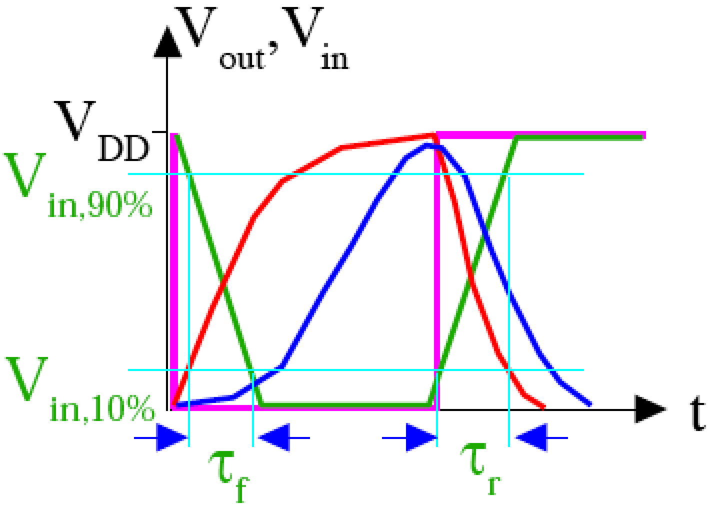
$$\tau_{PHL} = \frac{C_{load} L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

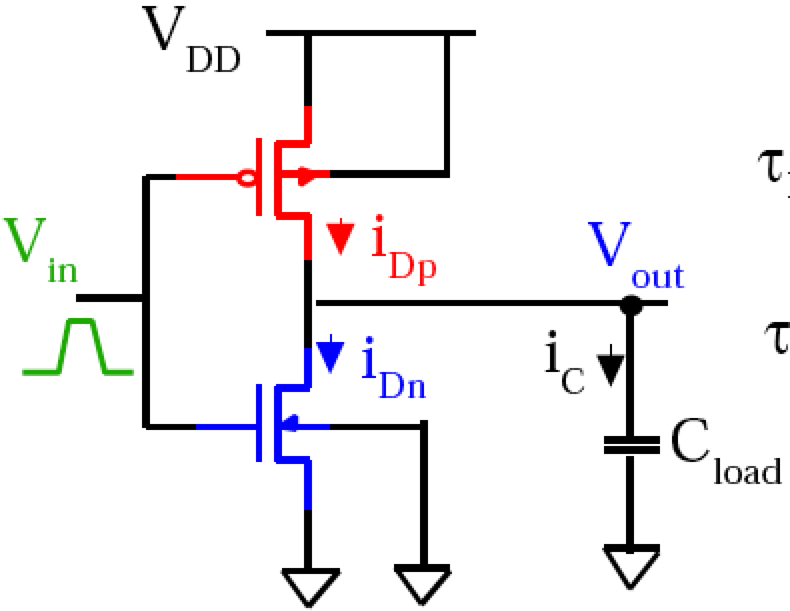
$$\tau_{PLH} = \frac{C_{load} L_p}{\mu_n C_{ox}\left(V_{DD} - \left|V_{T0p}\right|\right)}\left(\frac{1}{W_p}\right)\left[\frac{2\left|V_{T0p}\right|}{V_{DD} - \left|V_{T0p}\right|} + \ln\left(\frac{4\left(V_{DD} - \left|V_{T0p}\right|\right)}{V_{DD}} - 1\right)\right]$$

- Calculation of τ_{PHL}, depends largely on NMOS driver, i.e. nearly same for all INV types.
- Calculation of τ_{PLH}, depends largely on the load device and its operation, i.e. different for all INV types.
- Options to reduce τ_{PHL}, τ_{PLH}:
  - Decrease C_{load}
  - Increase V_{DD}
  - Increase W/L ratio (which usually means increasing W)

Account for Input Waveform Slope







EMPERICAL DELAY CORRECTIONS FOR INPUT τ_r, τ_f:

$$\tau_{PHL}(\text{actual}) = \sqrt{\tau_{PHL}{}^2(\text{step} - \text{input}) + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH}(\text{actual}) = \sqrt{\tau_{PLH}{}^2(\text{step} - \text{input}) + \left(\frac{\tau_f}{2}\right)^2}$$

CMOS INVERTER DELAY DESIGN FORMULAS

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

where $k_n = \mu_n C_{ox}\frac{W_n}{L_n}$

$$\frac{W_n}{L_n} = \frac{C_{load}}{\tau_{PHL}\mu_n C_{ox}(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

where $k_p = \mu_p C_{ox}\frac{W_p}{L_p}$

$$\frac{W_p}{L_p} = \frac{C_{load}}{\tau_{PLH}\mu_p C_{ox}(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

EXAMPLE 6.3

Design a CMOS inverter by determining the W_n and W_p of the nMOS and PMOS transistors to meet the following specs:

-> $V_{th} = 2$ V for $V_{DD} = 5$ V
-> Delay time of 2 ns for a V_{out} transition from 4 V to 1 V, with $C_{load} = 1.0$ pF.

The process and device parameters are specified as follows:

$k_n' = \mu_n C_{ox} = 30\ \mu A/V^2$,
$k_p' = \mu_p C_{ox} = 10\ \mu A/V^2$
$L_n = L_p = 1.0\ \mu m$
$V_{T0n} = 1.0$ V
$V_{T0p} = -1.5$ V
$W_{min} = 2\ \mu m$ (limited by design rules)

STEP #1: Satisfy the Delay Constraint: τ_{PHL} from 4 V to 1 V

HL => PULL-DOWN => τ_{PHL} determined by nMOS driver

NOTE $V_{in} = V_{OH}$ and $1 \leqslant V_{out} \leqslant 4$ V => nMOS LIN

$$C_{load}\frac{dV_{out}}{dt} = -\frac{\mu_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{OH}-V_{T0\,n})\,V_{out}-V_{out}^2\right]$$

$$\tau_{delay} = 2.0\,\mathrm{x}10^{-9}\,\mathrm{s} = -2\,C_{load}\frac{1}{\mu_n C_{ox}\dfrac{W_n}{L_n}}\int_{V_{out}=4}^{V_{out}=1}\frac{dV_{out}}{\left[2(V_{OH}-V_{T0\,n})\,V_{out}-V_{out}^2\right]}$$

$$= -2\,C_{load}\frac{1}{\mu_n C_{ox}\dfrac{W_n}{L_n}}\frac{1}{2(V_{OH}-V_{T0\,n})}\ln\left|\frac{V_{out}}{2(V_{OH}-V_{T0\,n})-V_{out}}\right|\Bigg|_{V_{out}=4}^{V_{out}=1}$$

$$= \frac{-C_{load}}{\mu_n C_{ox}\dfrac{W_n}{L_n}(V_{DD}-V_{T0n})}\left\{\ln\left[\frac{1\mathrm{V}}{2(5-1)\mathrm{V}-1\mathrm{V}}\right]-\ln\left[\frac{4\mathrm{V}}{2(5-1)\mathrm{V}-4\mathrm{V}}\right]\right\}$$

$$2.0\mathrm{x}10^{-9}\,\mathrm{s} = \frac{-1\mathrm{x}10^{-12}\,\mathrm{F}}{\left(30\mathrm{x}10^{-6}\,\mathrm{A}/\mathrm{V}^2\right)\dfrac{W_n}{L_n}(5-1)\mathrm{V}}\left\{\ln\left[\frac{1}{7}\right]-\ln\left[\frac{4}{4}\right]\right\}$$

$$\frac{W_n}{L_n} = \frac{1\,\mathrm{x}10^{-12}\,\mathrm{F}}{(2.0\,\mathrm{x}10^{-9}\,\mathrm{s})(30\,\mathrm{x}10^{-6}\,\mathrm{A/V^2})(4)}\ln(7) = \frac{1}{(2.0)(0.03)(4)}\ln(7) = 8.108$$

$\frac{W_n}{L_n} = 8.108\,,\ L_n = 1\mu m$ => $W_n = 8.108\ (1\ \mu m) = 8.1\ \mu m$

From τ_{delay} spec.

STEP #2: Satisfy the V_{th} constraint, where:

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(5 + (-1.5))V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

$$= \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(3.5)V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = 2\,V$$

=> $k_R = (1.5)^2 = \frac{9}{4}$

$$k_R = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{30\,W_n}{10\,W_p} = 3\frac{W_n}{W_p} = \frac{9}{4}$$

=> $W_p = \frac{4}{9}(3)W_n$

with $L_p = 1\ \mu m$

$$W_p = \frac{4}{9}(3)8.1\mu\,m = 10.8\mu\,m$$

LIMITS TO SCALING DEVICE DIMENSIONS TO REDUCE PROPAGATION DELAYS

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0\,n})}\left[\frac{2V_{T0\,n}}{V_{DD} - V_{T0\,n}} + \ln\left(\frac{4(V_{DD} - V_{T0\,n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0\,p}|)}\left[\frac{2|V_{T0\,p}|}{V_{DD} - |V_{T0\,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0\,p}|)}{V_{DD}} - 1\right)\right]$$

$$k_n = \mu_n C_{ox}\frac{W_n}{L_n} \qquad k_p = \mu_p C_{ox}\frac{W_p}{L_p}$$

If C_{load} = independent of L_n, W_n and L_p, W_p

$$\tau_{PHL} = \frac{C_{load}L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]\boxed{= \frac{k_{PHL}}{W_n}}$$

$$\tau_{PLH} = \frac{C_{load}L_p}{\mu_n C_{ox}\left(V_{DD} - |V_{T0p}|\right)}\left(\frac{1}{W_p}\right)\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T0p}|\right)}{V_{DD}} - 1\right)\right]\boxed{= \frac{k_{PLH}}{W_p}}$$

Also

$$\boxed{\tau_{fall} = \frac{k_{fall}}{W_n}} \qquad \boxed{\tau_{rise} = \frac{k_{rise}}{W_p}}$$

Cload ≈ *Cdbn + Cdbp + Cint + Cgb*

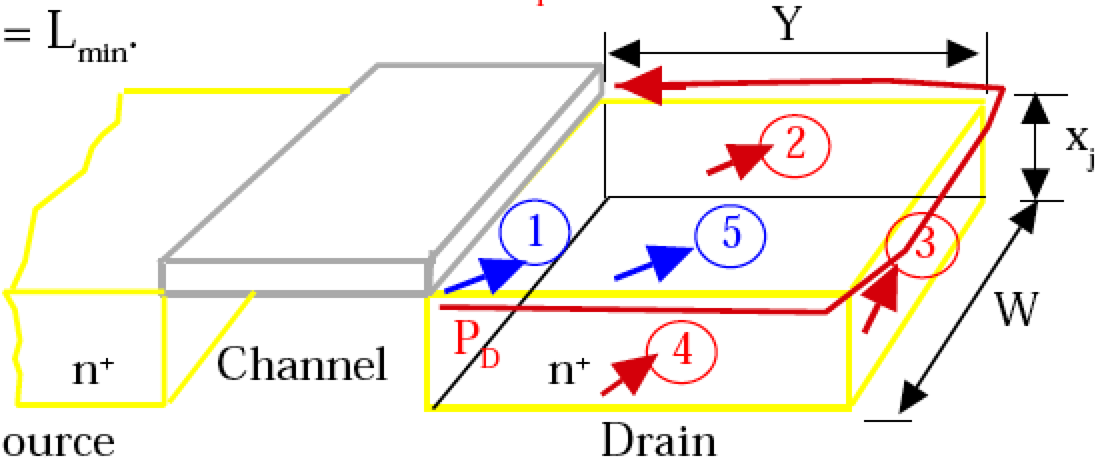
For C_{load} = constant

$$\tau_{PHL} = \frac{k_{PHL}}{W_n} \qquad \lim_{W_n \to \infty} \tau_{PHL} = \lim_{W_n \to \infty} \frac{k_{PHL}}{W_n} \to 0s$$

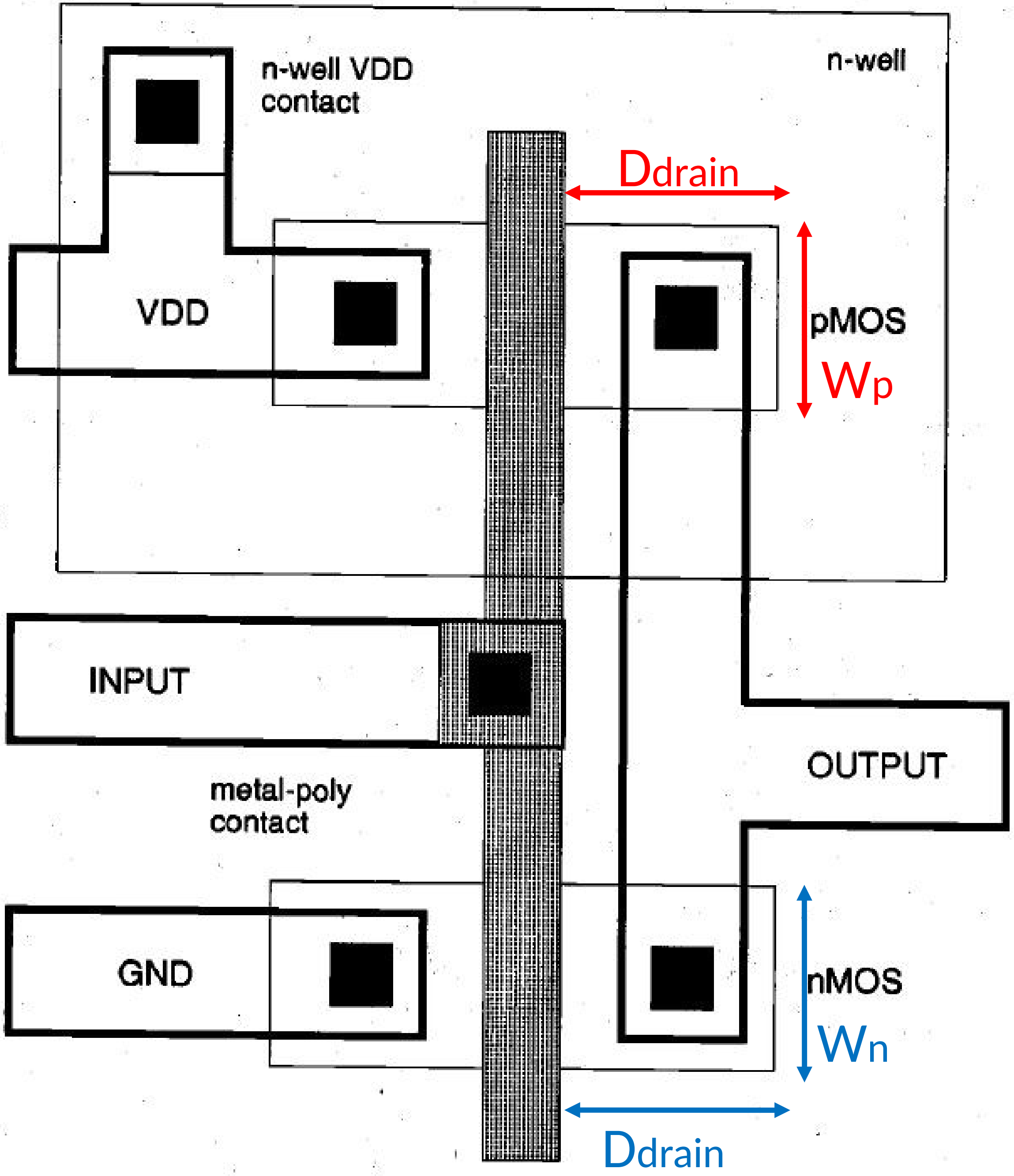
$$\tau_{PLH} = \frac{k_{PLH}}{W_p} \qquad \lim_{W_p \to \infty} \tau_{PLH} = \lim_{W_p \to \infty} \frac{k_{PLH}}{W_p} \to 0s$$

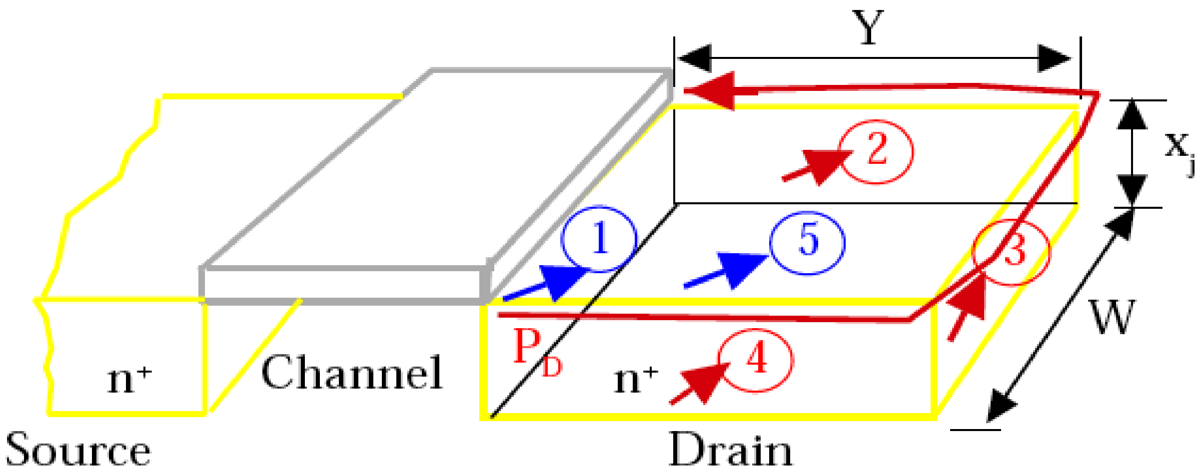
Only when C_{load} is dominated by C_{int} is C_{load} a constant design parameter that is independent of the device dimensions.

In practice, to minimize area, L_n, L_p are set to the minimum dimension , i.e. $L_n = L_p = L_{min}$.



Cload ≈ *Cdbn(Wn) + Cdbp(Wp) + Cint + Cgb*


n-well VDD contact
n-well
Ddrain
VDD
pMOS
Wp
INPUT
OUTPUT
metal-poly contact
GND
nMOS
Wn
Ddrain



$$C_{load} \approx \underbrace{C_{dbn}(W_n) + C_{dbp}(W_p)}_{\text{intrinsic}} + \underbrace{C_{int} + \boxed{C_{gb}}}_{\text{extrinsic}}$$

due to gate capacitance of next stage

where

$$C_{dbn}(W_n) = W_n(Y + x_j)C_{j0n}K_{eqn} + (W_n + 2Y)\ C_{jswn}K_{eqn}$$

$$C_{dbp}(W_p) = W_p(Y + x_j)C_{j0p}K_{eqp} + (W_p + 2Y)\ C_{jswp}K_{eqp}$$

$$C_{load} = \alpha_n W_n + \alpha_p W_p + \alpha_0$$

$$\alpha_0 = 2Y(C_{jswn}K_{eqn} + C_{jswp}K_{eqp}) + C_{int} + C_{gb}$$

$$\alpha_n = K_{eqn}\ ((Y + x_j)C_{j0n} + C_{jswn})$$

$$\alpha_p = K_{eqp}\ ((Y + x_j)C_{j0p} + C_{jswp})$$

$$\tau_{PHL} = \frac{C_{load} L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load} L_p}{\mu_n C_{ox}\left(V_{DD} - \left|V_{T0p}\right|\right)}\left(\frac{1}{W_p}\right)\left[\frac{2\left|V_{T0p}\right|}{V_{DD} - \left|V_{T0p}\right|} + \ln\left(\frac{4\left(V_{DD} - \left|V_{T0p}\right|\right)}{V_{DD}} - 1\right)\right]$$

Let $C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$

$$\frac{C_{load}}{W_p}$$

$$\frac{C_{load}}{W_n}$$

$$\tau_{PHL} = \Gamma_n\left(\frac{\alpha_0 + (\alpha_n + R\alpha_p)W_n}{W_n}\right) \qquad \tau_{PLH} = \Gamma_p\left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p\right)W_p}{W_p}\right)$$

where $R = \frac{W_p}{W_n}$ (set to static parameters, V_{th} in CMOS)

$$\Gamma_n = \left(\frac{L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\Gamma_p = \left(\frac{L_p}{\mu_p C_{ox}\left(V_{DD} - \left|V_{T0p}\right|\right)}\right)\left[\frac{2\left|V_{T0p}\right|}{V_{DD} - \left|V_{T0p}\right|} + \ln\left(\frac{4\left(V_{DD} - \left|V_{T0p}\right|\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \Gamma_n\left(\frac{\alpha_0 + \left(\alpha_n + R\alpha_p\right)W_n}{W_n}\right) \qquad \tau_{PLH} = \Gamma_p\left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p\right)W_p}{W_p}\right)$$

Hence, increasing W_p and W_n will have diminishing influence on τ_{PHL} and τ_{PLH} as they become large, i.e.

$$\tau_{PHL}^{Limit} = \underset{Wn->\infty}{\text{limit}}\ \tau_{PHL} = \Gamma_n\left(\alpha_n + R\alpha_p\right)$$

$$\tau_{PLH}^{Limit} = \underset{Wp->\infty}{\text{limit}}\ \tau_{PHL} = \Gamma_p\left(\frac{\alpha_n}{R} + \alpha_p\right)$$

absolute
minimum
delays

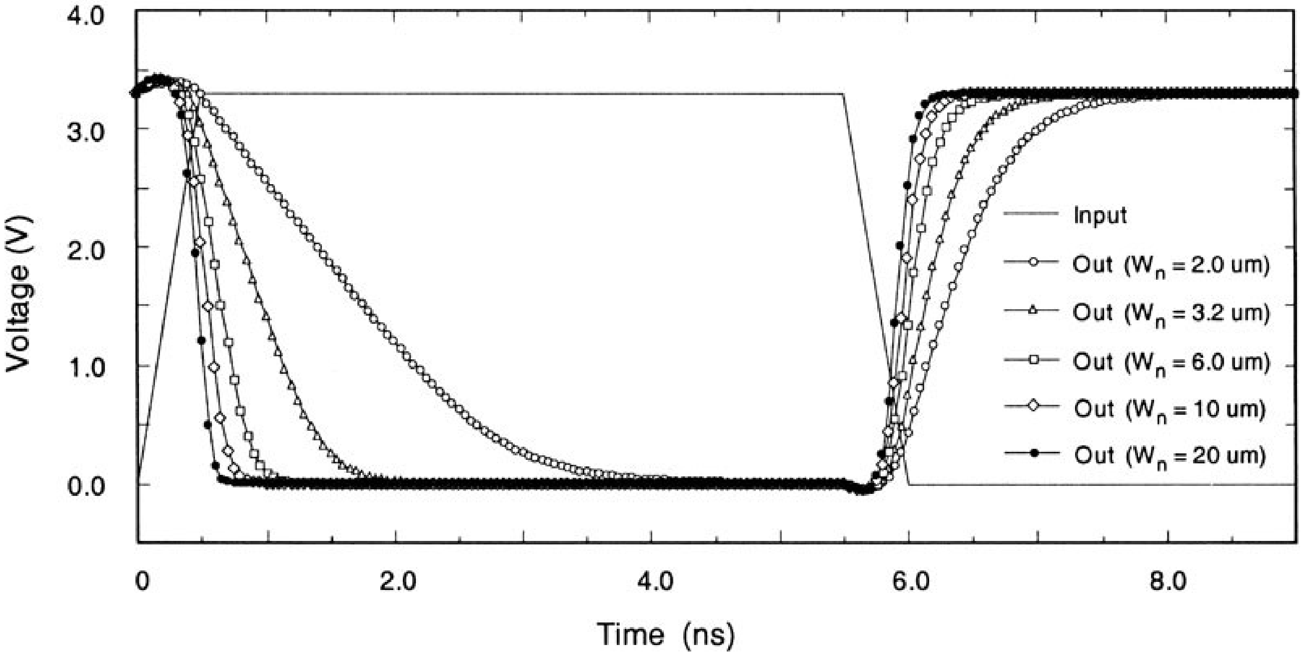
NOTE:

1. τ_{PHL}^{Limit}, τ_{PLH}^{Limit} are independent of $\alpha_0 = f(C_{int}, C_{gb})$.

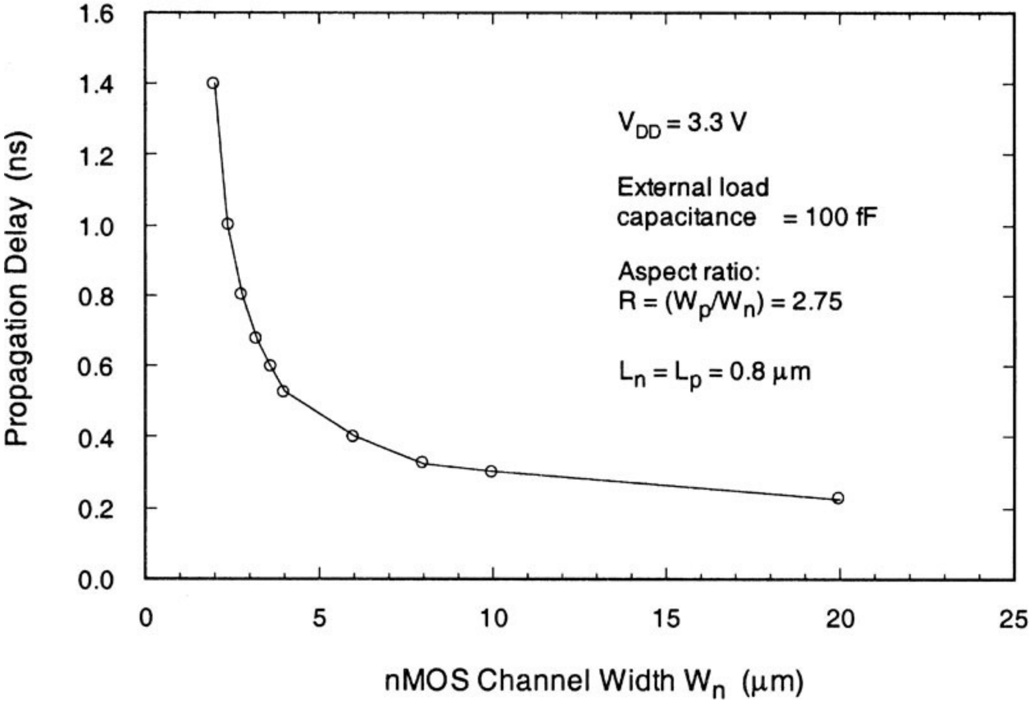
2. Achievement of ABSOLUTE MINIUMUM DELAYS comes with maximum cost, i.e.

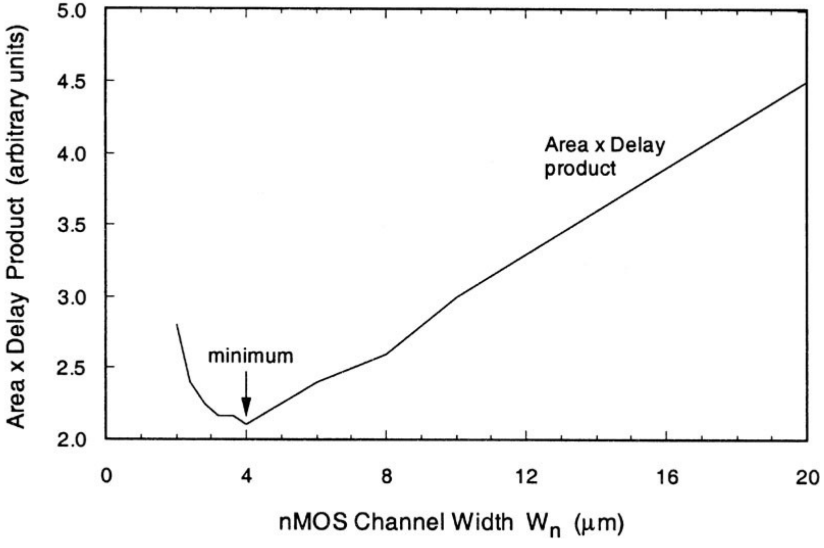
DIE AREA -> Maximized
POWER DISIPATION -> Maximized

Propagation Delay vs. W

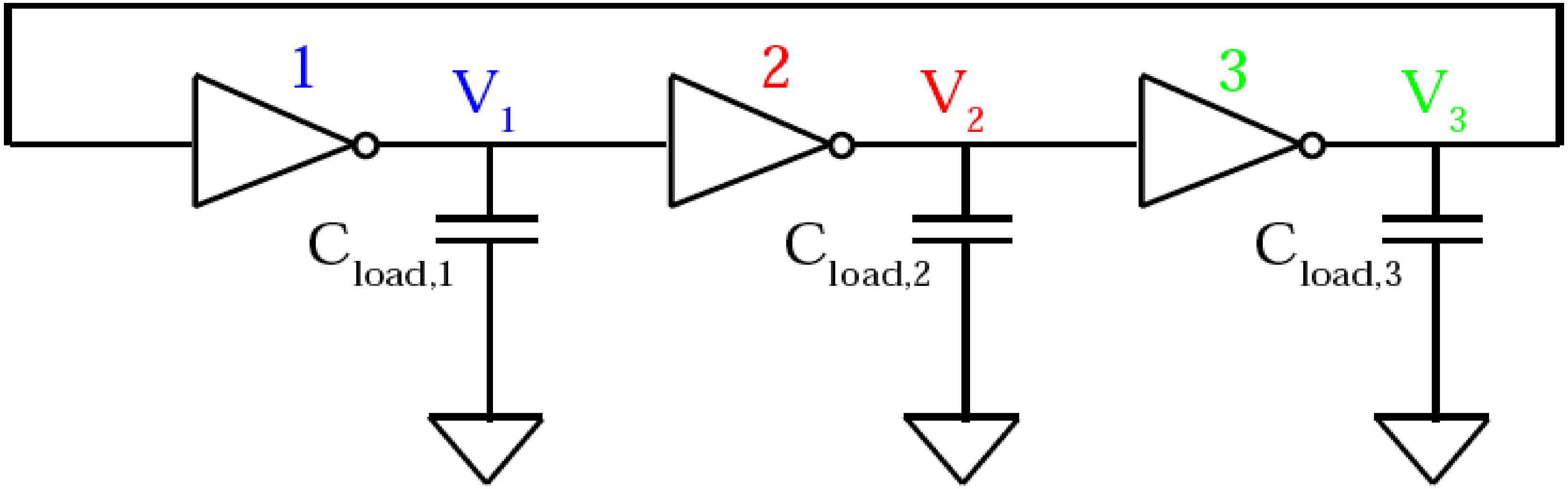


Propagation Delay vs. Area

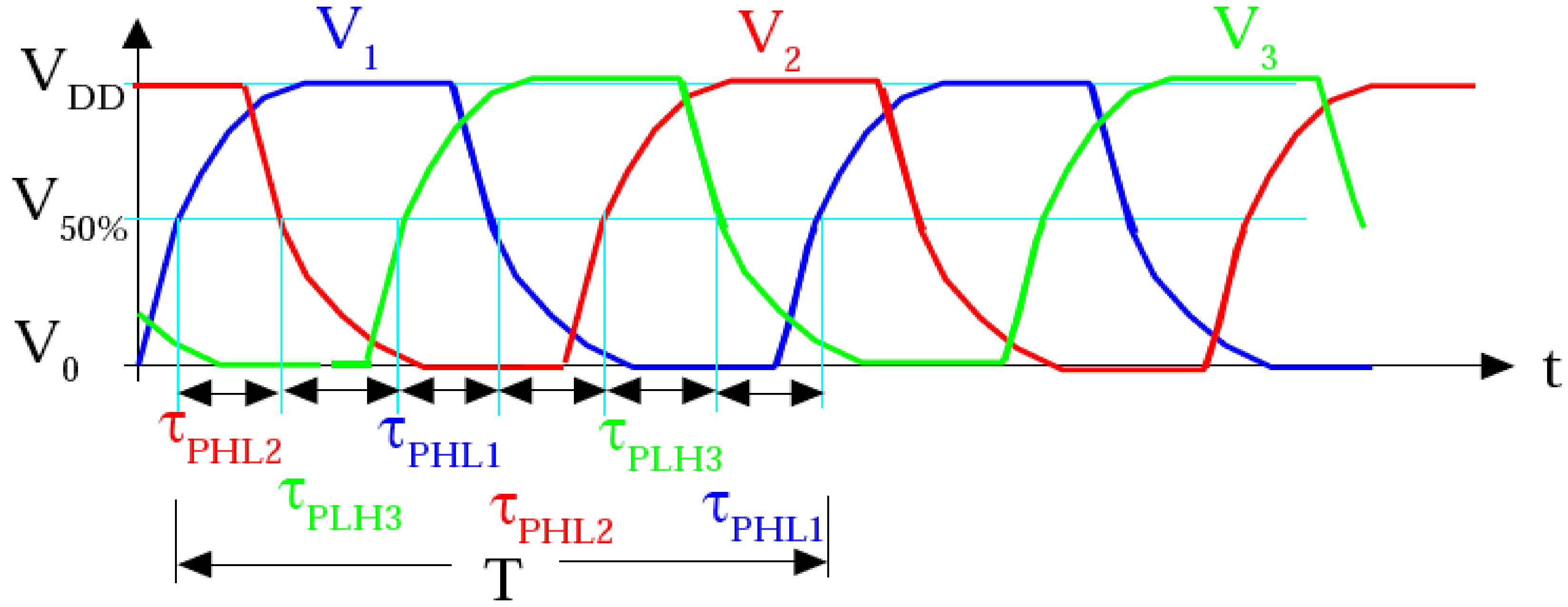


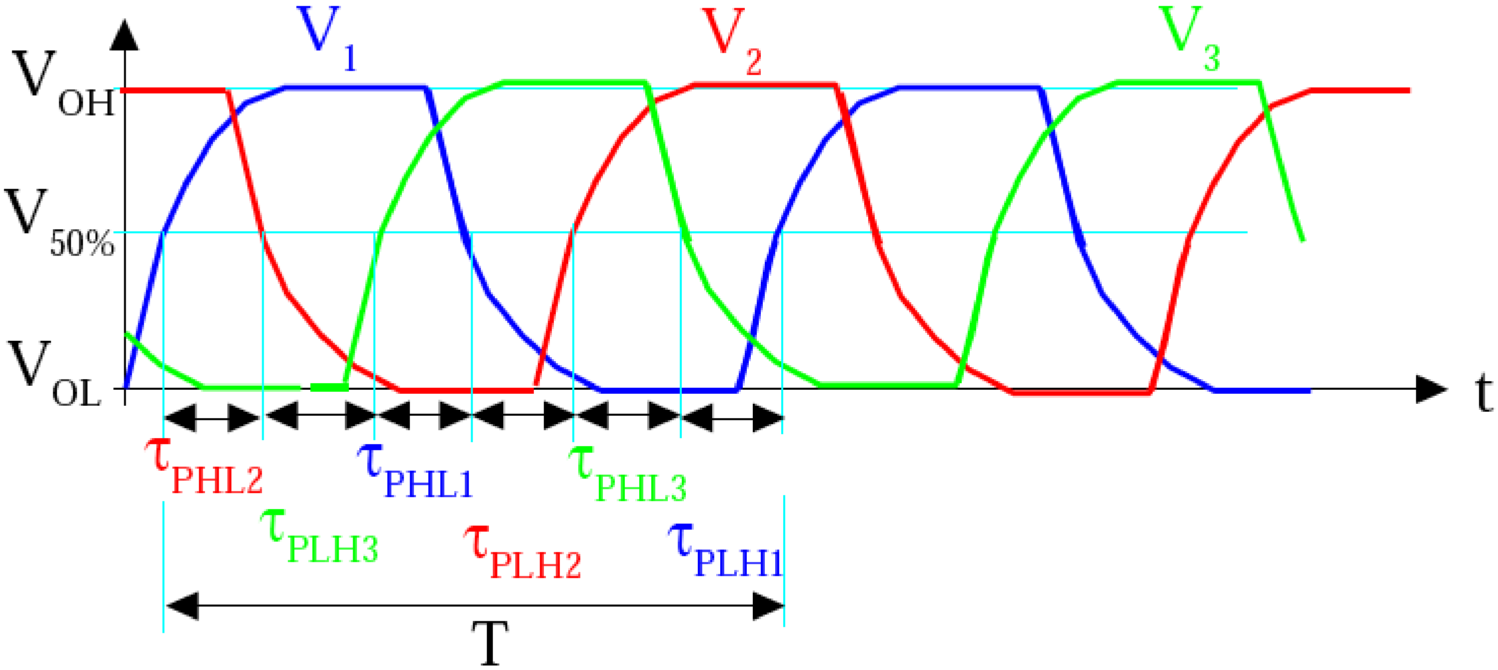


CMOS RING OSCILLATOR



$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3





$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3

$$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH1} = 6\tau_P$$

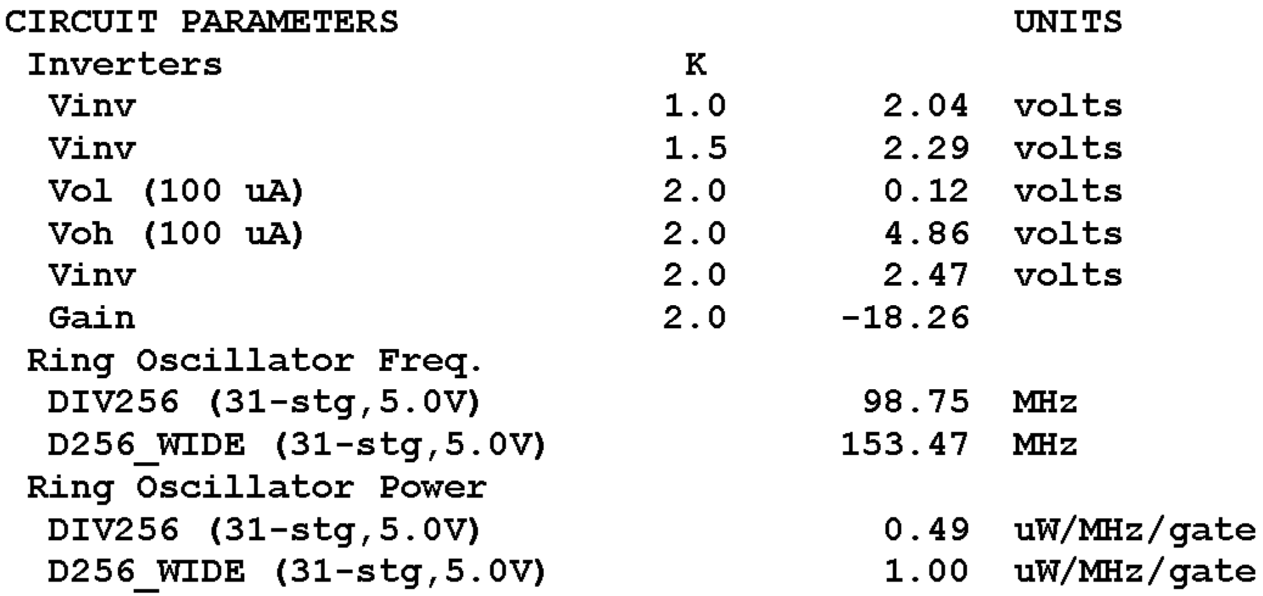
vhere $2\tau_p = \tau_{PHLi} + \tau_{PLHi}$ for i = 1, 2, 3

$$f = \frac{1}{T} = \frac{1}{3 \times 2\tau_p} = \frac{1}{6\tau_p}$$ Oscillation FREQ for 3 INVERTERS

For n INVERTERS:
where n = odd

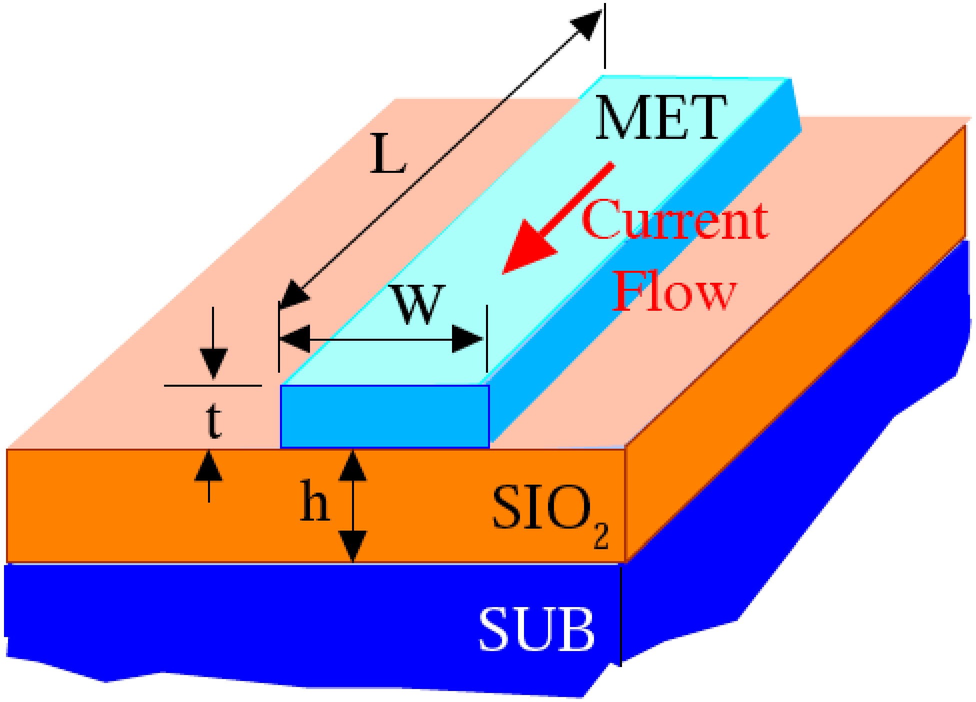
$$f = \frac{1}{T} = \frac{1}{2\,n\,\tau_P} \quad \text{or} \quad \tau_P = \frac{1}{2\,nf}$$

AMI 0.5 micron process



```
CIRCUIT PARAMETERS                                    UNITS
 Inverters                     K
  Vinv                        1.0         2.04  volts
  Vinv                        1.5         2.29  volts
  Vol  (100 uA)               2.0         0.12  volts
  Voh  (100 uA)               2.0         4.86  volts
  Vinv                        2.0         2.47  volts
  Gain                        2.0       -18.26
 Ring Oscillator Freq.
  DIV256 (31-stg,5.0V)                   98.75  MHz
  D256_WIDE (31-stg,5.0V)               153.47  MHz
 Ring Oscillator Power
  DIV256 (31-stg,5.0V)                    0.49  uW/MHz/gate
  D256_WIDE (31-stg,5.0V)                 1.00  uW/MHz/gate
```

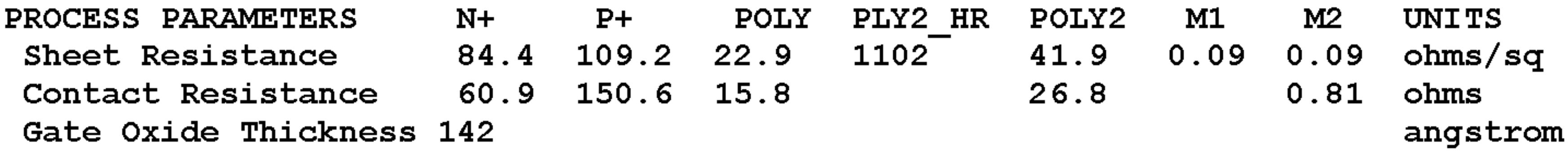
Interconnection Capacitance



PARASITIC RESISTANCE:

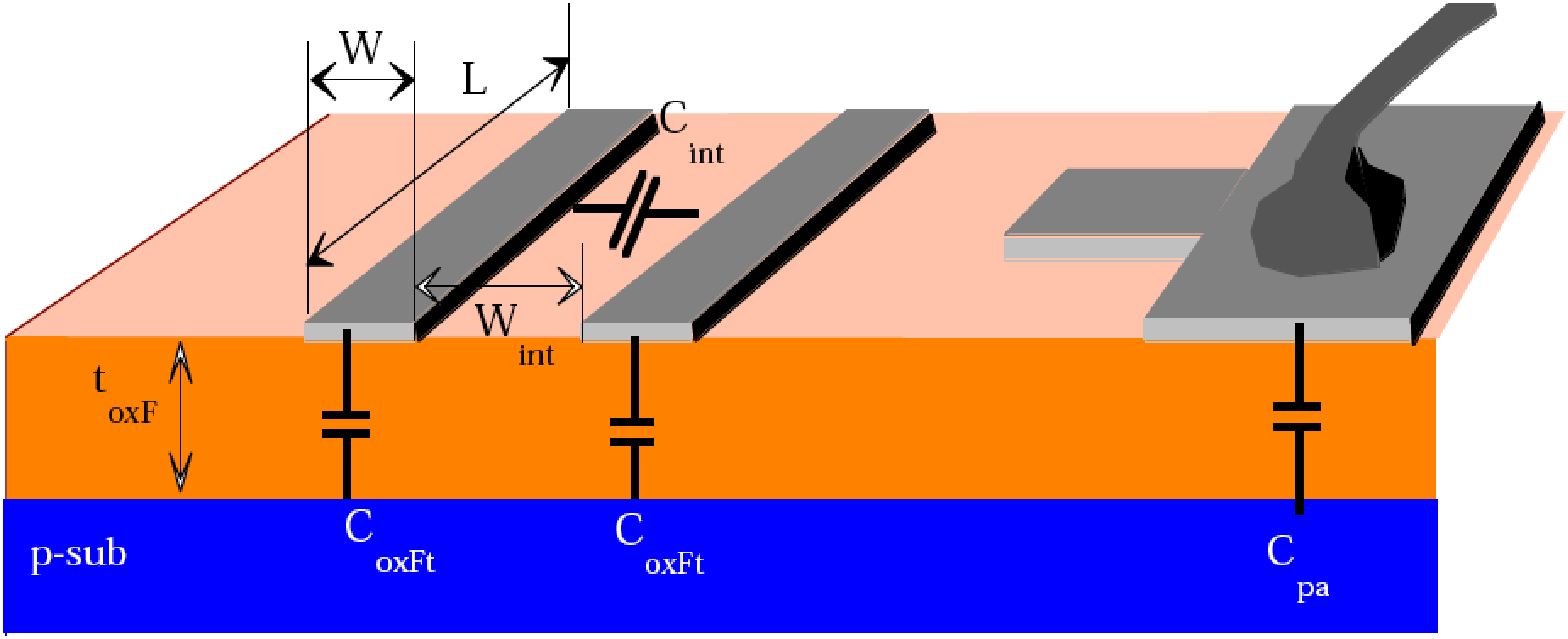
$$R_{metal} = \rho \frac{L}{Wt} = R_{sheet} \frac{L}{W}$$

AMI 0.5 micron process



PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	84.4	109.2	22.9	1102	41.9	0.09	0.09	ohms/sq
Contact Resistance	60.9	150.6	15.8		26.8		0.81	ohms
Gate Oxide Thickness	142							angstrom

Note: Polysilicon vs. Metal resistance!



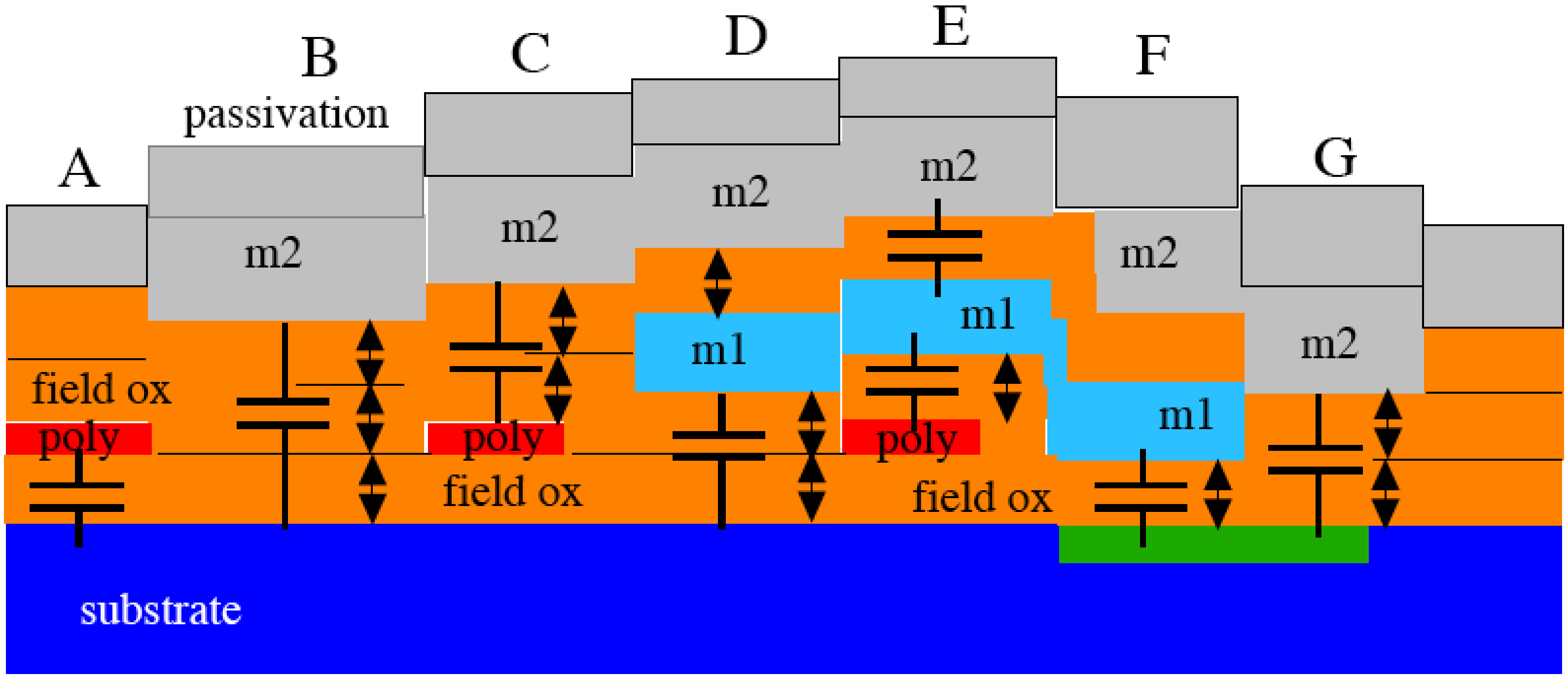
Double-metal double-poly n-well CMOS process

C_{mm} $C_{metal\text{-}to\text{-}metal} = 2.5\ nF/cm^2$

C_{oxm} $C_{metal\text{-}to\text{-}substrate} = 5.2\ nF/cm^2$

C_{oxp} $C_{poly\text{-}to\text{-}substrate} = 6.5\ nF/cm^2$

C_{mp} $C_{metal\text{-}to\text{-}poly} = 12.0\ nF/cm^2$



	Layer	Cap	Ox Thickness	Typ Value
A	Poly-substrate	C_p	3000 Å	50 aF/μm^2
B	Metal2-sub	C_{m2}	9000 Å	20 aF/μm^2
C	Poly-metal2	C_{m2p}	6000 Å	30 aF/μm^2
D	Metal1-sub	C_{m1}	6000 Å	30 aF/μm^2
E	Metal1-poly	C_{m1p}	3000 Å	60 aF/μm^2
E	Metal1-metal2	C_{m2m1}	6000 Å	50 aF/μm^2
F	Metal1-diffusion	C_{m1d}	3000 Å	60 aF/μm^2
G	Metal2-diffusion	Passivation	6000 Å	30 aF/μm^2

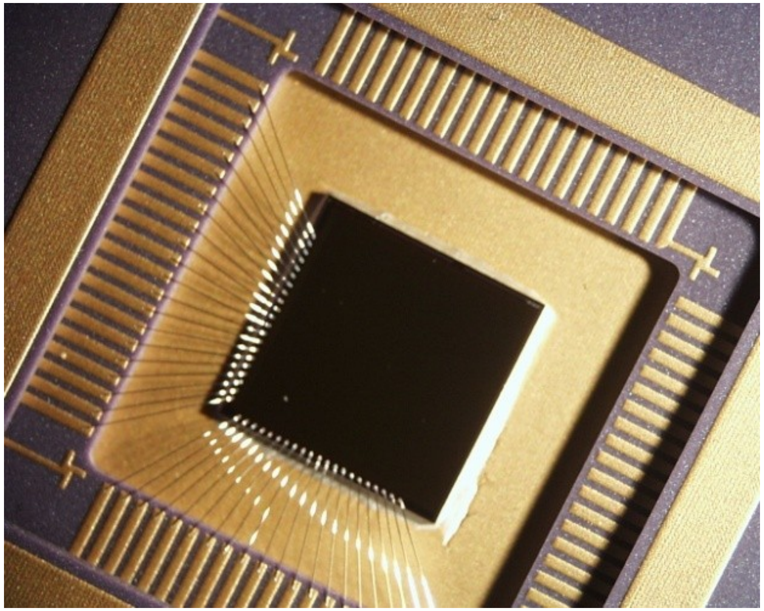
1 µm CMOS Capacitances

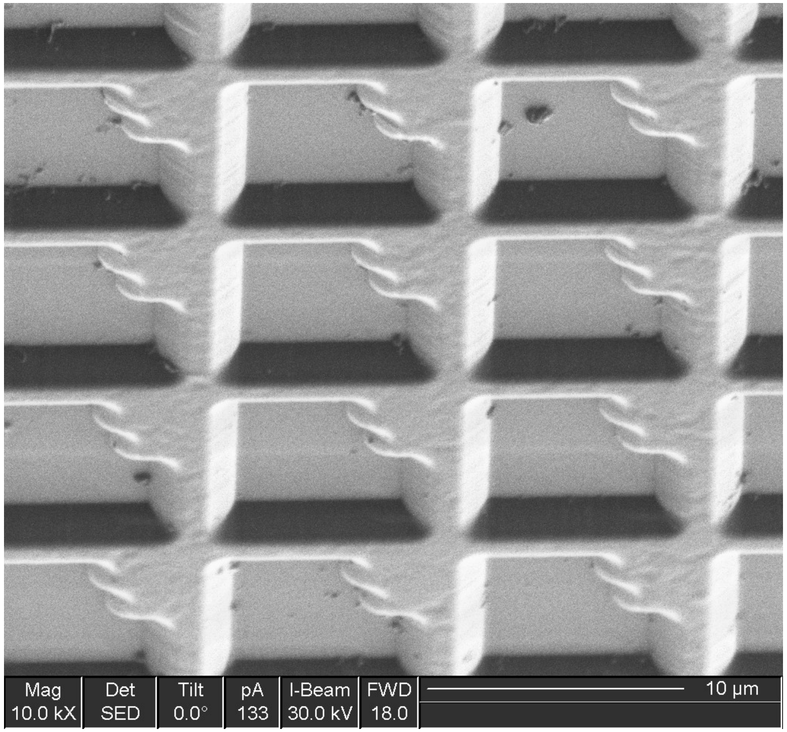
$t_{ox} = 200$Å

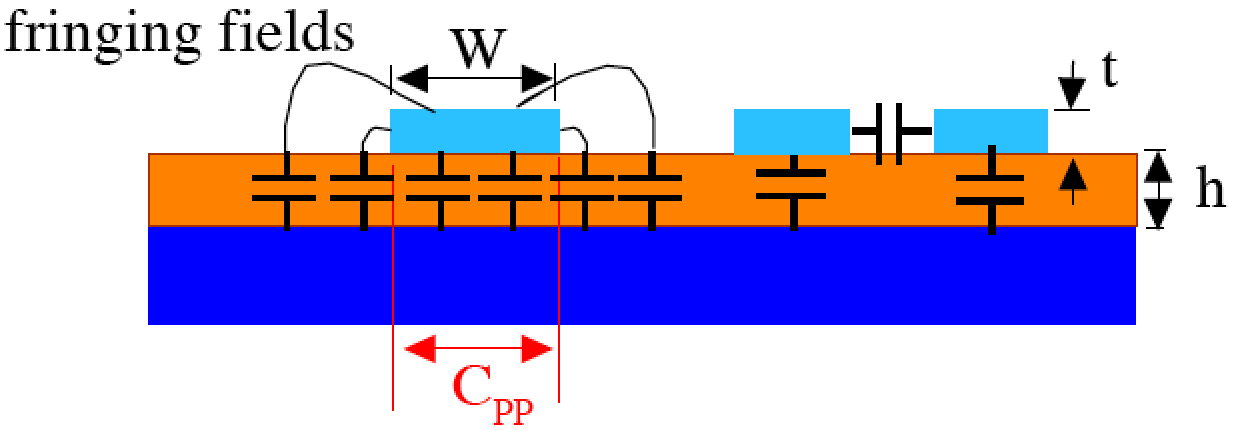
$C_g = 1800$ aF/μm^2

aF = 10^{-18} F

Surface of an IC







$FF = C_{total}/C_{PP}$ -> FRINGING-FIELD FACTOR

FF -> INC as t/h -> INC, W/h <- DEC, and W/L -> INC

(SEE PLOT FF in FIG. 6.18 of TEXT)

$$C_{total} = \varepsilon\left[\frac{W-\frac{t}{2}}{h} + \frac{2\pi}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)}\right] \text{ pF/}\mu\text{m L} \quad \text{for } W \geq t/2$$

$$C_{total} = \varepsilon\left[\frac{W}{h} + \frac{\pi\left(1-0.0543\frac{t}{2h}\right)}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)} + 1.47\right] \text{ pF/}\mu\text{m L} \quad \text{for } W < t/2$$

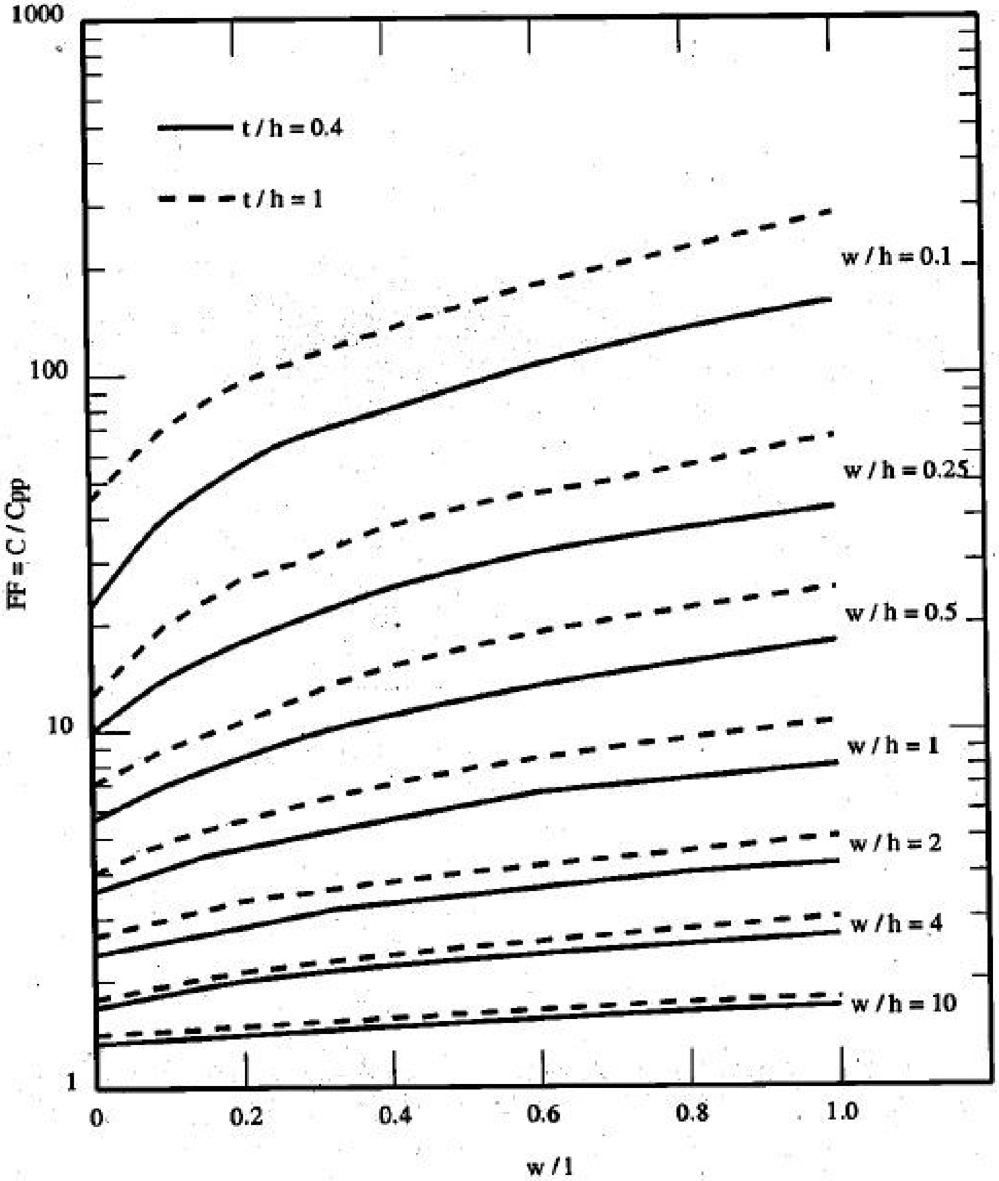
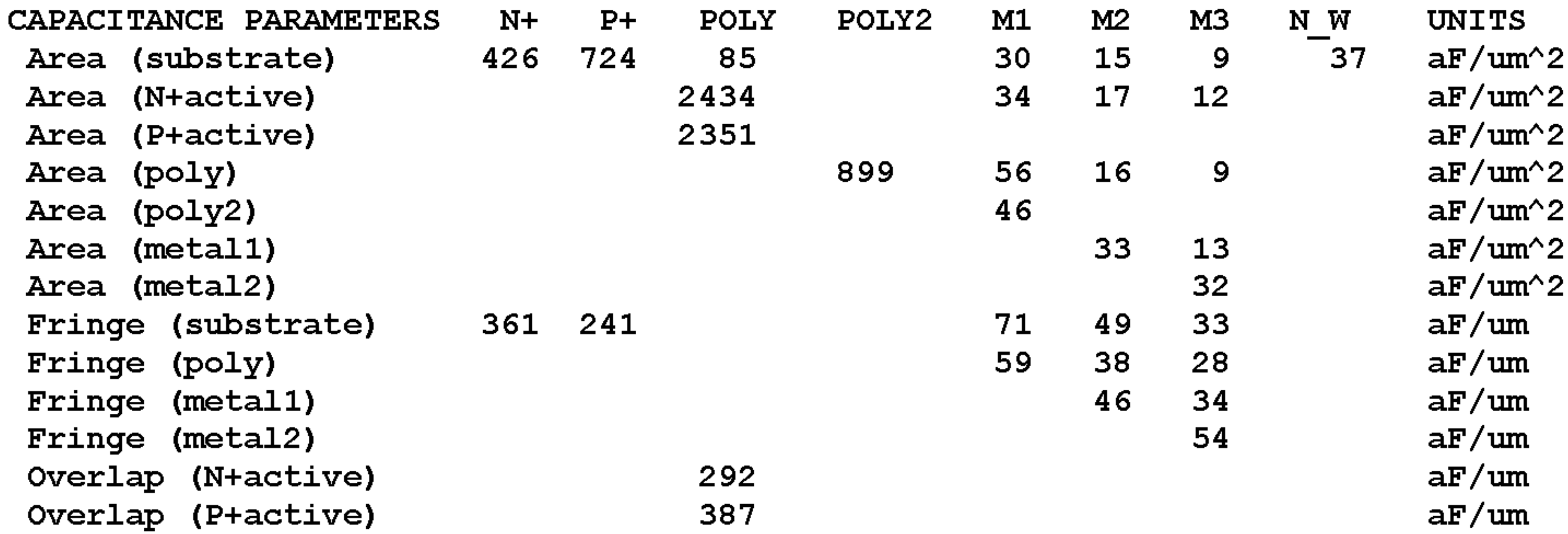
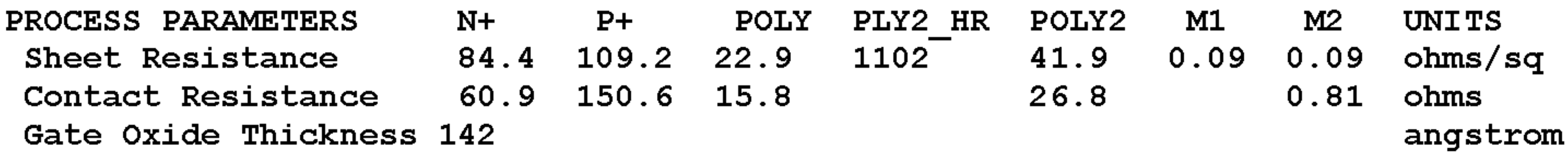


Figure 6.18. Variation of the fringing-field factor with the interconnect geometry.

AMI 0.5 micron process

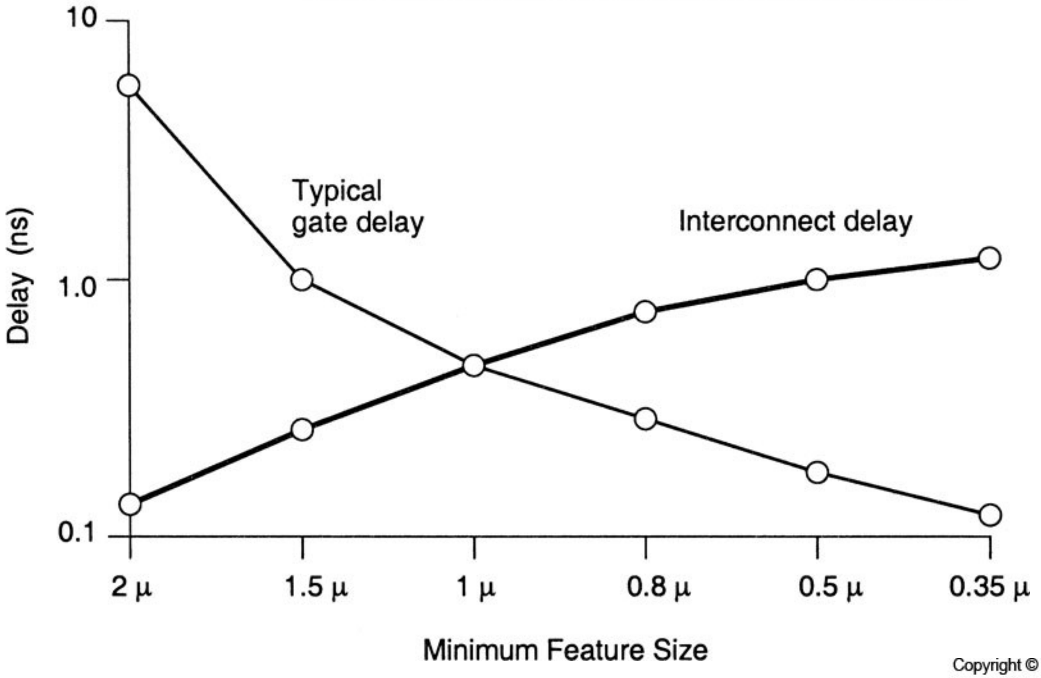


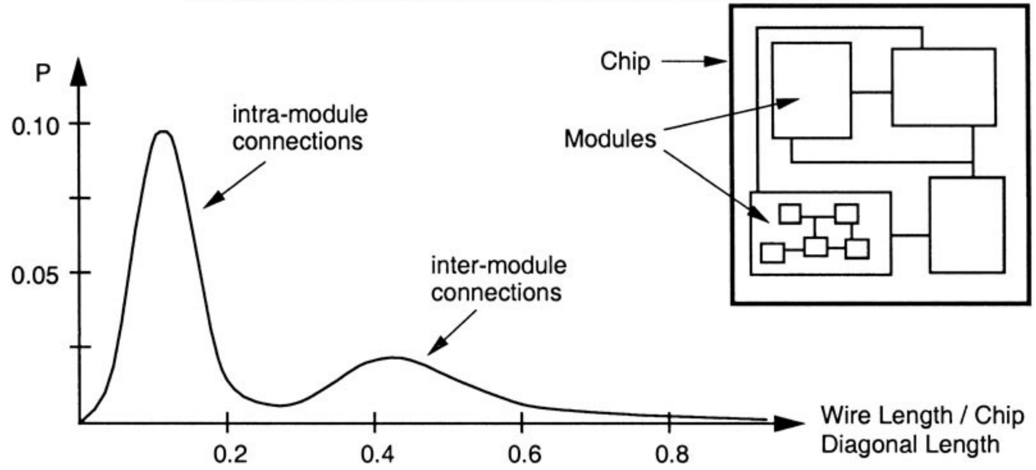
```
CAPACITANCE PARAMETERS   N+   P+   POLY   POLY2   M1   M2   M3   N_W    UNITS
 Area (substrate)       426  724    85            30   15    9     37   aF/um^2
 Area (N+active)                  2434            34   17   12          aF/um^2
 Area (P+active)                  2351                                  aF/um^2
 Area (poly)                              899     56   16    9          aF/um^2
 Area (poly2)                                     46                    aF/um^2
 Area (metal1)                                         33   13          aF/um^2
 Area (metal2)                                              32          aF/um^2
 Fringe (substrate)     361  241                  71   49   33          aF/um
 Fringe (poly)                                    59   38   28          aF/um
 Fringe (metal1)                                       46   34          aF/um
 Fringe (metal2)                                            54          aF/um
 Overlap (N+active)                292                                  aF/um
 Overlap (P+active)                387                                  aF/um
```



```
PROCESS PARAMETERS     N+     P+     POLY  PLY2_HR  POLY2   M1    M2    UNITS
 Sheet Resistance      84.4  109.2  22.9   1102     41.9   0.09  0.09  ohms/sq
 Contact Resistance    60.9  150.6  15.8            26.8         0.81  ohms
 Gate Oxide Thickness 142                                              angstrom
```

Interconnection Delays in Sub-micron process





Examples of Propagation Delay

Product	**CMOS technology generation**	**Clock frequency, *f***	**Fan-out=4 inverter delay**
Pentium II	0.25 µm	600 MHz	~100 ps
Pentium III	0.18 µm	1.8 GHz	~40 ps
Pentium IV	0.13 µm	3.2 GHz	~20 ps

Typical clock periods:
- high-performance µP: ~15 FO4 delays
- PlayStation 2: 60 FO4 delays

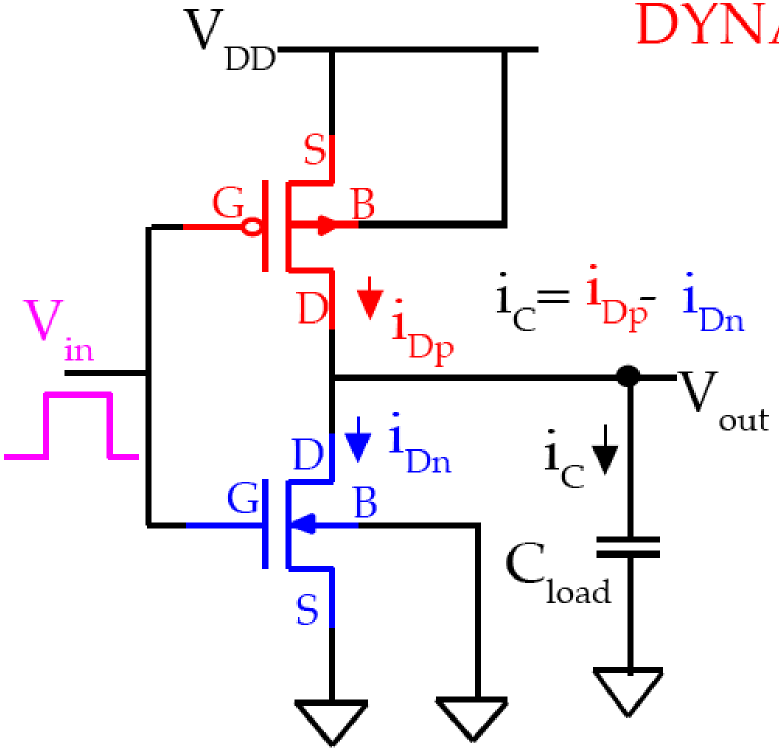
POWER DISSIPATION

P_s = Static power dissipation due to leakage current or other current drawn continuously from the power supply.

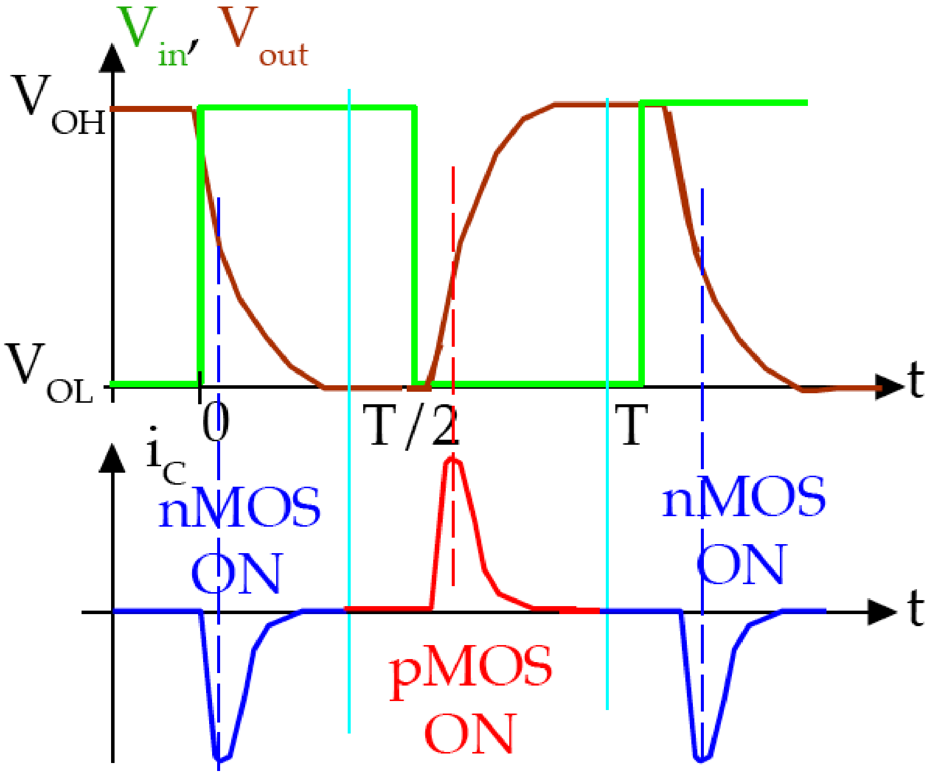
P_d = dynamic power dissipation due to charging and discharging load capacitances (v_{in} assumed to be square-like)

P_{sc} = short circuit power dissipation due to charging and discharging load capacitances during the finite rise and fall times of v_{in}.

DYNAMIC POWER DISSAPATION



$$i_C = i_{Dp} - i_{Dn}$$

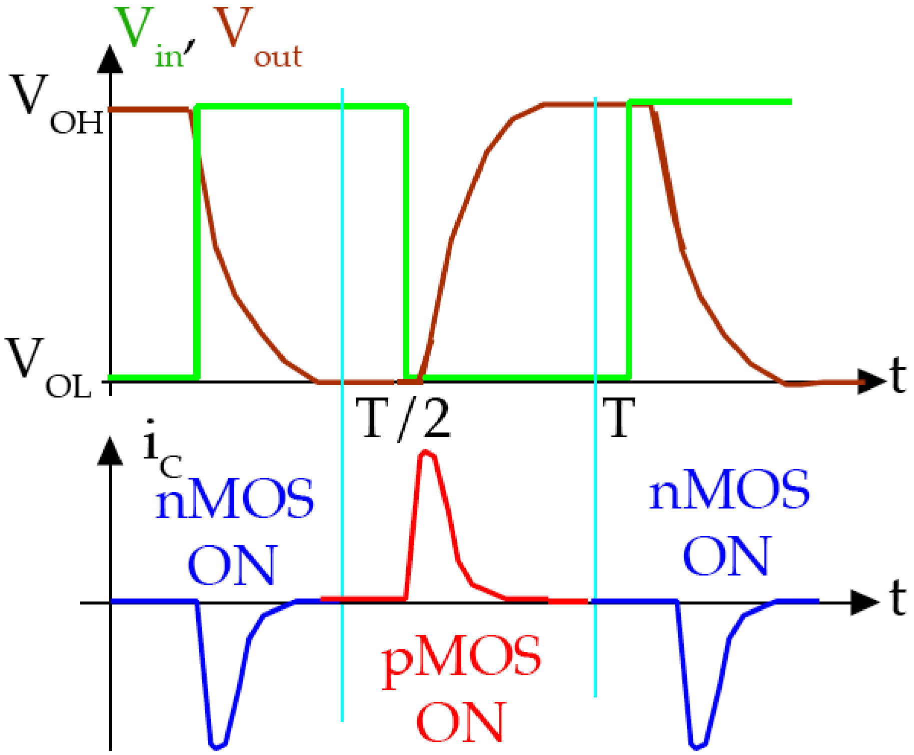


$$P_{avg} = \frac{1}{T}\int_0^T v(t)i(t)dt$$

$$P_{avg} = \frac{1}{T}\int_0^{T/2} V_{out}(t)\, i_{Dn}(t)\, dt + \frac{1}{T}\int_{T/2}^{T} \left(V_{DD} - V_{out}(t)\right) i_{Dp}(t)\, dt$$

where $i_{Dn}(t) = -C_{load}\frac{dV_{out}}{dt}$ $\quad i_{Dp}(t) = C_{load}\frac{dV_{out}}{dt}$

$$P_{avg} = \frac{1}{T}\int_{0}^{T/2} V_{out}(t)\left(-C_{load}\frac{dV_{out}}{\cancel{dt}}\right)\cancel{dt} + \frac{1}{T}\int_{T/2}^{T}\left(V_{DD}-V_{out}(t)\right)\left(C_{load}\frac{dV_{out}}{\cancel{dt}}\right)\cancel{dt}$$



$$P_{avg} = \frac{1}{T}\int_{V_{DD}}^{0} -C_{load}V_{out}(t)\,dV_{out} + \frac{1}{T}\int_{0}^{V_{DD}} C_{load}\left(V_{DD}-V_{out}(t)\right)dV_{out}$$

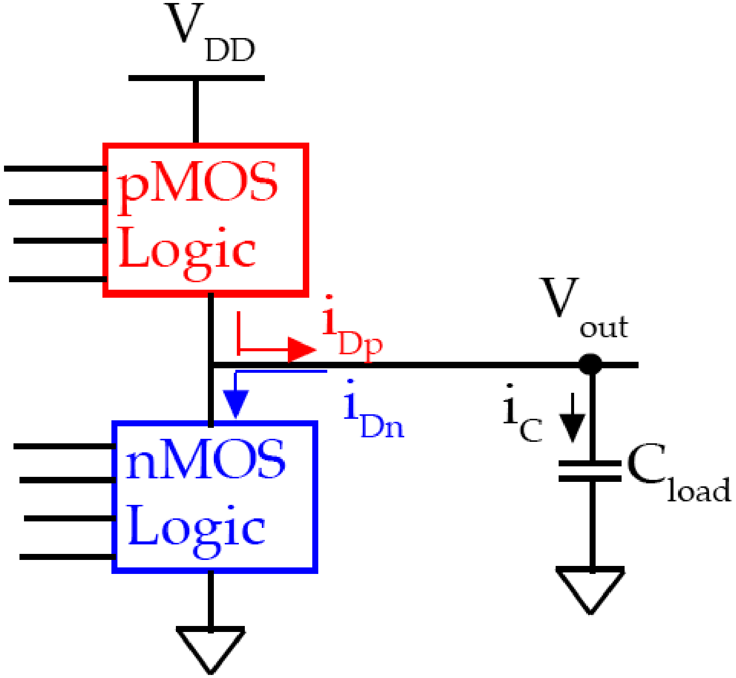
$$= \frac{1}{T}\left[-C_{load}\frac{V_{out}^{2}}{2}\Bigg|_{V_{out}=V_{DD}}^{V_{out}=0} + C_{load}\left(V_{DD}V_{out}-\frac{V_{out}^{2}}{2}\right)\Bigg|_{V_{out}=0}^{V_{out}=V_{DD}}\right]$$

$$P_{avg} = \frac{1}{T}\left[-C_{load}\frac{V_{out}^2}{2}\Bigg|_{V_{out}=V_{DD}}^{V_{out}=0} + C_{load}\left(V_{DD}V_{out} - \frac{V_{out}^2}{2} \right)\Bigg|_{V_{out}=0}^{V_{out}=V_{DD}} \right]$$

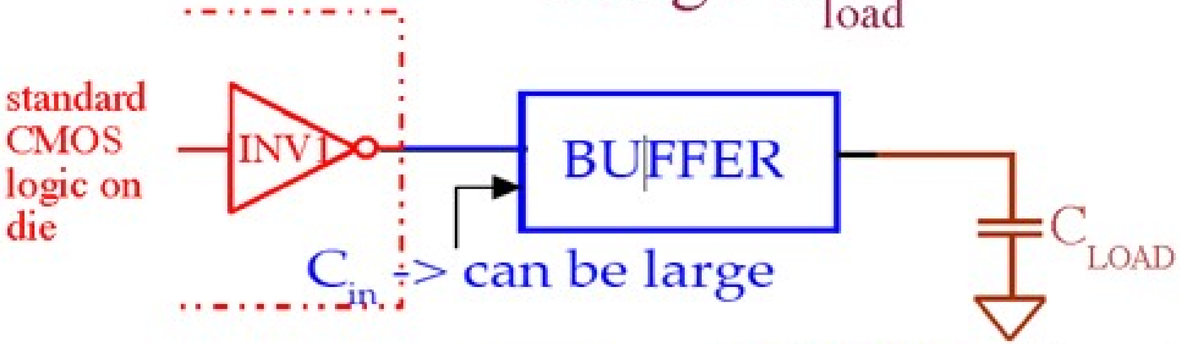
$$= \frac{1}{T}C_{load}V_{DD}^2$$

$$P_{avg} = C_{load}V_{DD}^2\, f$$

APPLIES TO GENERAL CMOS LOGIC CIRCUITS

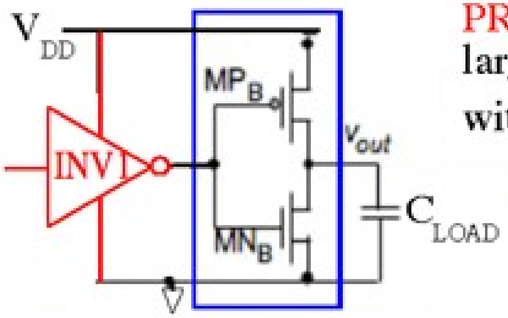


Cascade of N Inverters or Super-Buffer to Drive Large C_{load}



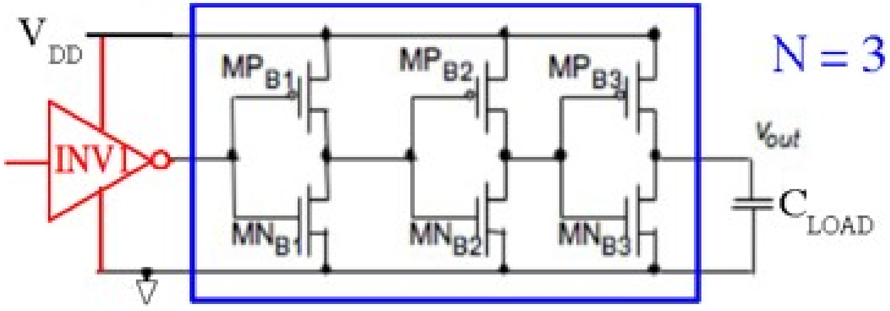
standard CMOS logic on die

C_{in} -> can be large



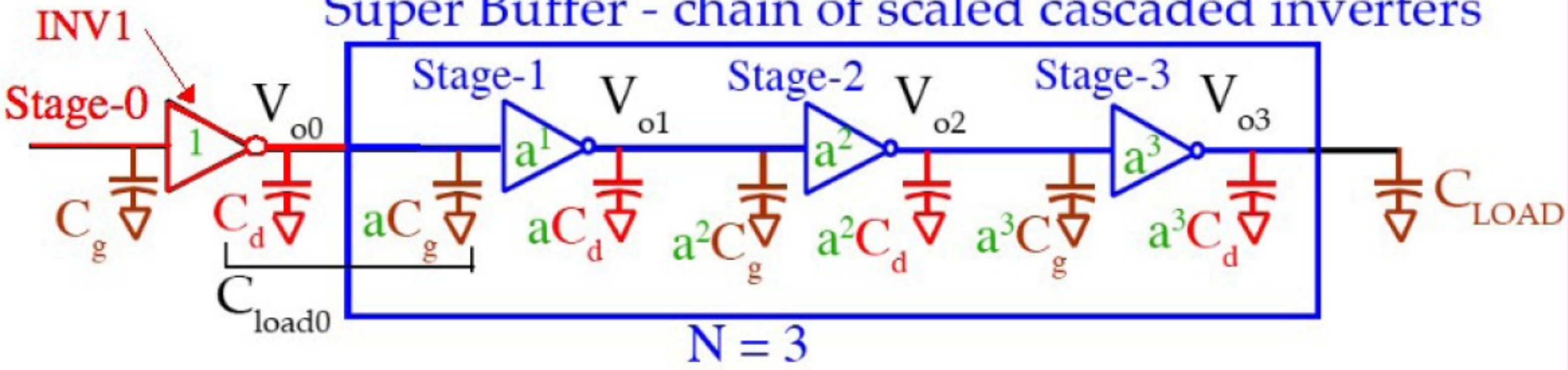
PROBLEM: A minimum sized inverter drives a large load C_{LOAD}, leading to excessive delay, even with a large buffer (large W/L).

SOLUTION: Insert N inverter stages in cascade with increasing W/L between INV1 and load C_{LOAD}. The total delay through N stages will be less than the delay through a singe stage driving C_{LOAD}.



Cascade of N Inverters or Super-Buffer to Drive Large C_{load} cont.

Super Buffer - chain of scaled cascaded inverters



CONSIDER N stages, where N is a variable, and $a^{N+1} = C_{LOAD}/C_g$

$W_{ni} = a^i W_{n0}$ and $W_{pi} = a^i W_{p0}$ for i = 0, 1, ..., N

$C_{loadi} = a^i(C_d + aC_g)$ for i = 0, 1, ..., N and $a^{N+1} = C_{LOAD}/C_g$

NOTE: ALL inverters have the same delay

$$t_d = \frac{\tau_0}{a^i}\frac{a^i(C_d + aC_g)}{C_d + C_g} = \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

where i = 1,...,N; τ_0 is the gate delay for INV1 in a ring oscillator with load $C_d + C_g$

$$t_{total} = (N+1)\cdot t_d = (N+1)\cdot \tau_0 \cdot \frac{C_d + aC_g}{C_d + C_g}$$

Choose N and a to minimize t_{total}

where $a^{N+1} = C_{LOAD}/C_g$ & $N+1 = \frac{\ln(C_{LOAD}/C_g)}{\ln(a)}$

Cascade of N Inverters or Super-Buffer to Drive Large C_{load} cont.

$$\left.\begin{aligned} t_{total} &= (N+1)\tau_0 \frac{C_d + aC_g}{C_d + C_g} \\ N+1 &= \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)} \end{aligned}\right] \Rightarrow \quad t_{total} = \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)} \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

$$W_{ni} = a^i W_{n0} \quad \text{and} \quad W_{pi} = a^i W_{p0}$$

TO MINIMIZE t_{total}:

$$\frac{dt_{total}}{da} = \tau_0 \ln\left(\frac{C_{LOAD}}{C_g}\right) \underbrace{\left[-\frac{1/a}{(\ln(a))^2}\left(\frac{C_d + aC_g}{C_d + C_g}\right) + \frac{1}{\ln(a)}\left(\frac{C_g}{C_d + C_g}\right)\right]}_{=0} = 0$$

$$a_{opt}\left[\ln\left(a_{opt}\right) - 1\right] = \frac{C_d}{C_g} \qquad \boxed{a_{opt} \geq e = 2.718}$$

For the SPECIAL CASE $C_d = 0 \Rightarrow \ln(a_{opt}) = 1$ or $a_{opt} = e^1 = 2.718$

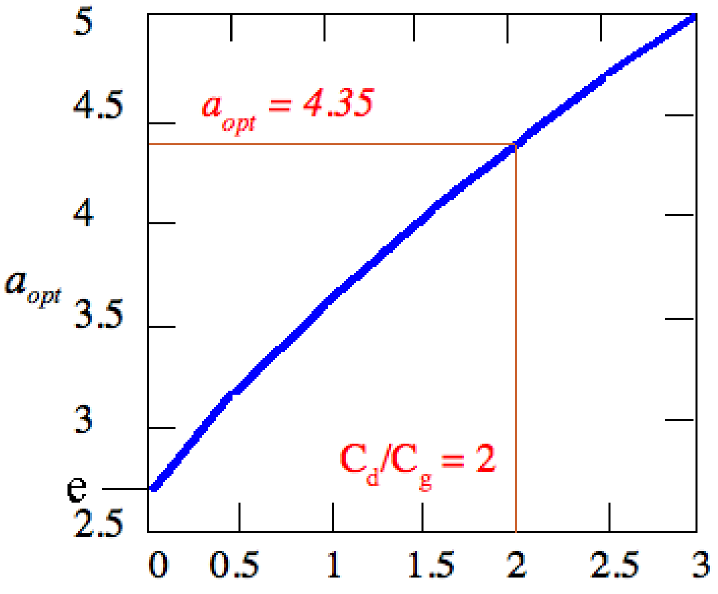
Since $C_d > C_g$, $C_d = 0$ is only an academic special case.

Cascade of N Inverters or Super-Buffer to Drive Large C_{load} cont.

EXAMPLE: Design a Buffer using a scaled cascade of inverters to achieve minimum total delay t_{total} when $C_{LOAD} = 100\ C_g$. Consider the case where $C_d = 2C_g$.

$C_d = 2C_g$ => plot a_{opt} as function of C_d/C_g: $a_{opt} = 4.35$ => $\ln(a_{opt}) = 1.47$

Plot using Excel, MathCad, MatLab.



$$\frac{C_d}{C_g}=a_{opt}\cdot(\ln a_{opt}-1)$$

$$N+1=\frac{\ln(C_{LOAD}/C_g)}{\ln(a_{opt})}$$

$$\Rightarrow N=\frac{\overset{4.61}{\boxed{\ln(C_{LOAD}/C_g)}}}{1.47}-1=2.13\rightarrow N=3$$

$$e^{3.13*1.47}=100\le\frac{C_{LOAD}}{C_g}\le e^{4*1.47}=365$$

i	W_{ni}/W_{n0}	W_{pi}/W_{p0}
1	$(a_{opt})^1 = 4.35$	$(a_{opt})^1 = 4.35$
2	$(a_{opt})^2 = 18.92$	$(a_{opt})^2 = 18.92$
3	$(a_{opt})^3 = 82.31$	$(a_{opt})^3 = 82.31$

3rd stage can be eliminated with little impact.