JEE 2600 Fall 2018 Exam 2 Study Guide

Exam 2 will primarily cover material in chapter 4, 5, and 6. Each new topic in this class builds upon old material, so the topics from exam 1 are likely to be on this test. Be sure to understand the following topics:

All the material from the exam 1 study guide.

Chapter 4:
- Counters – Modulo counter, count enable, terminal count
- Register files

Chapter 5:
- RTL design and High Level State Machines (HLSM)
    - Defining HLSMs from a word description
    - RTL design process
        - How to derive the datapath
        - How to derive the FSM
        - Make sure you know what the mathematical symbols mean
            - << or >> Bit shifter
            - * Multiplier
            - + Adder
            - >, <, == Comparator
            - Etc …
    - Using memories/register files in HLSMs
- Timing diagrams for HLSMs
- Using memories
- How to create larger memory arrays from smaller components
- Understand the difference between RAM and ROM memories

Chapter 6:
- Two level optimization
- Karnaugh maps
- Essential prime implicants and implicates. Non-essential prime implicants and implicates
- Don't Cares
- Optimized SOP or POS
- Faster Adders
- RTL Optimization
- Latency vs. Throughput
- Concurrent vs. Serial

Note: This is not an exclusive list of topics to study, but a high level guideline.