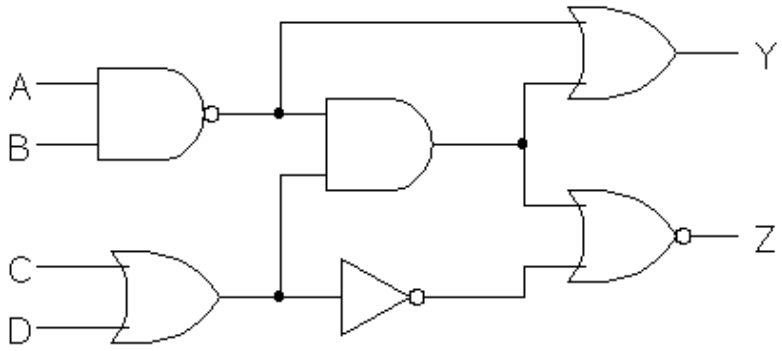
1. Convert the decimal number 435.64 to binary, octal, and hexadecimal.

2.
Part A. Convert the circuit below into NAND gates. Insert or remove inverters as necessary.

Part B. What is the propagation delay from any input to any output for both the original circuit and the NAND gate circuit from part A. Use 1 nS for inverters, 2 nS for NAND, 3 nS for NOR, 4 nS for AND, and 5 nS for OR gates.



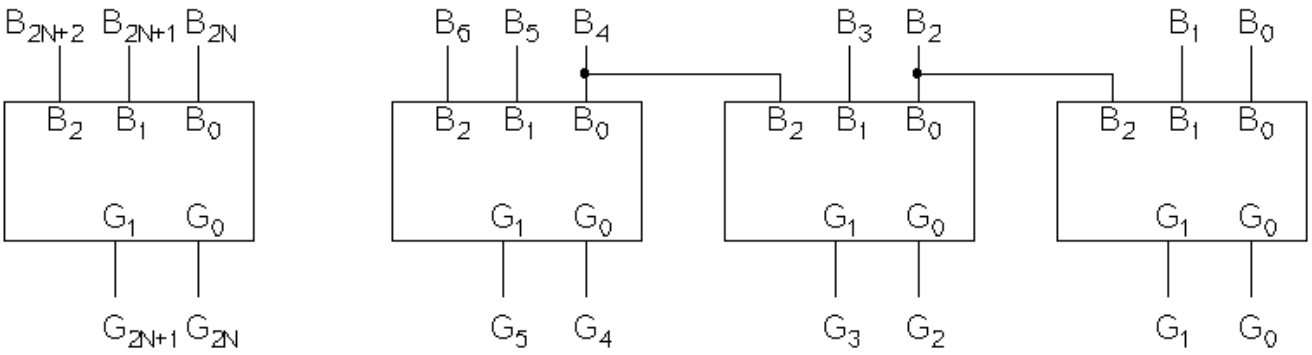
3. Follow the design procedure to design a circuit to add two 2-bit binary numbers. Show truth table, sum-of-minterms or product-of-maxterms, and draw a circuit.

4. Design a circuit to implement the following equation using an 8 to 1 multiplexer and on inverter.

$$F(A,B,C,D) = \Sigma m(0,2,4,5,8,9,10,11,13)$$

5. Design a circuit to implement a Full Adder using one 3 to 8 line decoder and OR gates as necessary.

6. Use the design procedure to design a binary to Gray code converter cell. Each cell has three inputs and two outputs. The three inputs would be an even binary bit and the next two more significant bits. The output bits are the corresponding even Gray code bit and the next more significant bit. Show the truth table, K-maps, minimized sum of products or product of sums, and draw a cell circuit. The cell would be used in a circuit as shown below where N is the cell number.



7. Multiply 3A.C and 26.8 hexadecimal numbers.

8. Design a circuit to implement the following equation using a 4 to 16 line decoder and 3-input OR gates.

$$F = B'D' + A'BC' + AC'D + AB'$$

9. Follow the design procedure to design a 2-bit by 2-bit multiplier. Show truth table, sum-of-minterms, or product-of-maxterms, and draw a circuit.

10. Design a circuit that converts a two digit BCD number (8 bits total) to binary number. Use only full adders in your design and minimize the number of full adders.

11. Prove the identity of the following Boolean equation, using algebraic manipulation

$$AB + BC'D' + A'BC + C'D = B + C'D$$

12. Using the design procedure design a 4-bit input priority encoder. The priority encoder has the following requirements:

- Four input bits
- The binary output value is the bit position of the most significant bit that is a one.
- The binary output has enough bits to represent the bit position of the most significant input bit.
- There is an additional output bit to indicate an error.
- If all of the input bits are zeros the error output signal is one.

Part A: Create a truth table.
Part B: Write sum-of-minterms or product-of-maxterms equations for your circuit.
Part C: Draw a circuit schematic of your design.

13. Design a Mealy model circuit that detects the bit pattern 0110110 in a

serial stream of data no matter where the sequence appears in the stream. The output is a 1 when the pattern is detected and 0 otherwise. Show the state diagram and state table. Do not draw the circuit

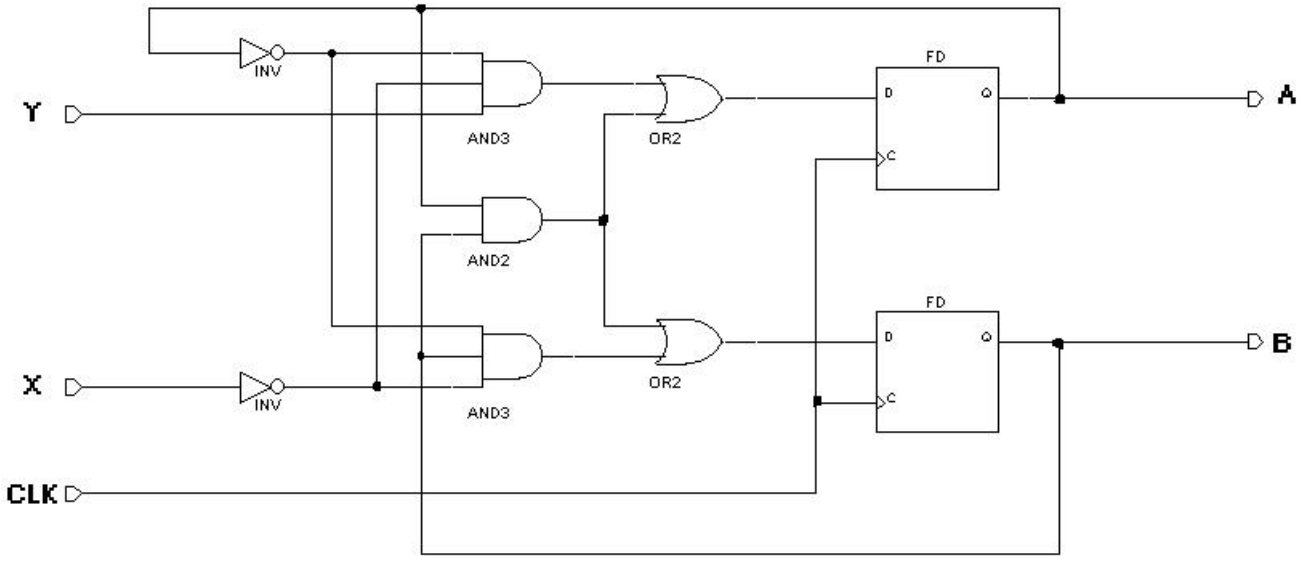
14. Design a 3-bit shift register that implements the following table using 4-to-1 multiplexers and D-type flip-flops

S1	S0	Synchronous Operation
0	0	Load
0	1	Shift right
1	0	No change
1	1	Shift left

15. What is the maximum frequency of the circuit in problem 2 if the propagation delay of the multiplexer is 5nS, the proagation delay of the flip-flop is 7nS, flip-flop hold time is 2nS and the flip-flop setup time is 4nS?

16. Design a counter that counts in the following sequence: 1000, 0100, 0010, 0001, 1100, 0110, 0011, 1001, 1010, 0101, 1110, 0111, 1011, 1101, 1111, 0000. Show the state diagram and state table.

17. Derive the state table and state diagram of the circuit below.



18. Design a 3-bit multi-function register using D-type flip-flops, Multiplexers, and the minimum amount of additional combinational logic. The multi-function register has operations listed in the following table:

S1	***S0***	***Operation***
0	0	Load Inputs
0	1	Shift Left
1	0	Clear
1	1	Complement if greater than 3

19. Design a 3-bit multi-function register using D-type flip-flops, Multiplexers, and the minimum amount of additional combinational logic. The multi-function register has operations listed in the following table:

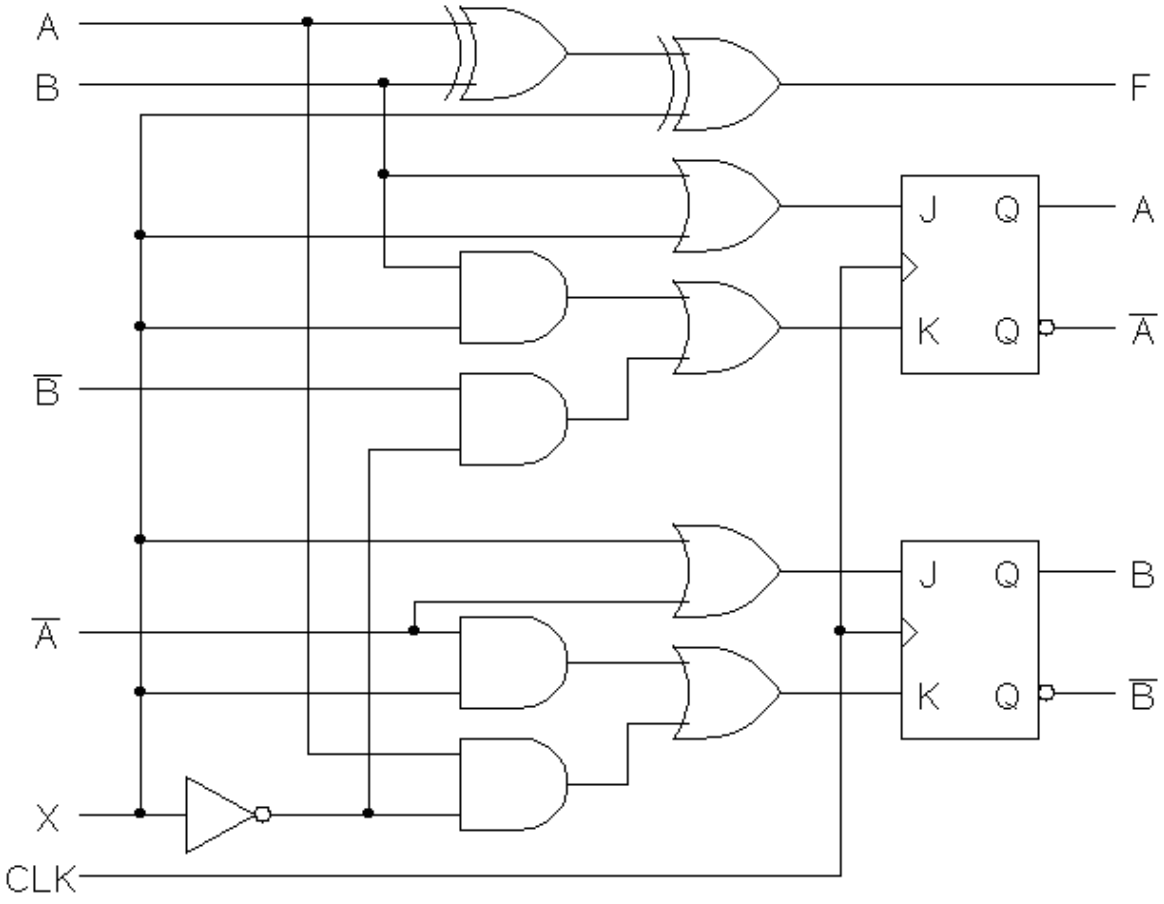
S1	***S0***	***Operation***
0	0	Load Complemented Inputs
0	1	Shift Right
1	0	Set to 1's
1	1	Complement if input is less than 4

20. A Barrel shift register is a special register where the data in the register can rotate a specified number of bits. As bits are rotated, the most significant bits are rotated back into the least significant bits of the register. Design a 3-bit barrel shift register that implements the following operations:

```
  S1   S0 | Synchronous Operation
======+=========================
```

0 0 | No Change
0 1 | Rotate left one
1 0 | Rotate left two
1 1 | Load external data

21. Using the circuit below and the sequential analysis procedure draw the state diagram and state table. Note: I do not expect you to know how JK flip-flops work.



22. Design a Moore model circuit (where the output can change only on a positive clock edge) that detects the bit pattern 1100110 (least significant bit first). This pattern can be detected even if it overlaps. Use a D-type flip-flop for the output detection bit (goes 1 when the pattern is detected, 0 otherwise). Show a state table and state diagram. Do NOT draw a circuit.

23. Design a sequential circuit to convert a word into its 2's complement. The word is sent into the sequential circuit in a serial stream least significant bit first. The output stream is the 2's complement also least significant bit first. There is a synchronization signal to reset the sequential circuit called RESET that will go to 1 for at least one clock cycle. When RESET goes to 0, the first bit of the word is ready at the input of the circuit. The circuit is a Mealy model. Use D-type flip-flops and the minimum amount of additional combinational logic.