CSE 463M: Digital Integrated Circuit Design and Architecture
Homework #3

The homework set is the same for both CSE 463M and 563M student:

This homework requires you to use the Cadence Tutorial from the class website along with the help form TA. Follow the tutorial in order to solve the problems bellow and get further familiar with Cadence.

Here is transistor data for AMI Semiconductor 0.5 micron process:

	NMOS	PMOS
K'	$120\mu A/V^2$	$-40\mu A/V^2$
V_{to}	0.8V	-0.8V
γ	0.6	0.6
λ	$0.06V^{-1}$	$0.06V^{-1}$
Xd (Under Diffusion)	6nm	6nm
NSUB	$1.3x10^{16}$ cm^{-3}	$4.8x10^{16}$ cm^{-3}
C_{ox}	1.1×10^{-3} F/m^2	1.1×10^{-3} F/m^2
$C_{gdo}=C_{gso}$	6.6×10^{-12} F/m	6.6×10^{-12} F/m
C_j	2.8×10^{-4} F/m^2	3×10^{-4} F/m^2
C_{jsw}	1.7×10^{-10} F/m	2.6×10^{-10} F/m

Problem set:

1. Design a CMOS inverter that will operate from a 5V power supply (i.e. Vdd=5V) and it has a threshold (V_{th}) of 3V. Show all hand calculations that allowed you to design this circuit. Use the data in the table above for your calculations.

2. Design the CMOS inverter from problem 1 in Cadence. Print the schematic of the inverter. Simulate the static behavior of the inverter. Make sure that your SPICE simulation indicates that the threshold of the inverter is 3V. If this is not the case, readjust the aspect ratios of your NMOS and/or PMOS in order to have the desired threshold of 3V. Print your SPICE simulation and indicate your Vth on the plot.

3. Using SPICE and the calculator within the SPICE simulator to compute V_{IL} and V_{IH}. Plot the results and indicate your results on the plot.

4. Draw the layout of the inverter in Cadence. Print the layout of the device.