Digital Integrated Circuit Design and Architecture
(CSE463M)

Final Examination - Take Home
Due by email Monday (Dec 16th) 11AM

Your Name: _____

You need to show all your work in order to get the full credit. There are seven problems in this exam. State any assumptions you believe necessary for solution of problems. Please submit all Cadance output you deem relevant.

1. (22 pts) Consider the function $\mathbf{Y=(A\bar{B}+C)\bar{G}+E\bar{F}}$

   a. Implement this function using CMOS logic and draw the circuit in Cadence. Assume that all signals and their respective inverse signals are available to the designer. Print the schematic.

   b. All transistors in the circuit have W/L = 1.8um/1.8um,

   $\mathbf{V_{T0,n}=0.8V}$, $\mathbf{V_{T0,p}=-0.9V}$, $\mathbf{k'_{T0,n}=110\frac{\mu A}{V^2}}$, $\mathbf{k'_{T0,p}=38\frac{\mu A}{V^2}}$. What is the value of the logic threshold when all inputs are connected to V_{th}? Show all hand calculations and simulate the results in Spice. Print the Spice simulation.

   c. Simulate the circuit for all possible input transitions and plot the results.

   d. What is the common Euler path for the PMOS and NMOS network of transistors? Draw the optimized stick-diagram layout.

   e. Draw the optimized layout in Cadence. Perform DRC and LVS on the layout. Print the layout of the circuit, the DRC and the LVS messages.

2. (18 pts) Design a 2 to 1 Multiplexer using CMOS Transmission Gates in Cadence.
   a. Draw the schematic in Cadence and print it.
   b. Simulate the transient behavior of the circuit for all possible combinations. Print the transient behavior.
   c. Draw the layout of the circuit. Print the layout of the circuit, the DRC and the LVS messages.

3. (15 pts) Design a 3-input CMOS NOR gate with logic threshold voltage of $V_{dd}/2$ when all inputs are connected to $V_{dd}/2$ and has a maximum fall time of 1nsec for 100fF load capacitance. Assume $K_n' = 100\mu\ A/V^2$, $K_p' = 100\mu A/V^2$, $V_{dd}=5V$, $V_{ton} = 1V$, $|V_{top}| = 1V$, $\gamma=0$ and $\lambda=0\ V^{-1}$.

4. (7 pts) Describe read/write operations of 1-cell dynamic RAM

5. (10 pts) Implement the following complex function with CMOS logic: Z=(AB+C)D. Design the CMOS circuit in Cadence using minimum size transistors. Simulate the circuit for all possible input transitions and plot the results (show all 16 possible transitions).

6. (13 pts) A piece of old (very old) CMOS equipment has 1000 interconnecting wires, each with 50 pF of capacitance (these are connections on a printed circuit board), and voltage L and H of 0V and 5V, respectively. If these interconnections switch at frequency of 50MHz, what is the power dissipation for these interconnects? If we converted to a single IC with V_{dd} = 1.8V, and 1000 interconnect wires with capacitance of 0.3pF (much smaller because the wires on an IC, rather than a printed circuit board) what would be the power dissipation for these interconnects?

7. (15 pts) An integrated circuit has been designed for operation over the V_{dd} range of 2.25V to 2.75V, and temperature from 0 degC to 75 degC. Tests of fabricated circuits show that under worst case V_{dd} and temperature as above, the circuits have maximum propagation delay of 0.9 times the maximum allowed value. In order to increase the market for these circuits they will be sold with widened specification limits for V_{dd} and temperature.
   a.) What is the limit for Vdd (the voltage at which the worst case process delay will be the maximum allowed) if temperature is kept to the present range?
   b.) What is the limit for the temperature if voltage is kept to the present range?