

# CSE 463 –Digital Integrated Circuits Design and Architecture

## Course Syllabus – Fall 2013

**Instructor:** Emir Osmanagić  
**Email:** [cse463@osmanagic.com](mailto:cse463@osmanagic.com)  
**Class:** Monday & Wednesday 5:30PM-7:00PM @ Crow 205  
**Office Hours:** by appointment  
**Grader:** Yiyi Zhang  
**Email:** [yiyi.zhang@wustl.edu](mailto:yiyi.zhang@wustl.edu)  
**Website:** <http://classes.engineering.wustl.edu/cse260/>  
**Textbook:** CMOS Digital Integrated Circuits Analysis and Design, S. M. Kang and Y. Leblebici, 2002  
**References:** Verilog HDL: A guide to digital design and synthesis, S. Palnikar, 1996.  
Basic VLSI Design, D. Pucknell and K. Eshraghian 1988.  
Fundamentals of CMOS VLSI Design, J. Uyemura, 1988  
**Prerequisites:** ESE232 (Intro to Electronic Circuits), CSE362M (Computer Architecture)

### Course Content

- ❖ MOS transistor theory
- ❖ Inverter
  - Static Characteristics
  - Switching Characteristics
  - Design
- ❖ Combinational Logic Circuits
- ❖ Sequential Logic Circuits
- ❖ Dynamic Logic Circuits
- ❖ Memories

### Goals

The course will start with an overview of the intrinsic properties of CMOS transistors and an overview of fabrication methodologies for integrated circuits. Combinational circuits will be introduced with the design of the inverter circuit. The static and dynamic properties of the inverter will be studied in detail using hand calculations and SPICE simulations. The state-of-the-art tool for designing ICs, Cadence, will be introduced and will be used to design and verify the physical layout of the inverter. Using parameters extracted from Cadence layout simulations, a Verilog model will be constructed. Other CMOS combinational and sequential digital circuits, such as NAND, NOR, SR latch, flip flop and others, will be constructed and simulated at transistor, layout and behavioral level.

### Grading

Homework	20%
Midterm#1	20%
Midterm#2	20%
Final	35%
Instructor	5%