Experiment 3: Non-Ideal Operational Amplifiers

Equivalent Circuits

The basic assumptions for an ideal operational amplifier are an infinite differential gain ($a_d$), an infinite input resistance ($R_i$), zero output resistance ($R_o$), infinite bandwidth, zero output voltage ($V_o$) when $V_+$ and $V_-$ are equal or alternatively when $V_d = V_+ - V_-$ = 0, zero input bias currents, and zero input offset voltage. Under these ideal conditions, an operational amplifier (op-amp) does not load down its input nor does the load affect the output. Under these conditions the analysis of the resulting electronic system is reduced to its simplest form. Although most op-amps approach these ideal conditions, in a number of applications it is important to understand the limitations imposed by the real behavior of op-amps.

Shown in Figure 1 are equivalent circuits for both an ideal op-amp (upper circuit) and a more realistic macromodel of an op-amp (lower circuit). The macromodel shows the additional components that approximate the non-ideal behavior of real op-amps. In modern op-amps, the differential gain is typically 100 to 300 Volts/mV. The input resistance (for small differential input voltages) can range from a few Mega ohms for bipolar input devices up to 10 Tera ohms for FET input devices (e.g. LMC6081). The output resistance is typically 50 to 100 ohms.
To account for an output voltage \( V_o \) when \( V_+ \) and \( V_- \) are equal, a common mode gain \( a_c \) and a common mode voltage, \( V_c = (V_+ + V_-)/2 \), are introduced into the circuit. Two current sources \( (I_+ \text{ and } I_-) \) represent nonzero input bias currents and a battery \( (V_{\text{offset}}) \) represents the non-zero dc offset voltage.

An often-used figure of merit for an op-amp is the common mode rejection ratio (CMRR), defined as

\[
CMRR = \left| \frac{a_d}{a_c} \right|
\]

CMRR at low frequencies is typically about 90 dB. Be aware that the common mode rejection typically degrades rapidly with increasing frequency, beginning at fairly low frequencies.

Another characteristic of real op-amps is limited frequency response and slew rate. These two effects limit the high frequency response of the amplifiers, but in different ways. Almost all op-amps have nearly flat gain up to some corner frequency. Above that frequency the gain decreases at about -6 dB/octave (or -20 dB/decade). This is the same frequency response as a simple RC low pass filter. When the input signal has a frequency higher than this corner frequency, the output will still be sinusoidal, but the gain will reduced. In addition there is a separate slew rate limitation. This is usually the result of a capacitor introduced in the design to stabilize the amplifier and make it easier to use. (Some very high speed amplifiers are available without compensation, and they can be tricky to use particularly at low closed loop gain.) The result of this capacitor is that no matter what the input to the amplifier does, the output voltage will not change faster than some limiting rate (volts/µSec). Another effect of this capacitor can be a delay from input to output following large (saturating) input signals. This results when this capacitor charges to a large voltage while the input is saturated, and then has to discharge before the output can resume tracking a normal input.

**Differential Gain**

\[
V_o = \frac{V_{\text{SAT}}}{Slope = a_d}
\]

Figure 2 – Transfer characteristic of an operational amplifier

Because the differential gain of an op-amp is so high, it is difficult to measure accurately. Referring to Figure 2, it can be seen that the differential input voltage \( (V_d) \) must be very small to obtain operation in the linear amplification region. Otherwise, the output will saturate at a voltage \( (V_{\text{SAT}}) \) somewhat less than the power supply voltage \( (V_{\text{CC}}) \). Because of this, we will use
a unity gain inverter circuit (negative feedback) with a voltage divider input as shown in Figure 3 below to measure the differential gain as a function of frequency.
If in the circuit of Figure 3, we set \((R_1 + R_2)\) much much greater than \(R_i\) or \(R_f\) and \(R_2 \ll R_1\) so that \(V_\cdot\) is small, then

\[
V_0 = -\frac{R_f}{R_i} V_S
\]  \hspace{1cm} (2)

To obtain a unity gain inverter we set \(R_f\) equal to \(R_i\) and, so as long as \(a_d\) is very large, then

\[
V_0 = -V_s
\]  \hspace{1cm} (3)

Consider now the voltage divider assuming \(I_i=0\) which results in

\[
V_\cdot = V_R \frac{R_2}{R_i + R_2}
\]  \hspace{1cm} (4)

Since the differential gain is

\[
a_d = \frac{V_0}{V_d} = \frac{V_0}{V_+ - V_-} = -\frac{V_0}{V_-}
\]  \hspace{1cm} (5)

then

\[
a_d = -\left(\frac{R_i + R_2}{R_2}\right) \frac{V_0}{V_R}
\]  \hspace{1cm} (6)

To facilitate the measurement of a high differential gain, equation (6) indicates that we should set \(R_1\) much greater than \(R_2\) and then measure \(V_0\) and \(V_R\) as functions of frequency. Most operational amplifiers have a single dominant pole so the differential gain should show a frequency dependence of the form

\[
a_d(\omega) = \frac{a_d(0)}{1 + j \frac{\omega}{\omega_0}}
\]  \hspace{1cm} (7)
where $\omega_0$ is the radian frequency of the dominant pole and $a_d(0)$ is the dc differential gain.
Common Mode Rejection Ratio (CMRR)

We will assume that $|a_d| >> 1$ and that $|a_d| >> |a_c|$. Under these assumptions, it is straightforward to verify in the circuit of Figure 4 that

$$V_0 = a_d(V_S - V_0) + a_c\left(\frac{V_S + V_0}{2}\right). \tag{8}$$

Therefore, since $a_dV_0 >> V_0$ and $V_0 = V_S$, it is easily shown that

$$CMRR = \frac{a_d}{a_c} = \frac{V_S}{V_0 - V_S}. \tag{9}$$

Since over most of its usable frequency range the common mode gain of an op-amp is much less than the differential gain, $V_0 - V_S$ will be much less than $V_S$ and may be difficult to measure with an oscilloscope. An AC voltmeter that can be isolated from circuit ground is more useful here for measuring the value of $V_0 - V_S$. Also, to obtain a readily measurable value, it will be necessary to use a rather large value for $V_S$. An input signal $V_S = 20$ V peak-to-peak is recommended so long as the output is distortion free.

Slew Rate

Slew rate determines the maximum frequency at which rated output can be delivered without significant distortion. It is easily measured with the simple inverter circuit shown in Figure 5 by applying a square-wave input signal ($V_S$) and examining the output voltage ($V_0$) on an oscilloscope. Typically, the applied $V_S$ is large enough to drive the output between $-V_{SAT}$ and $+V_{SAT}$ so that the resulting $V_o(t)$ looks as shown in Figure 6.

$$V_0 = a_d(V_S - V_0) + a_c\left(\frac{V_S + V_0}{2}\right).$$

Figure 4 - Circuit for measuring common mode rejection ratio

Figure 5 – Circuit for measuring slew rate
From the oscilloscope waveform as in Figure 6, the Slew Rate (SR) is given by

\[ SR = \frac{\Delta V}{\Delta t} \]  

(10)

The maximum time rate of change of a signal that can be reproduced by an opamp is limited by the slew rate, so slew rate can be used to determine the frequency range over which a sine wave can be amplified without serious distortion. For example, assume that the output voltage is given by

\[ v_o(t) = V_p \sin(2\pi f t) \]  

(11)

The slope is

\[ \frac{dv_o(t)}{dt} = 2\pi f V_p \cos(2\pi f t) \]  

(12)

The maximum value of the slope occurs at time \( t=0 \), so

\[ \frac{dv_o(0)}{dt} = 2\pi f V_p \]  

(13)

and

\[ f_{\text{max}} = \frac{SR}{2\pi V_p} \]  

(14)

where \( f_{\text{max}} \) is the maximum frequency at which the op-amp can reproduce a sine wave with peak value of \( V_p \) without serious distortion.
Offset Voltage and Bias Currents

Offset Voltage Measurement

To measure the dc offset voltage ($V_{\text{offset}}$) of an op-amp we set $R_1$ and $R_2$, indicated in Figure 7, to zero, that is, short circuits. Under these conditions

$$V_- = V_o \text{ and } V_+ = V_{\text{offset}}$$

so

$$V_{\text{offset}} = V_o \frac{1 + a_d - \frac{a_c}{2}}{\left( a_d + \frac{a_c}{2} \right)}$$

and, since $a_d >> 1 >> a_c$, then

$$V_{\text{offset}} = V_0$$

Therefore, from equation (17) we see that with the inverting input connected directly to the output and the non-inverting input connected to circuit common ground, the output will have a non-zero value which is the “dc offset voltage”.

Figure 7 – Circuit for measuring dc offset voltage and bias currents
I+ Bias Current Measurement

To measure $I_+$ of the op-amp we set $R_2 = 0$ in Figure 7. The result is

$$I_+ = -\frac{V_0 \left( 1 + a_d - \frac{a_c}{2} \right) - V_{\text{offset}} \left( a_d + \frac{a_c}{2} \right)}{R_1 \left( a_d + \frac{a_c}{2} \right)}$$  (18)

Choosing $R_1$ relatively large, say $1\,M\Omega$, and again assuming that $a_d \gg 1 \gg a_c$, we get:

$$I_+ \approx -\frac{V_0 - V_{\text{offset}}}{R_1}$$  (19)

I- Bias Current Measurement

To measure $I_-$ set $R_1$ to zero. In a manner similar to that above we find:

$$I_- \approx \frac{V_0 - V_{\text{offset}}}{R_2}$$  (20)

Notice the difference in minus signs between equations (19) and (20).
Experiment:

Equipment List

1 Printed Circuit Board with Two 741 Operational Amplifiers
1 Printed Circuit Board Fixture
1 Screwdriver
1 Solderless Wiring Fixture
   Assorted Resistors

Procedure

The printed circuit board with two 741 operational amplifiers should be mounted in the printed circuit board fixture with the components of the board on the same side as the banana plug jacks of the fixture. With the components facing you, jack 1 will be on your far left and jack 22 on your far right. Notice that jacks 1, 4, 18, and 22 have BNC as well as banana plug connectors. In this experiment the operational amplifier on the left is used for the open loop gain measurements while the one on the right is used for all subsequent measurements.
1. **Open Loop Gain Measurement.** Connect the circuit as indicated in Figure 8 using the left-hand portion of the printed circuit board. Notice that all resistors for this part of the experiment are on the printed circuit board. With zero volts across the inputs, adjust the 10k potentiometer to keep the amplifier at zero dc offset. *Measure the magnitude and phase* of the input voltage at jack 9 and the output voltage at jack 5 as a function of frequency. Note that from Equation (6)

\[ a_d = -1001 \frac{V_5}{V_9}. \]

- Keep the output voltage as large as is practical without distortion (about 20 V\(_{p-p}\)).
- Consider using the 10x Probe to observe \( V_R \) to keep from loading down this node.
- Vary the frequency over the range from 1 Hz to 10 kHz. **Be sure to take enough data to observe all interesting features, especially in the 1 to 20 Hz range.**
- Make your measurements as accurately as possible. You should be able to get at least two significant digits even from an oscilloscope display. Consider using the HP Digital Multimeter (DMM) for to measure \( V_R \) for better accuracy.

![Figure 8 - Open Loop Gain Measurement Circuit](image)

2. **Common Mode Rejection Ratio (CMRR).** To measure the common mode rejection ratio, construct the circuit of Figure 9. This employs the operational amplifier on the right hand side of the board.

- The CMRR depends strongly on the setting of the null adjust potentiometer, so before taking data, set the null adjustment potentiometer for zero dc offset.
- Display both the input signal \( (V_{15}) \) and the output signal \( (V_{17}) \) on the oscilloscope.
- With the input signal \( (V_{15}) \) about 20 V peak-to-peak and the output signal \( (V_{17}) \) relatively free of distortion when observed on the scope, measure the magnitude and phase of the output voltage \( V_{17} \) compared to the input voltage \( V_{15} \) over the frequency range from 5 Hz to 10 KHz.
- Use the HP DMM to get accurate readings of \( (V_{17} - V_{15}) \). Measuring each separately and then taking the difference using the math function on the scope does not work well!
3. Slew Rate. Construct the inverting amplifier circuit shown in Figure 10. Note that the 1k and 10k resistors are external. Apply a square wave of about 1 V peak-to-peak at 10Hz to the input of the circuit.

- Measure and record the rise time of the input signal.
- With this input measure and record the output rise time and voltage.
- Measure the delay time between the input and output at both the rising and falling edges.
- Repeat these measurements at 100 Hz, 1 KHz, 10 KHz, 100 KHz and 1 MHz.
- Is there any change in slew rate or delay time with frequency?
4. Overload Recovery Time. Use the previous circuit in Figure 10 and apply a 1 KHz square wave. Slowly increase the amplitude until the output begins to saturate. Make certain the amplifier has saturated on both the positive and negative sides of the square wave. You may have to adjust the DC offset of the function generator to get the amplifier to saturate on both polarities.

- What is the input amplitude at saturation?
- What are the saturated high and low output voltages?
- Increase the input signal to twice the value required to saturate the output. Measure the overload recovery time (delay time) between the input and output for both the rising and falling edges.
- Repeat this measurement for 100 Hz, 1 KHz, 10 KHz and 100 KHz.

5. Bias and Offset Measurements. Measure the input offset voltage and bias currents:

- With resistors 1 and 2 equal to zero in the circuit of Figure 11 examine and record the variation of the output voltage as the null adjust potentiometer is changed.
- Set the output voltage as close to zero as is possible and do not change the potentiometer during the remainder of the experiment.
- With $R_1$ equal to 1 M\(\Omega\) and $R_2$ equal to zero, record the output voltage. Calculate $I_+$. 
- With $R_1$ equal to zero and $R_2$ equal to 1 M\(\Omega\), record the output voltage. Calculate $I_-$. 

![Bias and Offset Measurement Circuit](image)

Figure 11 – Bias and Offset Measurement Circuit

Report

1. Plot on a single semi-log graph the magnitude of the differential gain, in dB, and the phase, in degrees, as a function of frequency.
   - What is the break frequency of the dominant pole for this operational amplifier?
   - What is the gain-bandwidth product?
   - Extrapolate the gain curve at high frequency to predict the unity gain bandwidth?
   - Are the gain-bandwidth product and unity gain bandwidth values equal?
   - How much uncertainty do you estimate for these measurements?
   - Are your measured results within specifications for this amplifier?
2. Plot on single semi-log graph the magnitude, in dB, and phase, in degrees, of the common mode rejection ratio (CMRR) as a function of frequency.
   • Does the approximation derived in class for the common mode rejection ratio remain valid over the entire frequency range?
   • Calculate the CMRR at 60 Hz.
   • Is your measured CMRR within the published specifications?

3. Examine the slew rate data you recorded.
   • Present your values for slew rate and discuss any frequency dependence.
   • Using the measured values of slew rate, calculate the maximum frequency at which the operational amplifier can develop a 10 V peak sine wave output.

4. Review the recovery time data you recorded.
   • Present your values for overload recovery time and discuss any frequency dependence.

5. Review the offset voltage and bias current data you recorded.
   • Over what range could the offset voltage be changed with the null adjust potentiometer?
   • What values did you obtain for the inverting and non-inverting bias currents?

6. Examine the inverting amplifier circuit in Figure 12. Assume that $R_1 = 5 \, \text{k}\Omega$ and $R_2 = 1 \, \text{M}\Omega$.
   • What is its predicted low frequency gain?
   • Based on the data presented in part 1 above and the low frequency gain of this amplifier, calculate the expected the 3 dB bandwidth of this inverting amplifier. Assume that the offset voltage and bias currents are zero and that $R_3 = 0$.
   • What useful function does $R_3$ serve in an inverter circuit?
   • What should nonzero value of $R_3$ be?

   ![Figure 12 - Half Power (-3 dB) Bandwidth Circuit](image)

References and Suggested Reading


