Experiment 6: CMOS FET Chopper Stabilized Amplifier

Fall 2009

This experiment is designed to introduce you to (1) the characteristics of complementary metal oxide semiconductor (CMOS) field effect transistors (FETs) and (2) the operation of chopper stabilized amplifiers. CMOS transistors are particularly important in electronic applications where power conservation is important, such as in pacemakers, digital watches, and hand held calculators. A CMOS device consists of a pair of n-channel and p-channel transistors configured to have essentially no power dissipation in either the ON or OFF state. Power is drawn from the main source, usually a battery or DC supply, only during the switching process. So, from a power dissipation viewpoint at low operating frequencies, CMOS devices are superior to other technologies.

Chopper stabilized amplifiers are used to stabilize DC or low frequency circuits against voltage drift due, for example, to temperature changes as well as low frequency noise sources such as 60 Hz line voltages. One common application is in optoelectronics where light is chopped mechanically, detected electrically, amplified, and demodulated electronically to evaluate the properties of a system. These devices are called "lock-in amplifiers".

Enhancement Mode MOSFETS

n-Channel

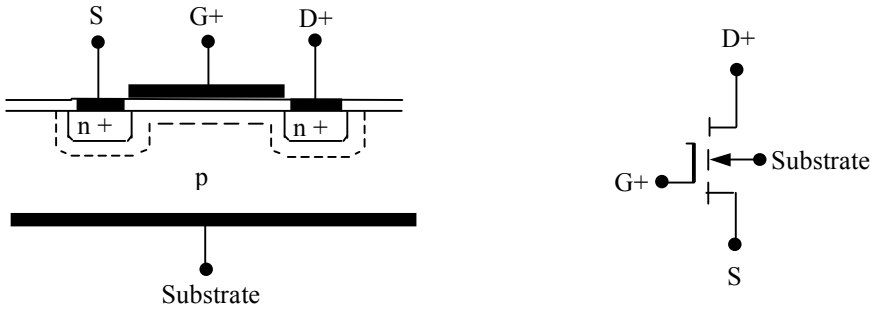


Figure 1 –Cross-section of n-channel enhancement mode MOSFET with circuit symbol

A cross-sectional schematic of an n-channel enhancement mode MOSFET is shown in Figure 1. The n+ regions are diffused or implanted into a p-type substrate to form source and drain regions, while a metal is deposited on a thermally grown oxide to form the gate region. With zero voltage on the gate, a space charge region isolates the source and the drain and no current flows through the transistor. To maintain isolation the substrate should be connected to the source. When a positive voltage is applied from gate to source, majority carrier holes are repelled and minority carrier electrons from the n+ wells are attracted to the surface of the semiconductor beneath the gate oxide layer. This is referred to as an n-channel and provides a current path from drain to source. When the positive gate to source voltage is increased, more minority carrier electrons are attracted to the channel and the drain to source current increases. This results in an output characteristic for the transistor similar to that shown in Figure 2.

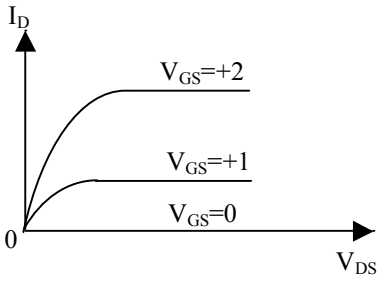


Figure 2 – Output characteristics of an n-channel device

p-Channel

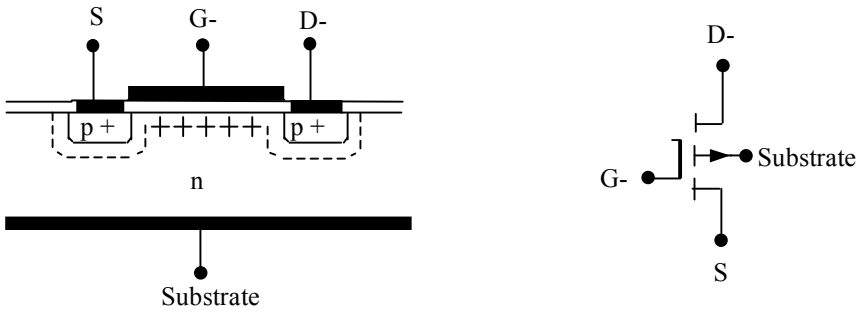


Figure 3 - Cross-section of p-channel enhancement mode MOSFET with circuit symbol

The p-channel transistor operates in a complementary fashion to the n-channel device. As indicated in Figure 3, a negative gate to source voltage repels majority carrier electrons and attracts minority carrier holes from the p+ wells in the n-type substrate to the surface region below the gate. This provides a conductive path from source to drain and allows current to flow from drain to source. A more negative voltage increases the extent of the conducting channel and allows more current to flow. Again, isolation is maintained by connecting the substrate to the source.

CMOS Inverter

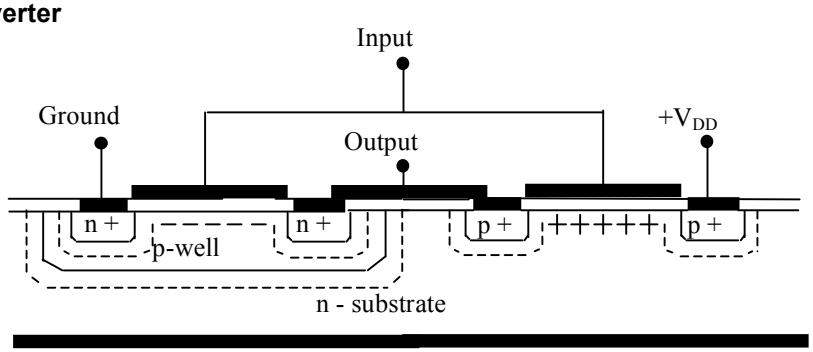
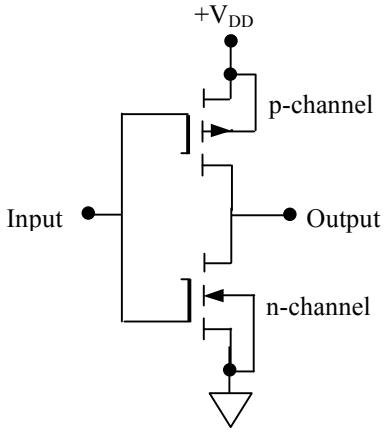


Figure 4 – Schematic cross-section of a CMOS inverter



$V_{out} = V_{OL} \approx 0V$ for $V_{in} > V_{IH} \geq V_{DD}/2$

$V_{out} = V_{OH} \approx V_{DD}$ for $V_{in} < V_{IL} \leq V_{DD}/2$

Figure 5 – Circuit symbol of a CMOS inverter

As indicated in Figure 4, the CMOS inverter combines n-channel and p-channel FET transistors on the same substrate by diffusing or ion implanting a p-well into an n-substrate. Metallization is then used to connect the gates together for the input and to connect the drains together for the output. The resulting circuit symbol is shown in Figure 5. When the input is at ground potential there is zero voltage from gate to source in the n-channel device so it is ***OFF***. With this input the p-channel gate is negative relative to the p-channel source so the p-channel device is ***ON***. This connects the output to $+V_{DD}$, and so with the input at zero the output is $+V_{DD}$. In complementary fashion, when the input is at $+V_{DD}$, the n-channel gate is positive relative to the source while the p-channel gate is at 0V relative to the p-channel source and so the output is connected to ground and the output equals 0V. Note that the switching occurs over a small range of V_{in} near $V_{DD}/2$, so the device can also be used as an amplifier if properly biased.

Bilateral Switch

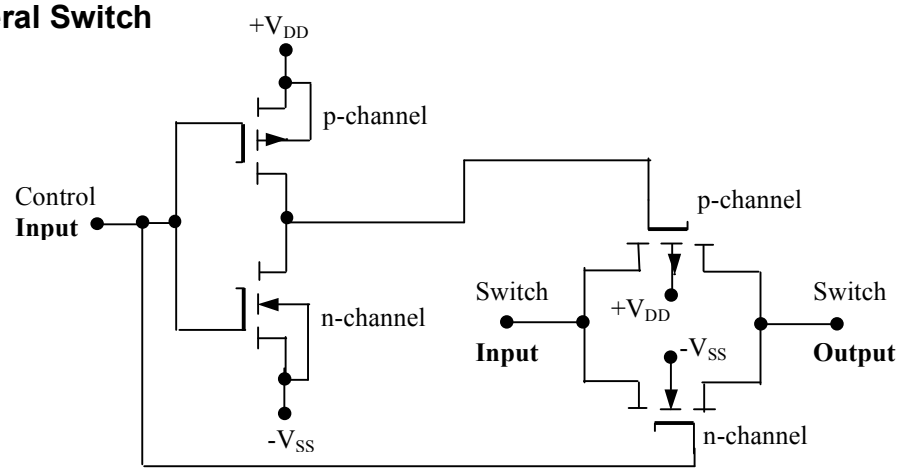


Figure 6 – Circuit diagram of a CMOS bilateral switch

The operation of a CMOS bilateral switch can be ascertained from Figure 6. When the input to the control inverter is $+V_{DD,}$ the inverter output is $-V_{SS}$. This sets the gate of the p-channel device of the switch to $-V_{SS,}$ which turns it ***ON***. At the same time the $+V_{DD}$ at the control input is applied to the gate of the n-channel device, turning it ***ON***. So a $+V_{DD}$ control input turns both switch devices ***ON***. On the other hand when the control input is $-V_{SS,}$ the inverter output is $+V_{DD}$, which is applied to the gate of the p-channel device in the switch and so turns it ***OFF***. At the same time the $-V_{SS}$ at the control input is applied to the gate of the switch

n-channel transistor, which turns it ***OFF***. So a $-V_{SS}$ at the control input turns both switches ***OFF***. In this experiment, this switch will be used as a modulator-demodulator.

Chopper Stabilized Amplifier

In this experiment we will use CMOS inverters and switches to construct a chopper stabilized amplifier, useful for amplifying DC and very low frequency signals. The input signal will first be modulated with bilateral switches which are controlled by an oscillator made with a pair of CMOS inverters. This modulated signal will then be amplified by an inverter. The amplified signal will then be demodulated by other switches controlled by the same oscillator as the modulator. The demodulated signal will then be low pass filtered to obtain an amplified version of the input signal.

Modulation

To understand the modulation process, assume that we have a low frequency signal v(t) with frequency components (Fourier transform) V(jω). As indicated in Figure 7 we assume that the highest frequency component in the signal is ω_m.

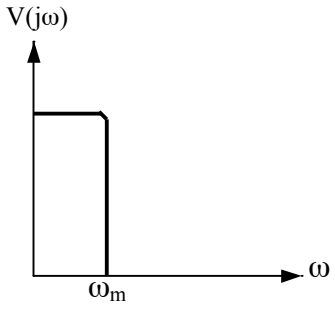


Figure 7 – Fourier transform of signal v(t)

The effect of the pulse amplitude modulation (PAM) is to multiply the signal v(t) by a square wave that alternates between +1 and –1 at the radian frequency $\omega_c = 2\pi f_c$. See Reference 2, Section 8.5, page 601. The Fourier representation of this modulating signal is

$$S(t) = 2\sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\left(\frac{n\pi}{2}\right)} \cos(n\omega_c t) \qquad (1)$$

The modulated signal is then the product of the initial signal v(t) and equation (1) which gives

$$v_m(t) = 2v(t)\sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\left(\frac{n\pi}{2}\right)} \cos(n\omega_c t) \qquad (2)$$

The product of each frequency component of v(t) and each frequency component of S(t) gives terms of the type

$$2\cos(\omega t)\cos(n\omega_c t) = \cos[(n\omega_c + \omega)t] + \cos[(n\omega_c - \omega)t] \quad . \tag{3}$$

So the Fourier transform of the modulated signal is as indicated in Figure 8.

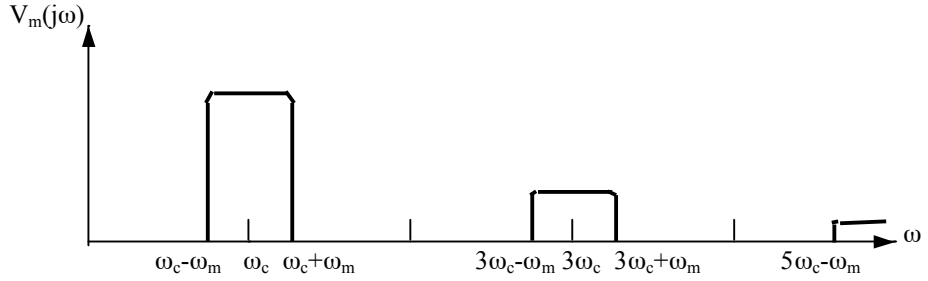


Figure 8 – Fourier transform of modulated signal $v_m(t)$

Demodulation

The modulated signal $v_m(t)$ given by equation (2) is then amplified by some factor A and then demodulated. In the synchronous demodulation process, the amplified signal is again multiplied by equation (1) to obtain

$$v_d(t) = 4Av(t)\sum_{n=1}^{\infty}\frac{\sin\left(\frac{n\pi}{2}\right)}{\left(\frac{n\pi}{2}\right)}\cos(n\omega_c t)\sum_{m=1}^{\infty}\frac{\sin\left(\frac{m\pi}{2}\right)}{\left(\frac{m\pi}{2}\right)}\cos(m\omega_c t) \tag{4}$$

The Fourier transform for this demodulated signal is shown in Figure 9.

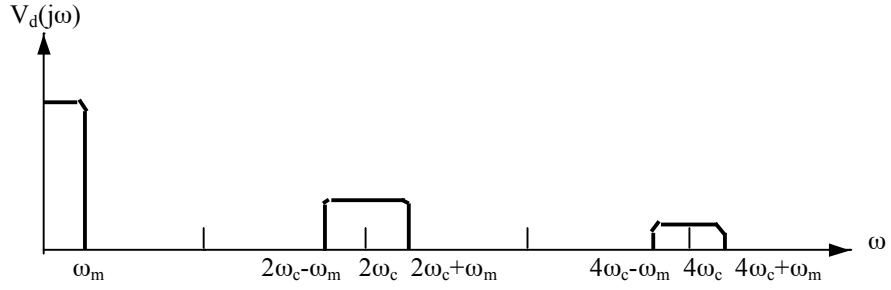


Figure 9 – Fourier transform of demodulated signal $v_d(t)$

To recover the original signal in amplified form, the demodulated signal is applied to a low-pass filter with a cut-off frequency somewhat above ω_m but less than $2\omega_c-\omega_m$.

Experiment:

Equipment List

1 Printed Circuit Board with a CD4007 Dual Complementary Pair plus Inverter and a CD4066 Quad Bilateral Switch
1 Printed Circuit Board Fixture
1 Solderless Wiring Fixture
1 100 Ω Resistor

Procedure

Two general purpose CMOS integrated circuits are used in this experiment: the CD 4007 and the CD 4066. The CD4007 consists of a dual complementary pair FETs and a FET inverter. These are indicated by the inverter symbols in Figure 10. The CD4066 has four transmission gates and associated drivers. These are shown as switches (Sw.) A, B, C, and D in Figure 10. This printed circuit board in several configurations will be used to perform this experiment.

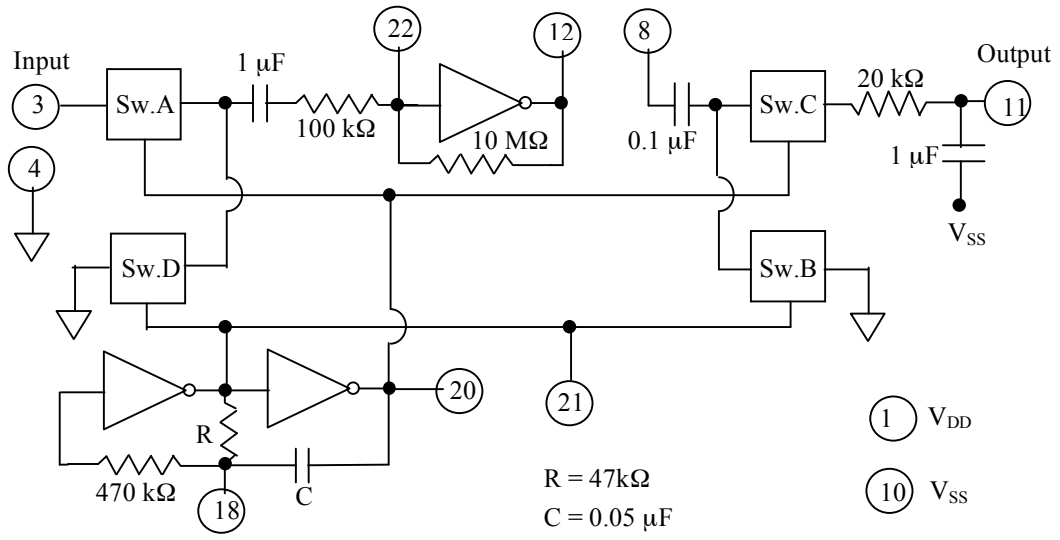


Figure 10 - CMOS Printed Circuit Board Diagram. Caution: keep |VDD| + |VSS| < 18 V.

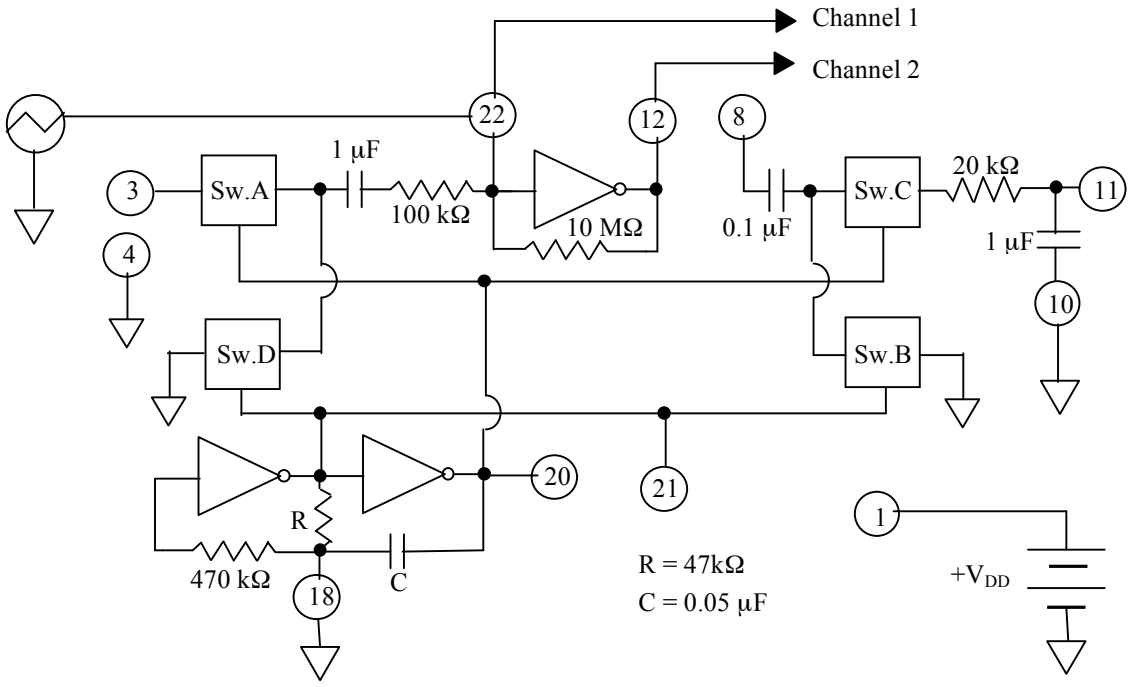


Figure 11 - Transfer Characteristic Measurement Circuit

1. Inverter Voltage Transfer Characteristic (VTC) - Connect the printed circuit board as shown in Figure 11. Set V_{DD} = 5 V. Set the function generator to triangular wave at a frequency of about 100 Hz. Adjust the peak-to-peak output from the function generator to equal +VDD, the DC power supply voltage and set the function generator DC offset to +VDD/2. Observe and record the input and output voltage waveforms for the inverter. Use X-Y format on the scope to obtain the Inverter VTC. Also, use cursors to find the slope (gain) of the inverter in the linear threshold region of the VTC near $V_{DD}/2$ and then copy this scope display.

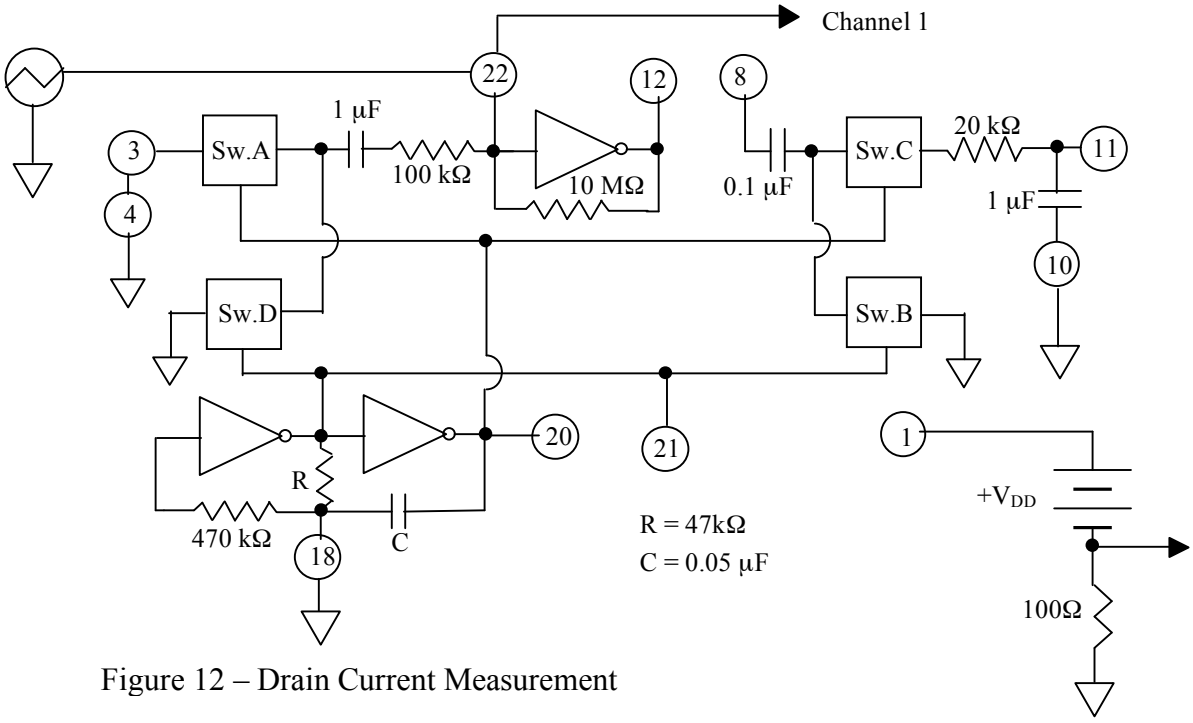


Figure 12 – Drain Current Measurement

Channel 2

2. Drain Current Measurement (Drain Current vs. Input Voltage) - Reconnect the printed circuit board as shown in Figure 12. Record the input voltage and inverter current waveforms at VDD values of +3.5 (if possible), +5, and +7.5 V DC. (Note: if the currents are too small to measure with the 100 ohm resistor, a larger value can be used!) Also, use X-Y format on the scope to get the characteristic.

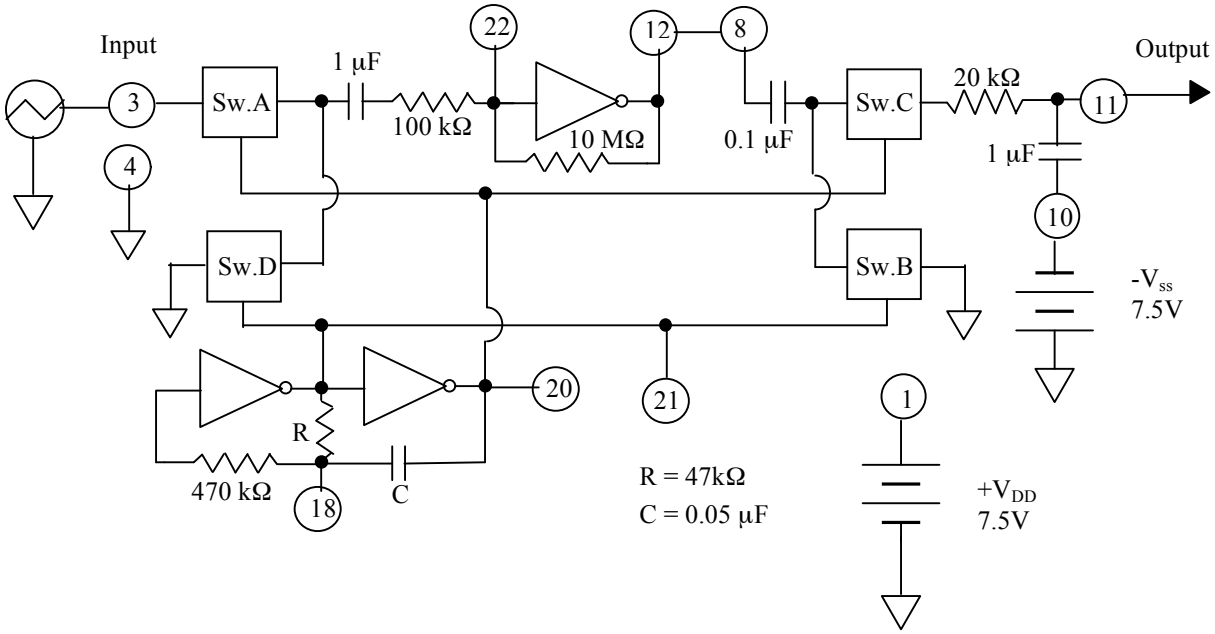


Figure 13 - Chopper Amplifier Circuit

3. Chopper Amplifier - In this part of the experiment, the CD 4007 and CD 4066 are used as elements of a chopper amplifier. Reconnect the printed circuit board as indicated in Figure 13. Referring to Figure 13, the various functions of this circuit can be determined. The two inverters on the bottom left of Figure 13 act as an oscillator which generates about a 200 Hz quasi-square wave and its complement. These square waves drive the switches, with switches A and D functioning as a single-pole, double-throw switch on the input, and switches C and B performing the same function on the output. The other inverter at the top of Figure 13 is used as an AC Amplifier. In operation, an input signal is square wave modulated by the input switches, amplified by the ac amplifier, and demodulated by the output switches. The 20 kΩ, 1 μF low pass filter minimizes the high frequency ripple in the output.

(a) Oscillator Operation and AC Amplifier Bias - First, apply the DC power only (V_{DD} = 7.5 V and V_{SS} = -7.5 V) with jack 3 grounded (no function generator input) and check the operation of the oscillator by looking at the two square wave control signals at jacks 20 and 21. They should be complementary. Then check the DC bias on the ac amplifier at jack 22. It should be within a volt or so of ground. Also, see if the output on jack 11 is zero when the input on jack 3 is grounded. Copy the waveforms at jacks 18, 20, and 21.

(b) AC Amplifier Response to Pulse Modulated Signals - Disconnect the jumper from jacks 8 and 12 and display the input at jack 3 and output at jack 12 of the AC Amplifier on the scope. For DC inputs on jack 3 of +0.5V, +0.2V, -0.2V and -0.5V, copy the scope waveforms.

(c) Chopper Amplifier DC Transfer Characteristic – Reconnect the jumper between jacks 8 and 12. Measure the transfer characteristic (DC gain) of the chopper amplifier by applying DC voltages between about -2 V and +2 V to the input on jack 3 and measuring the output at jack 11. This can be done manually using a potentiometer on the 5 VDC power supply. Be sure to take sufficient data to determine the linear and nonlinear ranges of the transfer characteristic. To reduce data taking time, try using the function generator to provide a very low frequency (0.1 Hz) triangle signal with 0V offset. For example, a $4V_{p-p}$ setting will give outputs on jack 3 associated with +2V and –2V, respectively.

(d) Chopper Amplifier Frequency Response - Apply a sinusoidal signal of 0.1 V_{p-p} with zero offset voltage to the input and measure the gain of the entire system from 0.1 to 300 Hz. If the output voltage on jack 11 is saturated (clipped), use an attenuator to reduce the input signal level. Take sufficient data to make a Bode plot (gain vs. frequency) for the entire system, paying special attention to the 0.1 to 5 Hz range and the region near the frequency of the oscillator.

Report

1. Inverter Voltage Transfer Characteristics (VTC) - Present the input and output waveforms recorded for V_{DD} = +5V. Also present VTC recorded using the X-Y format on the scope. Using the definitions given in Reference 1, Figure 10.5, page 957, estimate the values of for V_{OH}, V_{OL}, V_{IL}, and V_{IH} from the VTC and calculate the noise margins (NM_H and NM_L) for this inverter. With no input, what would you expect the output of the inverter to be considering the 10 MΩ bias resistor? What affect, if any, does the 10 MΩ bias resistor have on the Inverter VTC?

2. Drain Current - On the same graph plot values of drain current vs. input voltage for VDD values of 3.5, 5, and 7.5 V.

3. Chopper Amplifier Results

(a) Oscillator Operation and AC Amplifier Bias – Present the scope displays recorded for the oscillator in part 3 (a) above and comment on these results. Also, what was the DC bias measured at jack 22 for the AC Amplifier (Inverter)?

(b) AC Amplifier Response to Pulse Modulated Signals – Present the waveforms taken for the AC Amplifier in response to DC inputs. Discuss and explain the salient features of this response.

(c) Chopper Amplifier DC Transfer Characteristic - Plot or present the DC transfer characteristic of the chopper amplifier. Discuss and explain the salient features of this characteristic. Was the output of the chopper amplifier what you expected?

(d) Chopper Amplifier Frequency Response - Make a Bode plot (gain versus frequency) of the

Chopper Amplifier from the data taken in part 3 (d) above. Comment on the bandwidth of the chopper amplifier and the gain near the oscillator frequency.

4. Chopper Amplifier Gain Analysis - Referring to Figure 13, derive an equivalent circuit for the portion of the printed circuit board between jacks 12 and 22. See Problem 4.114 on 374 page of Reference 1. Now label the voltage at the left end of the 100 kΩ resistor as V_I and the voltage at jack 12 as V_O and calculate the gain V_I/V_O. What affect does the 100 kΩ resistor have on the AC Amplifier gain? What is the function of the 10 MΩ resistor? Using the expression for the small signal, low frequency gain of the AC Amplifier, comment on the agreement between this and the two experimental gain determinations.

5. Oscillation Frequency Analysis - Show theoretically that the oscillation period at jack 20 is approximately independent of the 470 kΩ and is proportional to RC. Assume the *ON* resistance (r_{DS}) of the FETs is << R. Indicate the proportionality factor and calculate the expected value of the oscillation period.

6. Chopper Amplifier Bandwidth Analysis - Experimentally, the -3 dB point of the chopper amplifier system was below 2 Hz even though the -3 dB point of the output filter is $(1/2\pi RC) = [1/2\pi(20\ k\Omega)(1\ \mu F) = 8$ Hz. Explain why these are different.

References

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