JEE2600 Schematic Tutorial using the

Xilinx Student Edition ISE 6.3i

This page is a general tutorial for entering a schematic and running a simulation using your Xilinx Student Edition 6.3i software. To work through this tutorial on your own PC, you must:
(1) Install the Xilinx software that came with the textbook. Be sure to follow the installation instructions that are provided with the CDs and first verify this software is compatible with your machine. I am using WindowsXP with service pack 2 and seems to work okay.
(2) You must also download and install Xilinx's ModelSim tool. The file for this tool is over 90 megbytes and it can be downloaded from http://www.xilinx.com/ise/mxe2/license.htm. Be sure to install the **starter** version, not the FULL version. You have to obtain a license for the starter version but it is free.

You can also use the CEC computer lab (Windows machines) to access the Xilinx tools but the Xilinx tools there are an earlier version. I suspect you'll be able to follow this tutorial using the tools in the CEC lab but some of the menus and steps will differ.

After installation Start the Project Navigator. You may be prompted to download an updated version of Projector Navigator but I would skip this update.

Be sure to make frequent saves of your files as you work this tutorial.
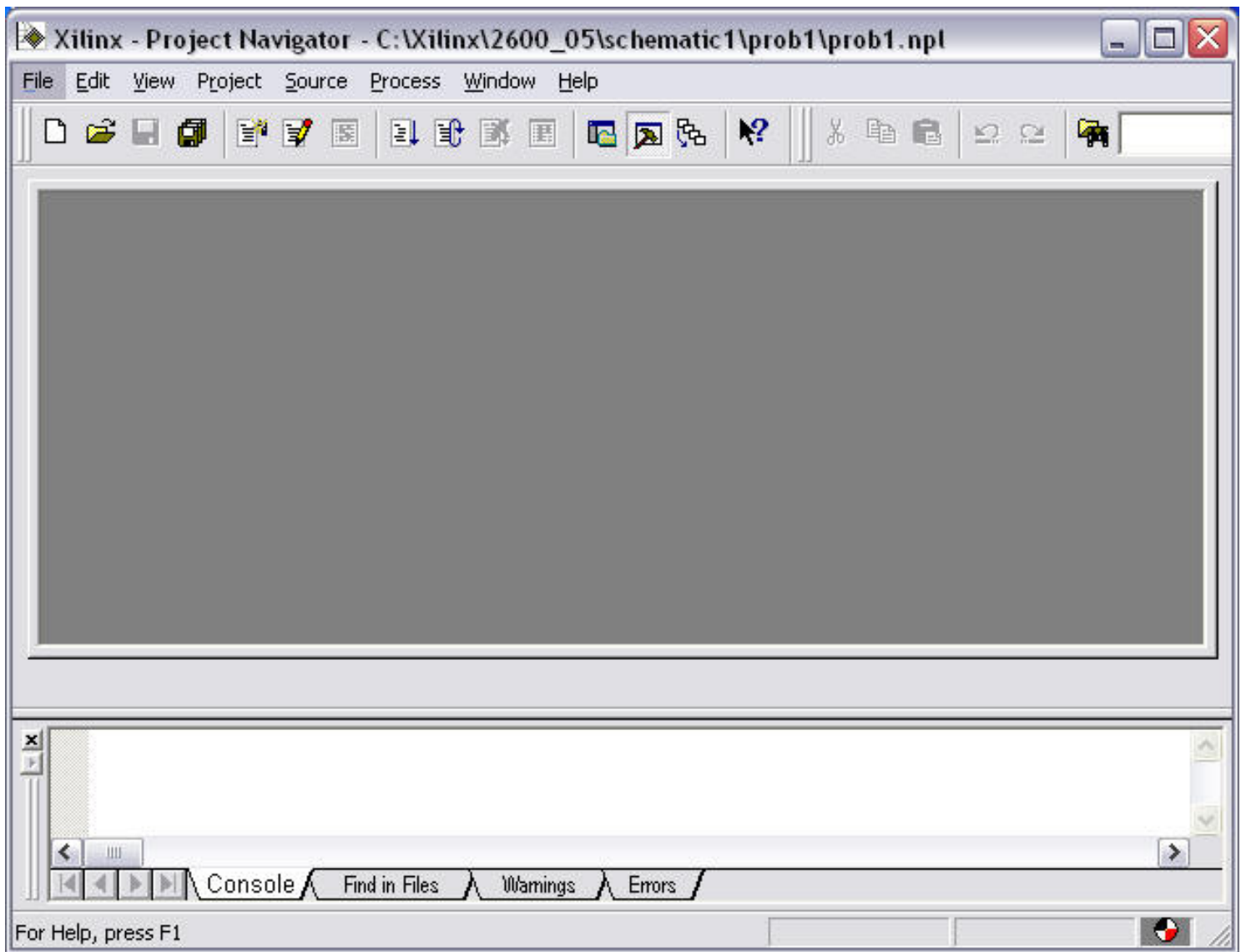
Go under **File**, and select **New Project ...**

New Project

Enter a Name and Location for the Project

Project Name:

tutorial1

Project Location:

C:\Xilinx\2600_05\schematic1\tutorial1   ...

Select the type of Top-Level module for the Project

Top-Level Module Type:

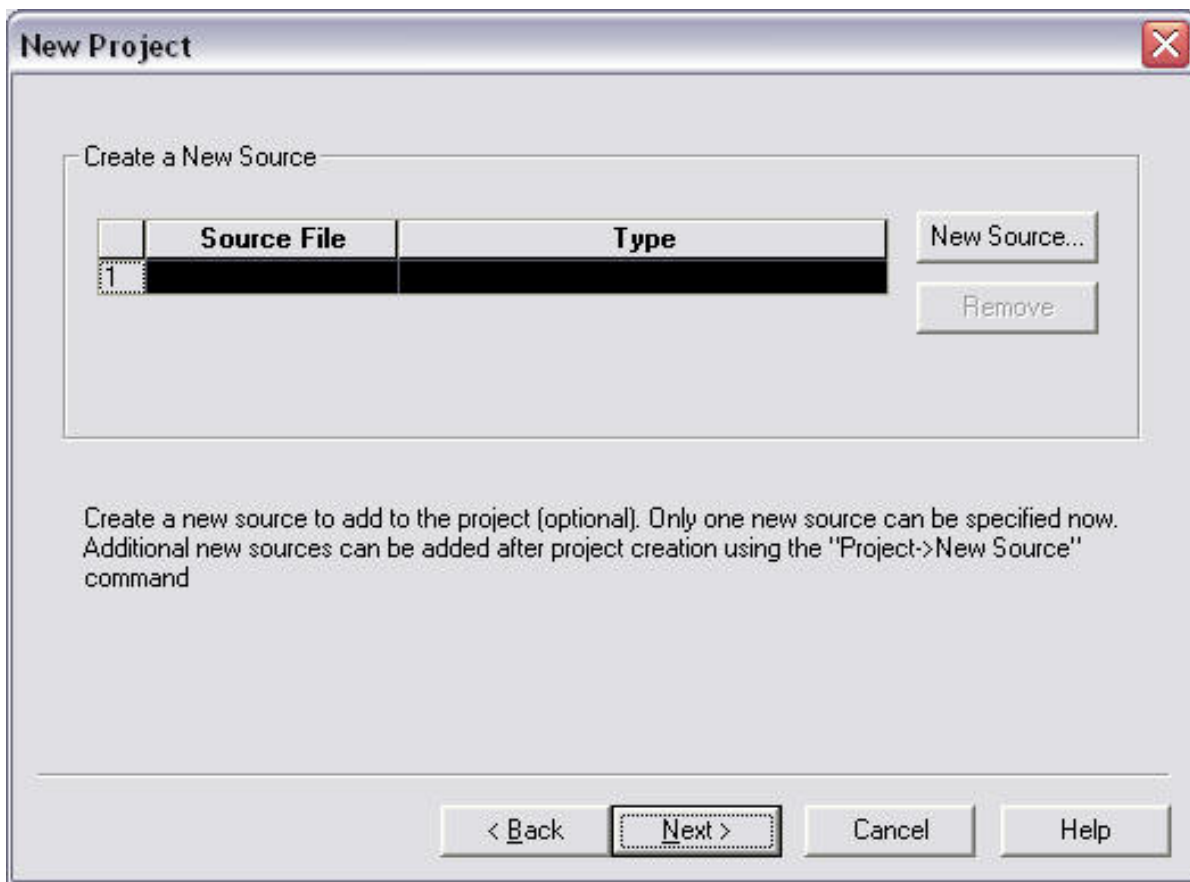Schematic

< Back   Next >   Cancel   Help

I called the project tutorial1 and established a project location. Be sure to select **Schematic** for the Module Type. Click Next

New Project

Select the Device and Design Flow for the Project

Property Name	Value
Device Family	Virtex
Device	xcv50
Package	bg256
Speed Grade	-4
Top-Level Module Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	Modelsim
Generated Simulation Language	VHDL

< Back   Next >   Cancel   Help

Select the values as shown above if possible. Be sure to select Modelsim. Click next.
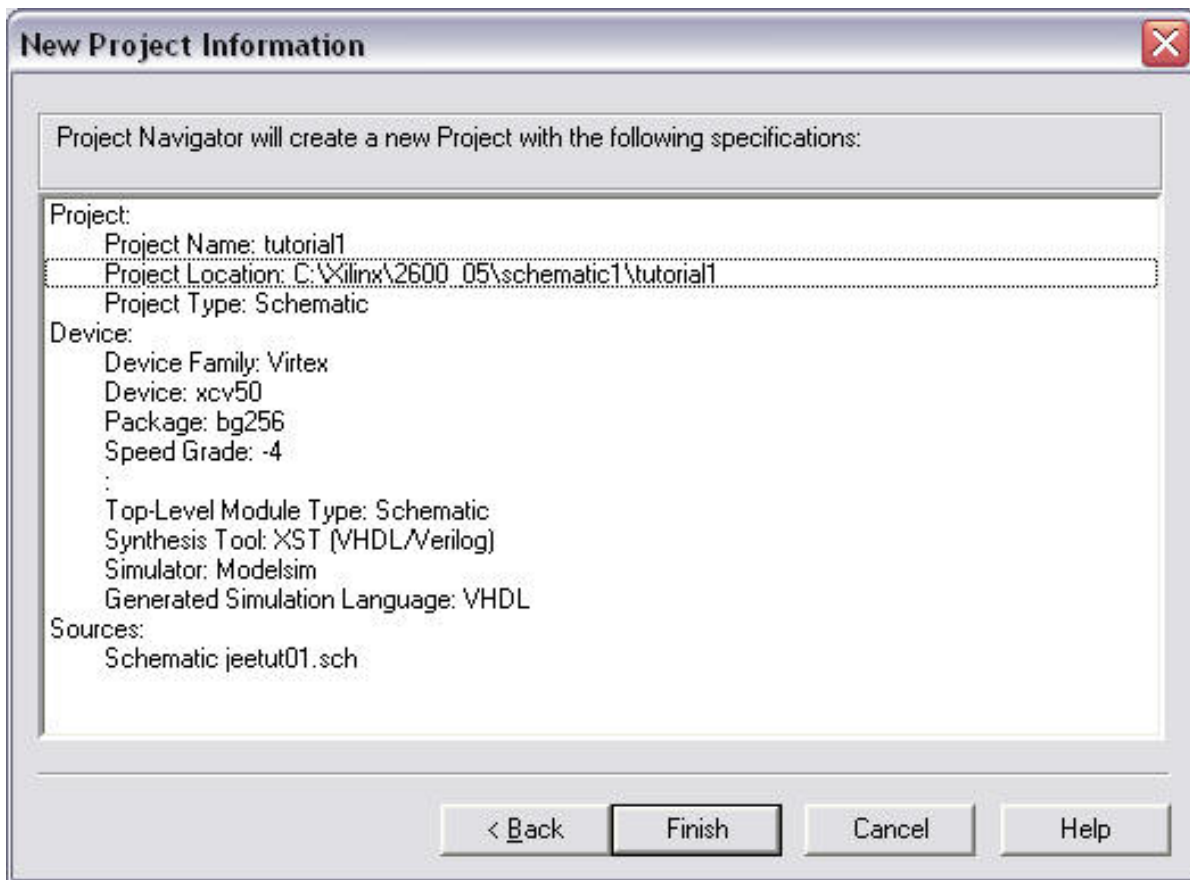

Click the **New Souce...** button.
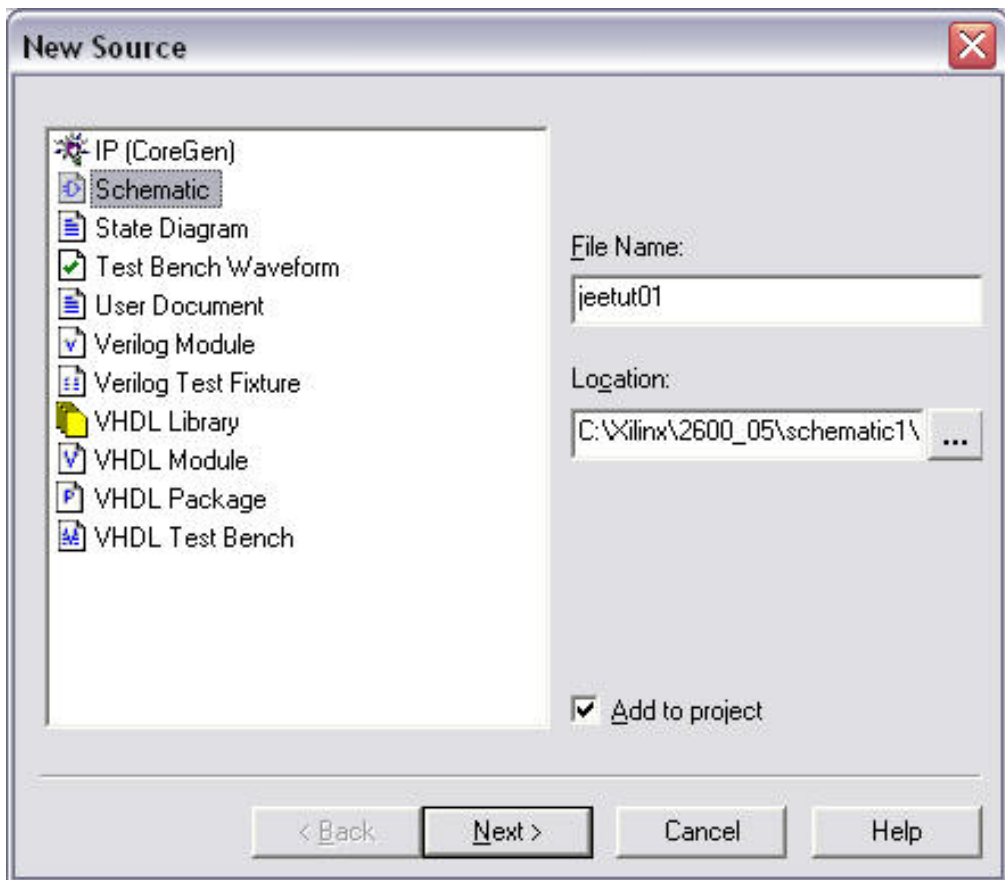
Use file name jeetut01. Leave the location at your default. Highlight the Schematic icon and click next.
The next menu will be **New Source Information**. Click Finish.
The next menu will return you to **Create a New Source**. Click next.
The next menu will be **Add Existing Sources**. Click next.

New Project Information

Project Navigator will create a new Project with the following specifications:

Project:
      Project Name: tutorial1
      Project Location: C:\Xilinx\2600_05\schematic1\tutorial1
      Project Type: Schematic
Device:
      Device Family: Virtex
      Device: xcv50
      Package: bg256
      Speed Grade: -4
      :
      Top-Level Module Type: Schematic
      Synthesis Tool: XST (VHDL/Verilog)
      Simulator: Modelsim
      Generated Simulation Language: VHDL
Sources:
      Schematic jeetut01.sch

< Back   Finish   Cancel   Help

You should get a menu similar to the above. Click finish.
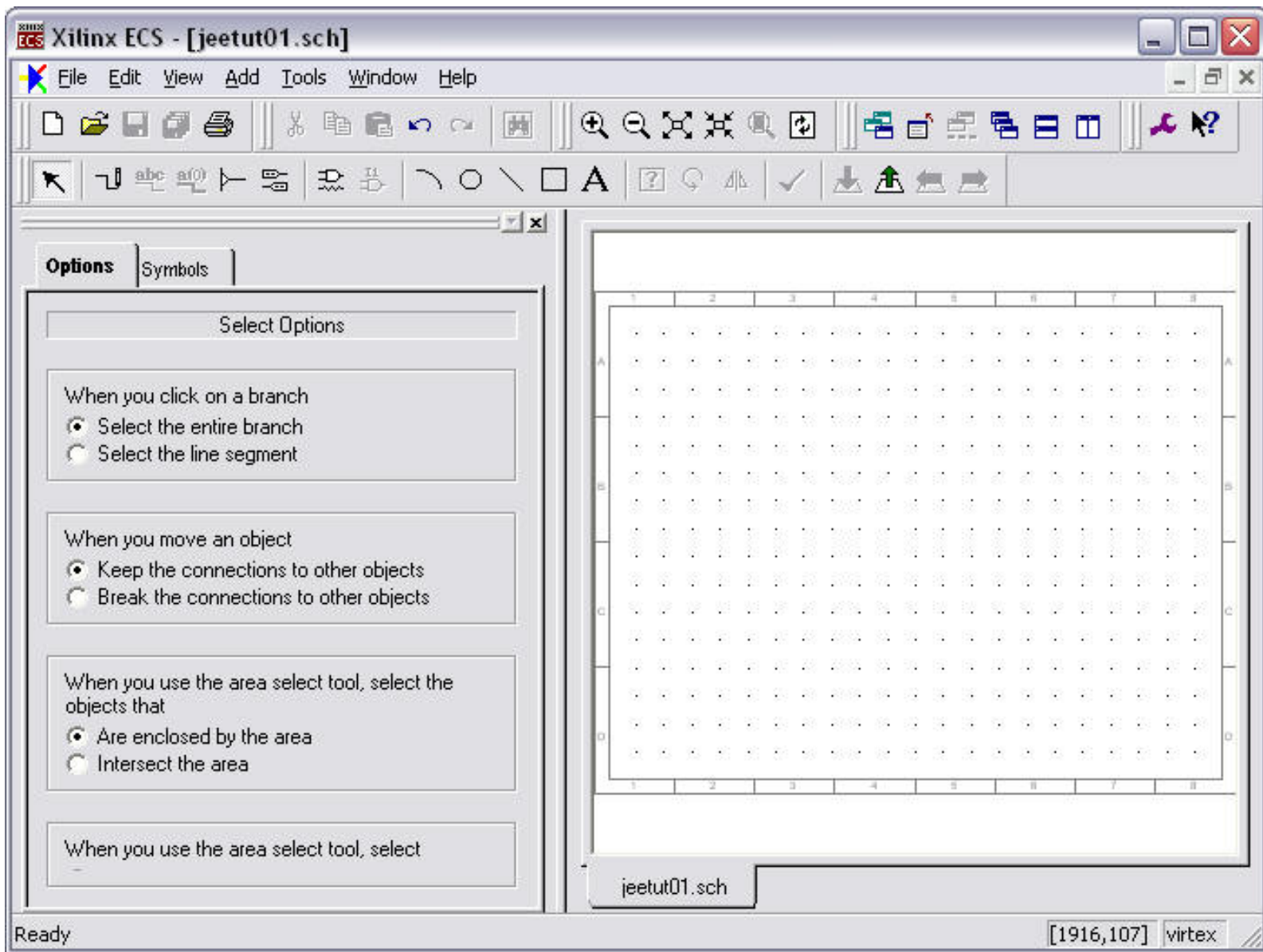
The Xilinx ESE tool should appear similar to the above which will allow you to enter your schematic. You will have to zoom in when you enter your schematic so you can see what is happening. A few of the icons in the above menu you will be using here are:

Add Symbol - Used to select and add schematic symbols to your circuit.

Add I/O Marker - Used to identify and label inputs and outputs of your circuit

Add Wire - Used to wire your circuit.

Select - Gets you out of any of the above modes and allows you to select a particular symbol/wire on the schematic.

For the example here, we'll use an example covered in class. The following boolean expression will be drawn and then simulated:

Click the Add Symbol icon and find the **and2** (this means 2-input AND gate). Click on **and2** and then move the cursor onto the schematic (jeetut01.sch above). Drop the AND gate onto the schematic by clicking the left mouse button. Repeat

this process by adding one **inv** symbol (inverter) and one **nor2** (two input nor gate) symbol. If you add too many symbols, use the Select tool to select the unwanted symbol (left click). The right-click on the symbol and select Delete.
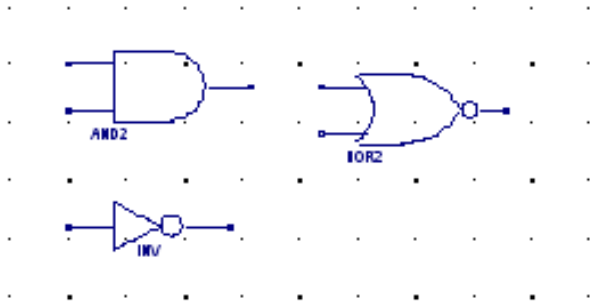
Arrange the three symbols so they are approximately located on the schematic like shown above. It is recommended that you zoom in so the inputs and outputs of the symbols can easily be seen. Next, the schematic will be wired by using the Add Wire tool.

Click the Add Wire icon. Move the cursor to the AND2 output until you see 4 dots appear. Left click and draw the line over the upper input of the NOR2. When the 4 dots appear, left click again and wire is complete. Repeat for wiring from the INV output to the other NOR2 input.

Never start a wire at the input of a gate. (You will generally get an error if you do.)
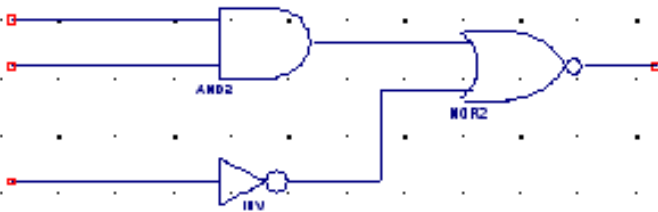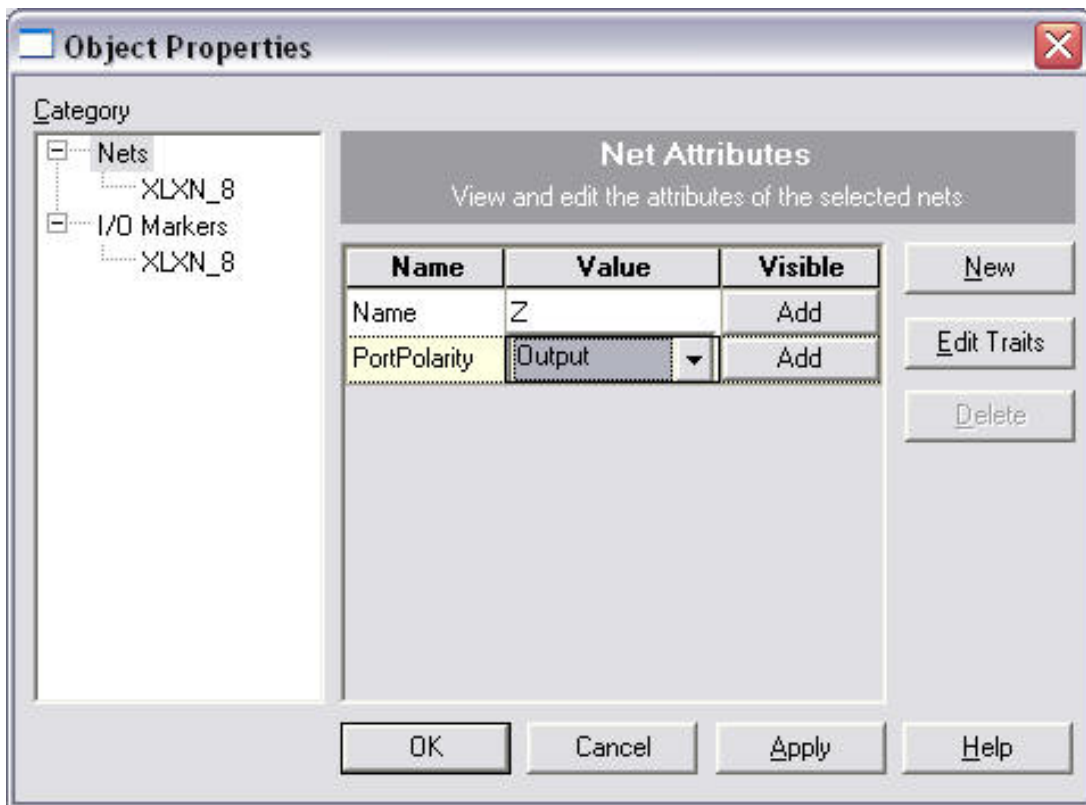

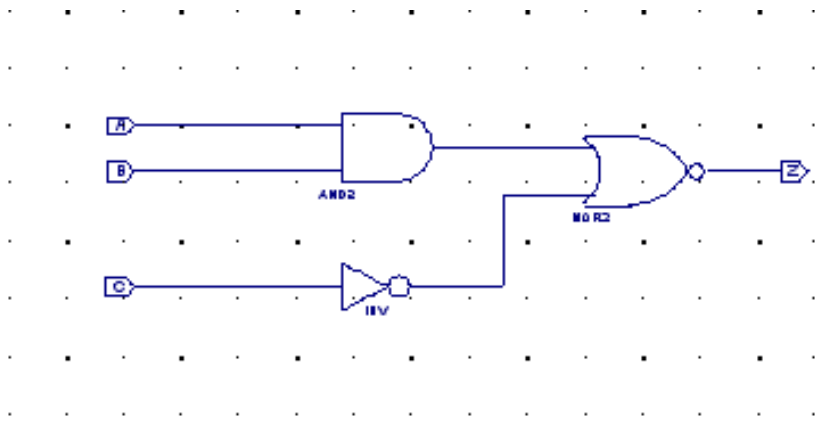Continue to add wires until your schematic looks similar to the above.

Next click on the Add I/O Marker icon. Move the cursor over the end of the wire connected to the INV input. Left click and an I/O marker will be planted. Continue this process for the remaining inputs and outputs.
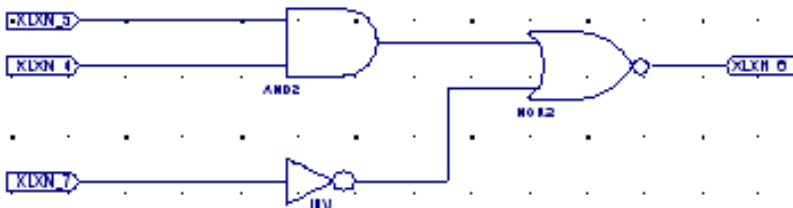

Next, double left-click on the I/O marker for the output of the circuit (the NOR2 output).

Change the Name Value to Z and the PortPolarity Value to Output. Click OK.
Repeat this process for the three inputs (A, B, C). Be sure the PortPolarity is set to Input.


Next, run the Schematic Check which is located under Tools on the ESE tool bar.

Schematic Check Errors

Error No.	Error Msg
1	No errors detected

Center

Zoom In

Zoom Out

Close

Help
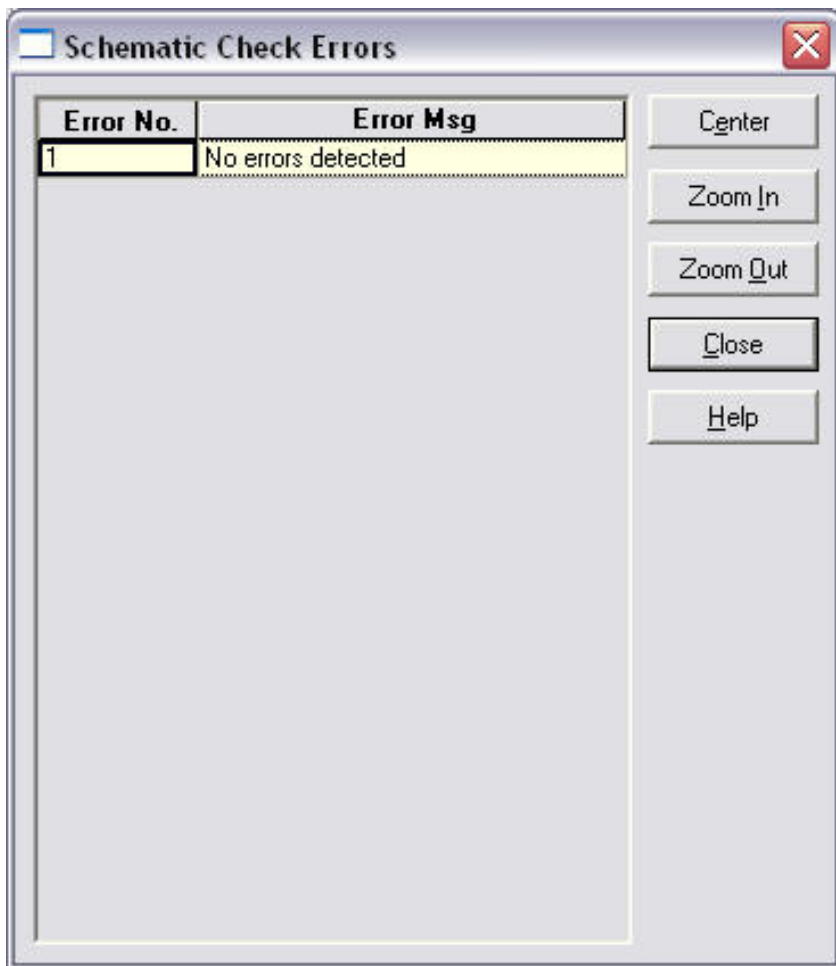
Fix schematic errors if there are any. Click the Close button for the above menu.

Click the save button for the entered schematic (Xilinx ESE page) and then you can close this application but the Xilinx Project Manager should remain open. Going back to the Xilinx Project Manager.
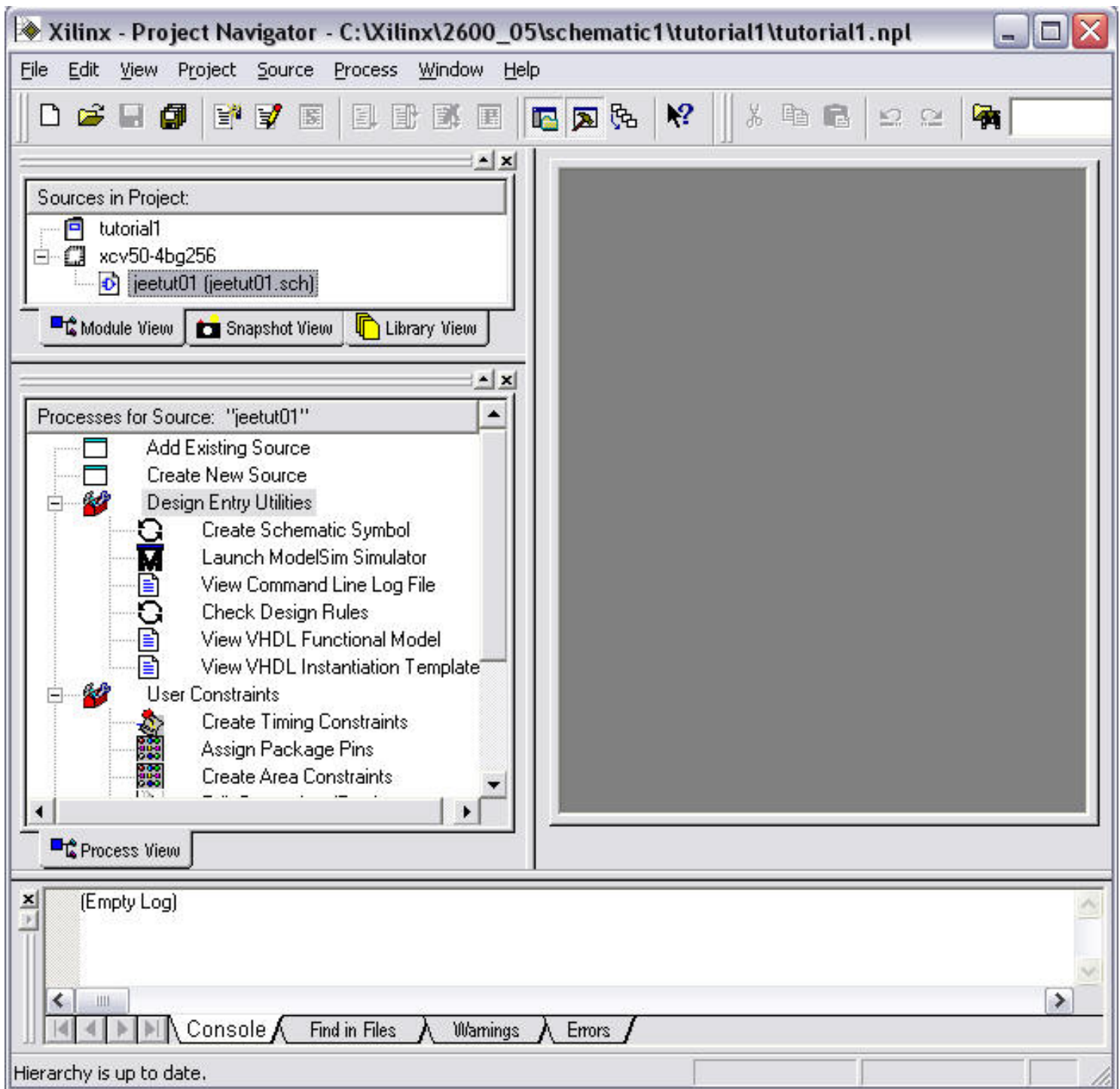
Arrange the sub-windows on this page so you can clearly see the Process View (Processes for Source: "jeetut01" shown above). Scroll down this menu until you see the Synthesize - XST. Left double click on this menu item.
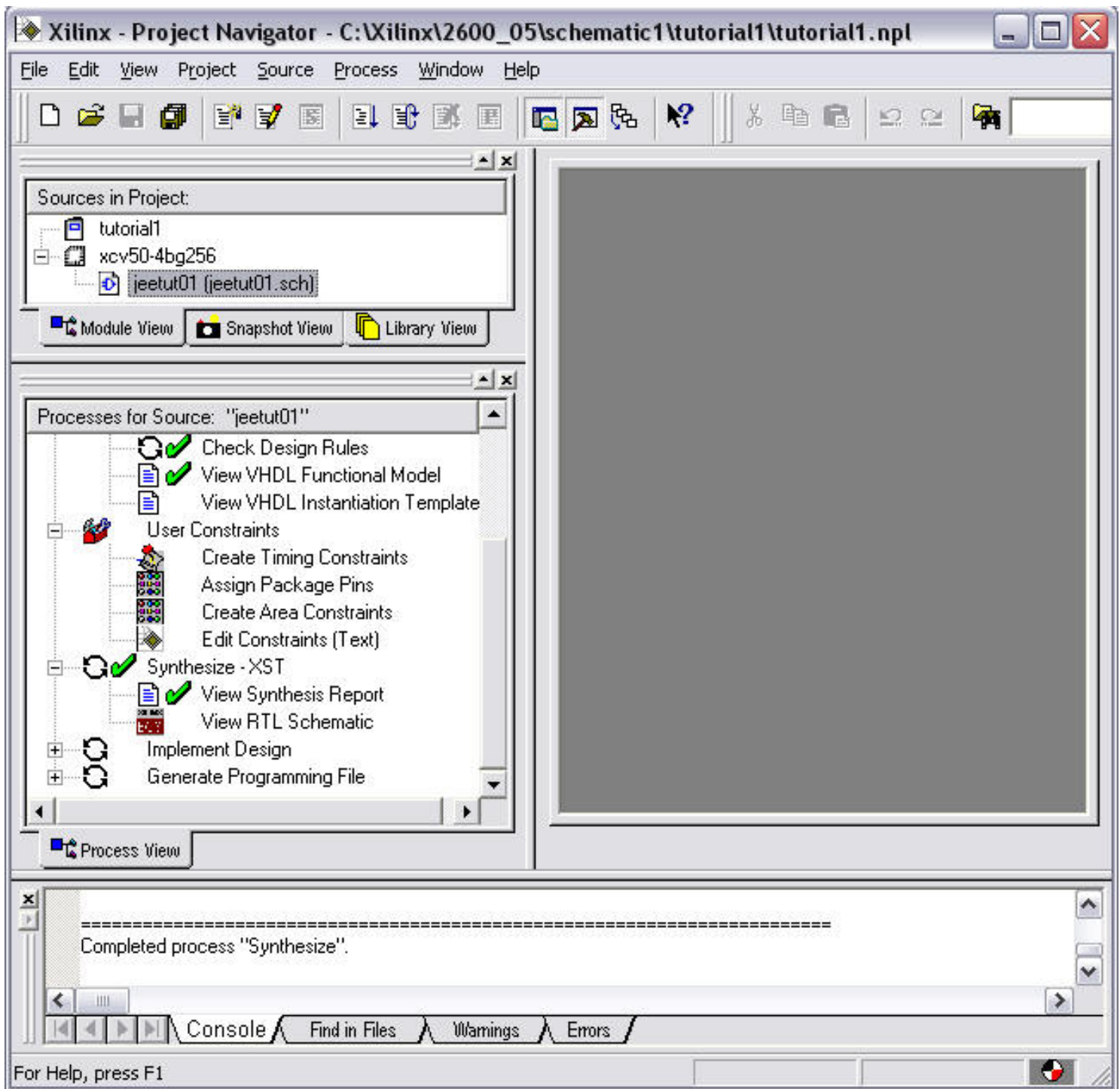
If you have the Console tab selected as shown above, you should see Completed process "Synthesize".

Next, double left-click on the Launch ModelSim Simulator menu item located within the Process View window. This activates ModelSim which allows waveforms to be generated for the inputs so the design can be tested.
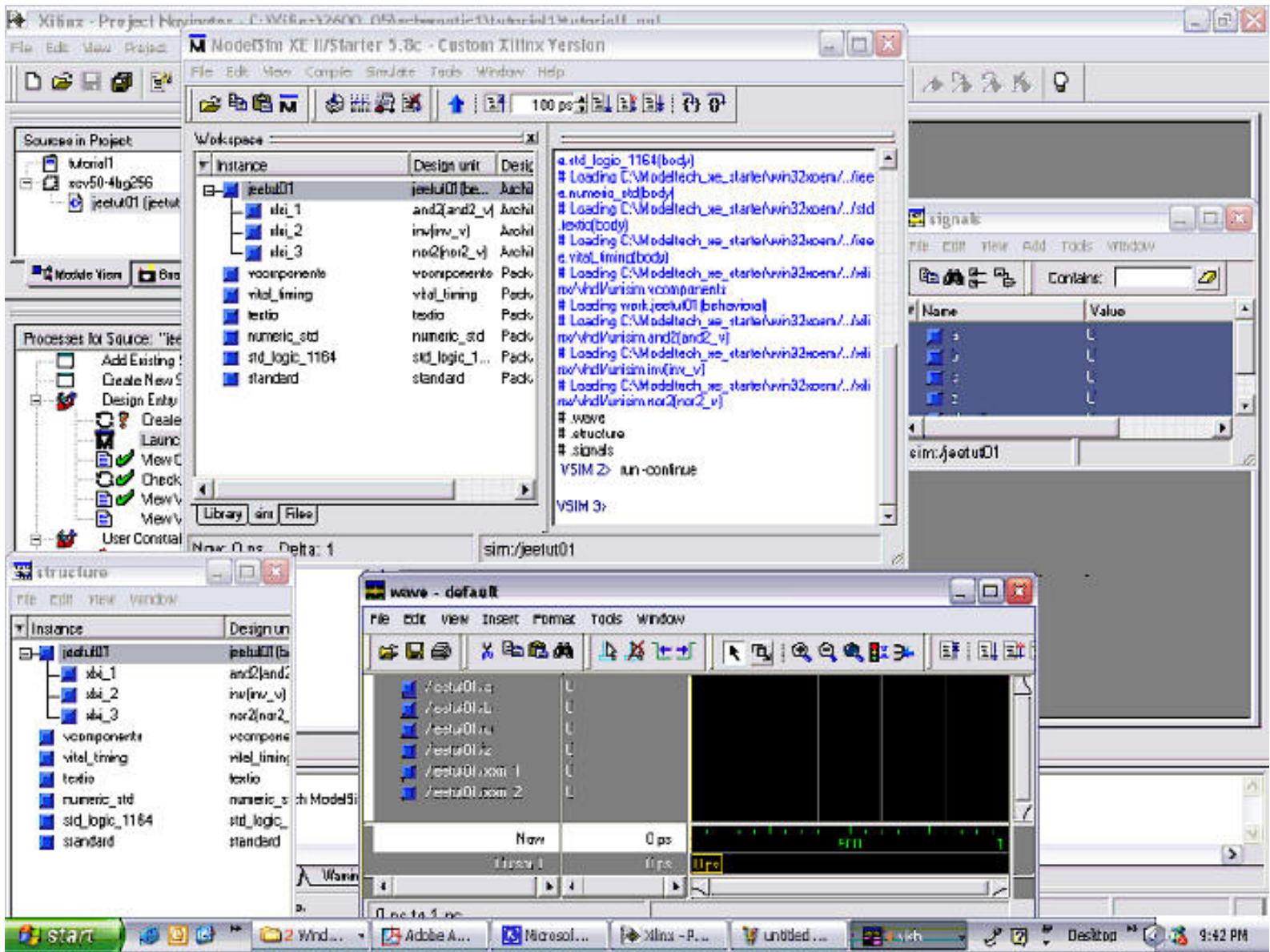
Several pages will pop-up including the Wave, Signals, and Structure.

In the wave window, highlight the two signals that are not our inputs A, B, C or output Z. These are the signals for the internal wiring from the AND2 and INV gates to the inputs of the NOR2 gate.
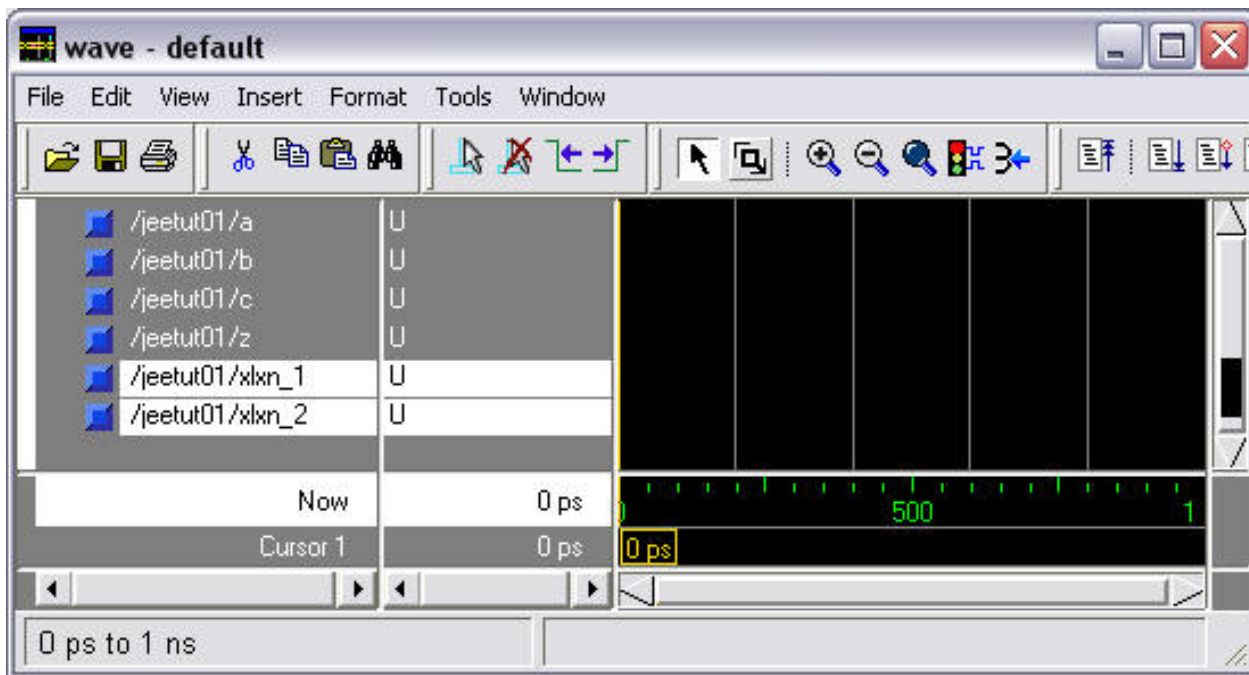
Right click on these signals and then select Delete to remove them from the generated signals.

In the "Signals" window, highlight signal A.
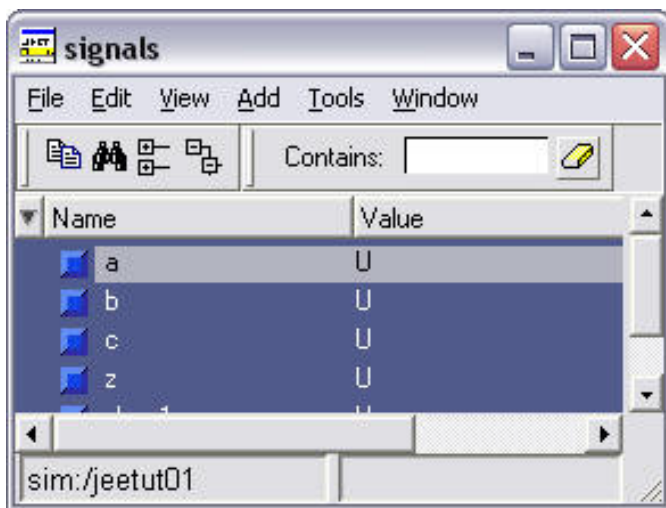
Right click on this selection and select the Force... option.

Enter a 0 (zero) for value and then click OK.
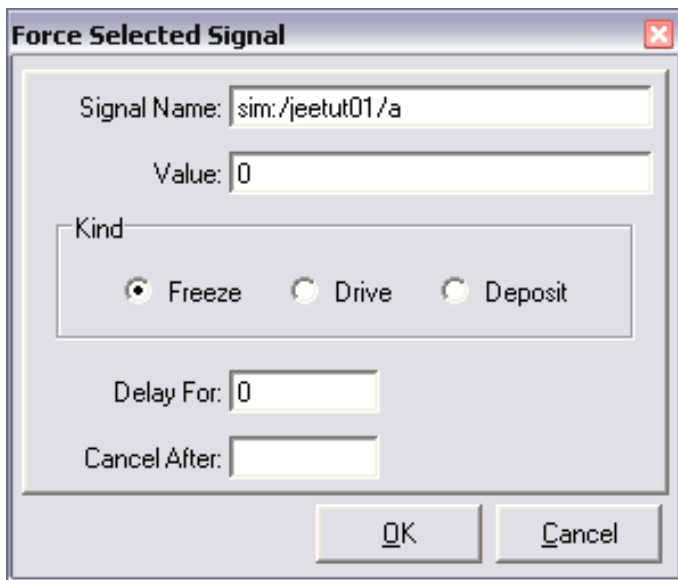Go back and look at the ModelSim command window and note the following command appears:
force -freeze sim:/jeetut01/a 0 0
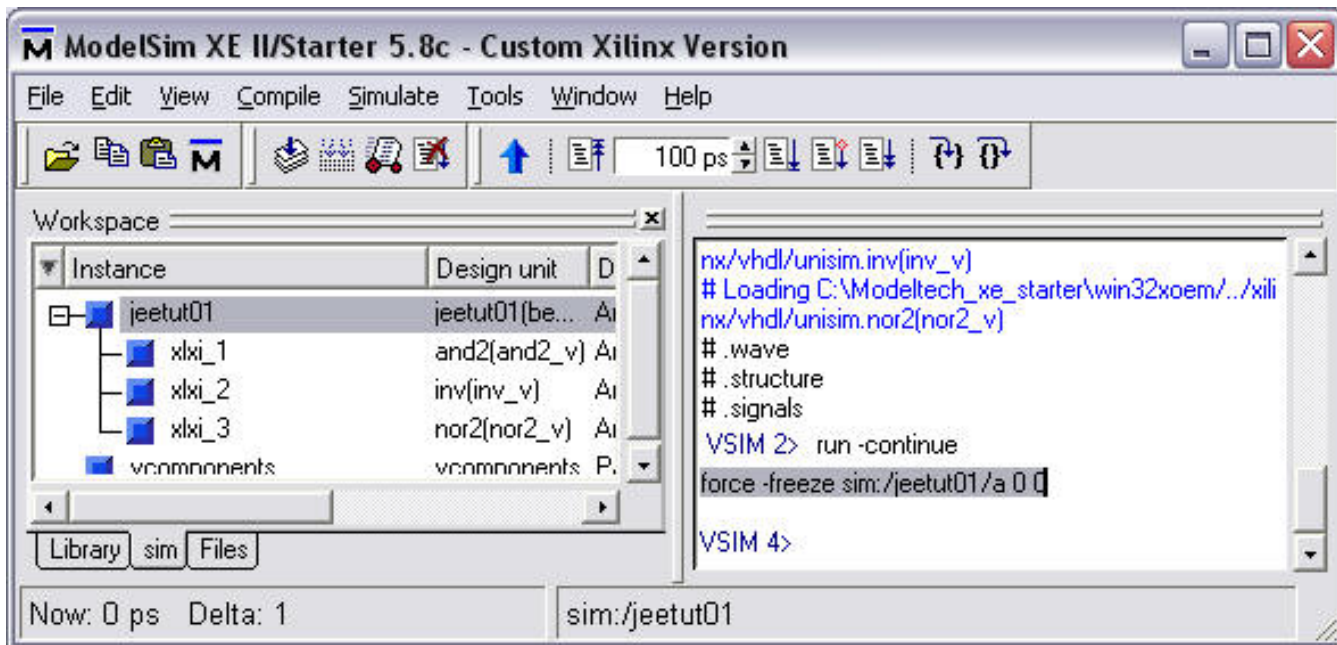
You can either use the dialog boxes to enter commands or type them in on the command window. You can also write a script file of ModelSim commands. Change signals b and c to 0. Now run the simulation by typing "run" on the command window.

ModelSim XE II/Starter 5.8c - Custom Xilinx Version

File Edit View Compile Simulate Tools Window Help

100 ps

Workspace

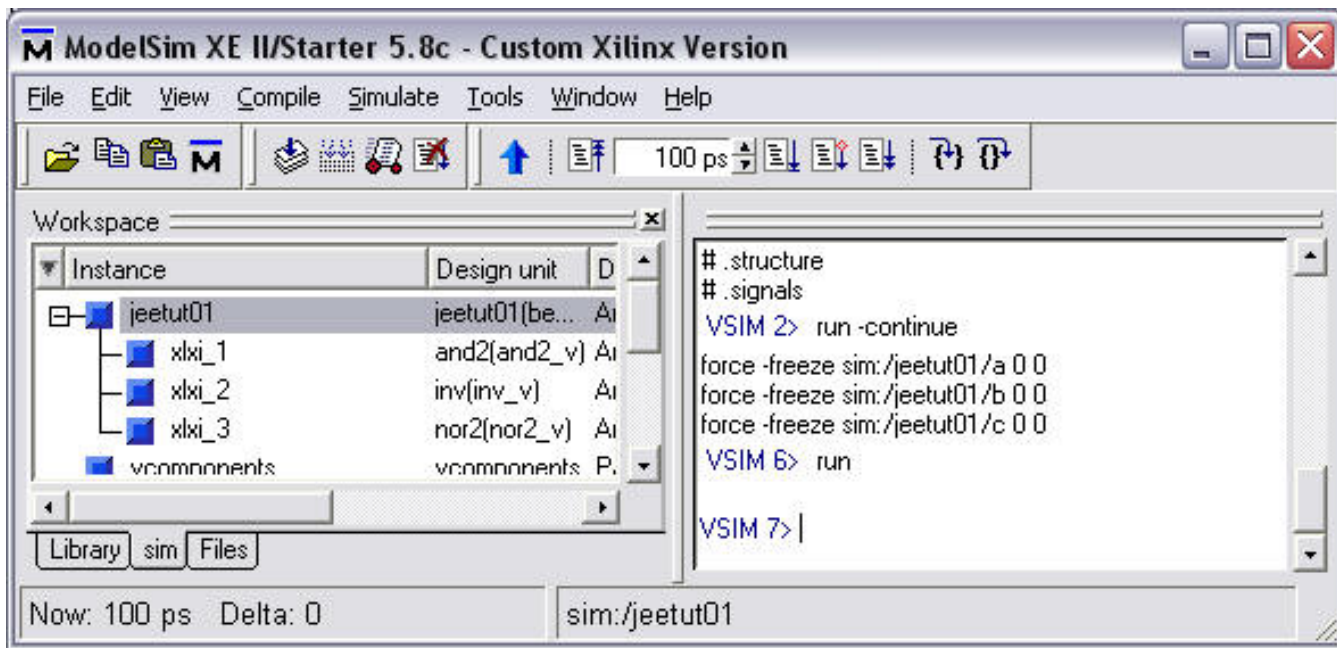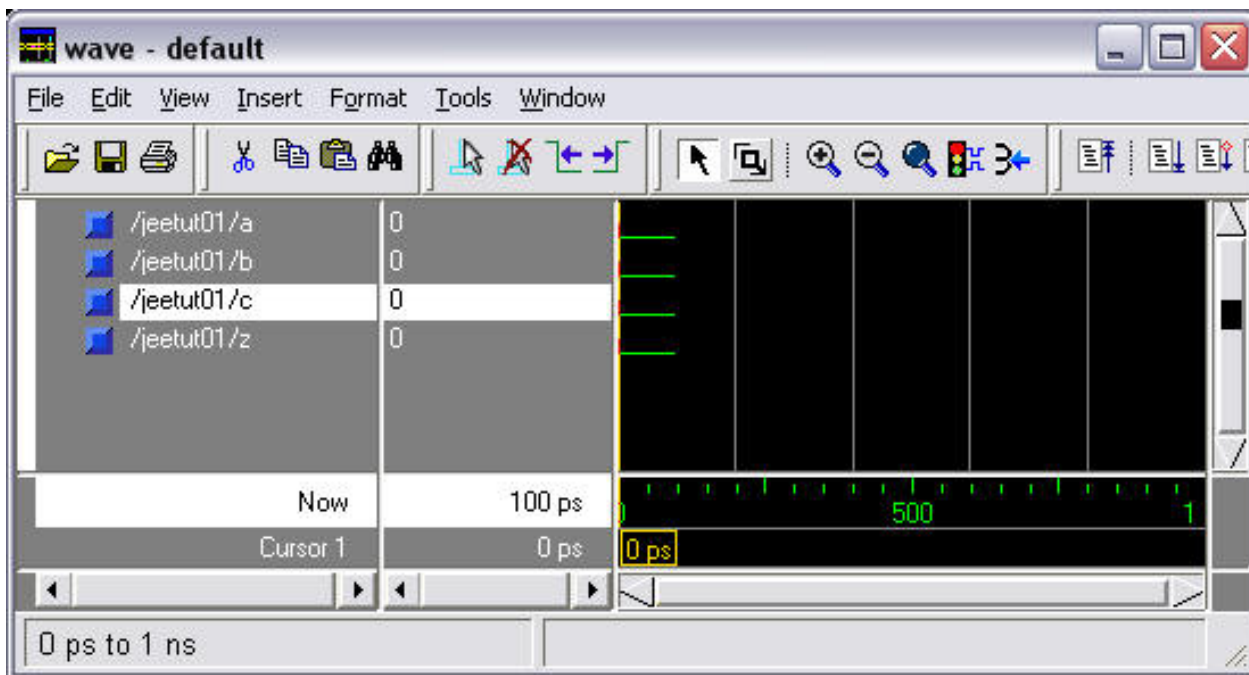| Instance	Design unit	D
jeetut01	jeetut01(be...	A
xlxi_1	and2(and2_v)	A
xlxi_2	inv(inv_v)	A
xlxi_3	nor2(nor2_v)	A
vcomponents	vcomponents	P.

Library | sim | Files

```
# .structure
# .signals
VSIM 2> run -continue
force -freeze sim:/jeetut01/a 0 0
force -freeze sim:/jeetut01/b 0 0
force -freeze sim:/jeetut01/c 0 0
VSIM 6> run

VSIM 7> |
```

Now: 100 ps   Delta: 0   sim:/jeetut01

Now, look at the wave page. Note the three inputs are all shown as low (0's) and the output z is also low (0). Does this agree with the input equation we were modeling here?

wave - default

File Edit View Insert Format Tools Window

/jeetut01/a	0
/jeetut01/b	0
/jeetut01/c	0
/jeetut01/z	0

| Now | 100 ps |
| Cursor 1 | 0 ps |

0 ps

500

0 ps to 1 ns

Next force inputs a, b, and c to 1, 0, 0 respectively. Type in run again. Repeat until you've covered all input states. Does the output waveform agree with the boolean expression for this circuit?

wave - default

File Edit View Insert Format Tools Window

/jeetut01/a	1		
/jeetut01/b	1		
/jeetut01/c	1		
/jeetut01/z	0		

Now	800 ps
Cursor 1	0 ps

0 ps

500

1

0 ps to 1 ns