ESE 566A Modern System-on-Chip Design, Spring 2017 Tutorial for Cadence Encounter

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1. Introduction

We use Cadence Encounter for placing and routing standard cells, but also for power routing and clock tree synthesis. The Verilog gate-level netlist generated by Synopsys DC has no physical information: it is just a netlist, so the Cadence Encounter will first try and do a rough placement of all of the gates into rows on the chip. Cadence Encounter will then do some preliminary routing, and iterate between more and more detailed placement and routing until it reaches the target cycle time (or gives up). Cadence Encounter will also route all of the power and ground rails in a grid and connect this grid to the power and ground pins of each standard cell, and Cadence Encounter will automatically generate a clock tree to distribute the clock to all sequential state elements with hopefully low skew. The automated flow for place-and-route is much more sophisticated compared to what we did in the previous tutorial.

2. Login to the Linux Lab server

Detailed explanation is in ese566-linux-tutorial.pdf

3. Getting prepared using Design Compiler

In the terminal, change path to your project directory, and compile your code using *design compiler*.

(If you don't know how to use design compiler, look at ese566-dc-tutorial.pdf)

4. Encounter

4.1 Start Encounter

Download the "<u>Default.view</u>" and modify it according to your design for MMMC view definition file later. Please specify the name of the *.sdc* file used in your synthesis script. It should be the *.sdc* file generated by *Design Compiler* in the previous design step.

	This is a file generated by Design Compiler.
1	# Version:1.0 MMMC View Definition F (You need to change it according to your design)
2	# Do Not Remove Above Line
3	create_library_set -name vtvt_tsmc180 -timing {/project/linuxlal/cadence/vendors/VTVT/vtvt_tsmc180/Synopsys_Libraries/libs/vtvt_tsmc180.lib}
4	create_constraint_mode -name constraint_rule -sdc_files
5	create_delay_corner -name_vtvt_tsmc180 -library_set (vtvt_tsmc180)
6	create_analysis_view -name constraint_rule -delay_corner vtvt_tsmc180 -constraint_mode (constraint_rule)
7	set_analysis_view -setup {constraint_rule} -hold {constraint_rule}
8	

Figure 4.1 Default.view

Then execute the following command in the shell to start encounter

% encounter

You will get the following printout in the terminal and a window pops up which looks like the one as below. This window will lead to the design window.

	Terminal – dengxue.yan@linu:	xlab009:~/ESE461/DCTutorial	×
File Edit View Terminal	Tabs Help		
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@(#)CDS: IQRC/TQRC	14.1.6-s260 (64bit)	Mon Mar 2 11:26:49 PST 2	015 (Linux 2.6.1
8-194.el5) @(#)CDS: 0A 22.50-p @(#)CDS: SGN 10.10- @(#)CDS: BCDB 11 5	011 Tue Nov 11 03:24 p124 (19-Aug-2014) (:55 2014 64 bit executable)	
Starting "Encou	nter v14.23-s044_1"	on Sat Oct 8 15:22:12 20	16 (mem=89.1M) -
Running on linu 6_64)	xlab009.seas.wustl.e	edu (x86_64 w/Linux 3.10.0	-327.22.2.el7.x8
This version was co Set DBUPerIGU to 10 Set net toggle Scal	mpiled on Fri Mar 20 00. e Factor to 1.00 e 1.00000	0 11:30:09 PDT 2015.	
**INF0: MMMC trans	ition support versig	n v31-84	
encounter 1>			

Figure 4.2 Command and the printout of "encounter"



Figure 4.3 The window popped out when execute "encounter"

En Set Set
Levy Carline & Y
1 Blackage 2 2 Perform 2 3 Perform 2 4 Perform 2 5 Perform 2 6 Perform 2 7 Perform 2 8 Perform 2 9 Perform <t< th=""></t<>

Figure 4.4 The design window of "encounter"

4.2 Import Design

Go to "File->Import Design" and add files to import your netlist file, and you have to:

- Provide synthesized Verilog (*.syn.v*) which is the output netlist file generated by Design Compiler in the previous design step.
- Provide path for the LEF file from technology library. Set path to *"/project/linuxlab/cadence/vendors/VTVT/vtvt_tsmc180/vtvt_tsmc180_lef*" and select the "*vtvt_tsmc180.lef*" file from the folder.
- Provide the supply nets as *vdd*! and *gnd*! in the appropriate boxes as below. These represent the global power supply and ground net in your design.
- Load the "Default.view" edited above for MMMC view definition file

	2. Uncollapse collapse the dir	ectory tist Files
Encounter(R) R Elipite Design ECQ Design Saye Design Create OA Library Import R]L RTL. Synthesis Load Save Check Design Egit Analysis MMMC V	Collapse the dir Collapse the dir Click here to the the the time syn (control control to the to control	Counter_vare Counter_vare Counter_vare Counter Counter_vare Counter Counter_vare Counter Counter Counter Counter Counter Counter Counter Counter Counter Counter Counter

Click "OK" to finish

Figure 4.4 Import netlist

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- Technology/P	Cell: View: Thysical Libraries:					4. Select	vtvt_smc180.lef
OA Deforence 1. Select here	e Libraries:	7. The result	> <	2. Click here	>		UVV_ismc180_inuaderiaa.gz ⊇ vlvt_ismc180_Streamin.map
Floorplan	lew Names: (cadence/	vendors/VTVT/vtvt_tsmc180/vt	vt_tsmc180_lef/vtvt_tsmc	180.10			
IO Assig	gnment File:					Delete	Filters
G	CPF File:						Close
MMMC View D	Pefinition File:	eate Analysis Configuration)	D			
<u>o</u> k	Save	Load	Cancel H	lelp			
			Figure	4.5 lm	port LE	F file	

	Design Import ×
Netlist:	
 Verilog 	
	Files: Counter.syn.v
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	Library:
	Cell:
	View:
Technology/Phy:	sical Libraries:
o oa	
Reference L	.ibraries:
Abstract View	Names:
Layout View	Names:
 LEF Files 	b/cadence/vendors/VTVT/vtvt_tsmc180/vtvt_tsmc180_lef/vtvt_tsmc180.lef
Floorplan	
1. Sp	ecify the power net
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Pov	ver Net vidi
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_	Z. Click n
Analysis Configu	Select Default.view
ranaysis configu	
lick OK to	finish Crete Andula Conferentia
mon on to	Create Analysis Configuration

Figure 4.6 Add power net and MMMC view file

Then, you will be seeing a blank screen with horizontal lines on your main window (layout window). Press "f" for fit screen view of layout.

7		

Figure 4.7 The initial layout window

Specify *"floorplan"* options in the *"Floorplan->Specify* Floorplan" and set the values as figure 4.8.

v Partitio <u>n</u>	FIG	orplan Po <u>w</u> er	Place	Optimize	Cloc	Specify Floo	orplan	×
) e (<	Specify Floorp	lan).			Basic Advanced		1
*		Structured Data Automatic Floo	a Path Irplan			Specify By: Size Die/IO/Core Core Size by: Siz	Coordinates Ratio (H/W):	1
		Resize Floorpla	эп				• Core Utilization:	0.699833
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	-				_	Dimension:	Width:	53.82
		Ro <u>₩</u>			- N -		Height:	45.36
		Eloorplan Tool	box			Die Size by:	Width:	53.82
		Edit Floorplan Snap Floorplar Check Floorpla	n an	Ctrl+	N	Core Margins by: Core to IO Bo Core to Die B Core to Left 10 Core to Right 10	Height: oundary .0 Core to Top .0 Ore to Bottom	45.36
	_	Instance Group Generate Regro	o ouped N	letlist	•	Die Size Calculation Use: 🔵 Max Floorplan Origin at: 💿 Lowe	: IO Height ● Min I r Left Corner ⊖ Cen	O Height ter Unit: Micron
		<u>G</u> enerate Floor	rplan		•		Cancel	Help

Figure 4.8 Specify Floorplan

Set the global nets vdd! and gnd! at "Power->Connect Global Nets".

G	lobal Net Connections	×	Global Net Connections	×
Connection List Provide Madeual Provide Provide Madeual Provide Provi	ver Ground Connection prin Tie High Tie Low Instance BasenIme: Pin Name(\$_vdd Net Basename: Cope Single Instance: Under Module: Under Power Domain: Under Power Domain: Under R Apply All Connection Perbose put Logate Delete Delete	Connection List	Power Ground Connection Onnect Image: Pin Te Low Instance Baser pine:* Pin Name(signal) Net Basename: Single Instance: Under Module: Under Power Domain: Under Power Domain: Under Rest Global Net genel Overrig 6 Uut Add to List 8. Finish Delete	
Contraction ((Truch) (Truch)			

Figure 4.9 Set the global nets

Go to "*Power->Add Ring*" and set Net pins to *vdd*!, *gnd*!. And you change width and spacing of power ring.

Fower Place Optimize Clock Route Timing Verify Option 2. Press Ctrl+Left Click to multi-select Connect Global Nets Basic Advanced Via Generation sen Nets 🔍 🔣 🔍 🕗 । 👶 १ 1 Multiple Supply Voltage Power Planning ddl Add Ring ... Net(s): Power Analysi Add Stripe. Rail Analysis Edit Power Via. Ring Type Report Create Power/Ground Pin. Ore ring(s) contouring Around core boundary Along I/O boundary PG Cut/Repair. Exclude selected objects Block ring(s) around Each block Each reef Selected power domain/fences/reefs Each selected block and/or group of core rows Cancel Help Clusters of selected blocks and/or groups of core rows With shared ring edges User defined coordinates: MouseClick O Block ring Core ring **Ring Configuration** Top: Bottom: Left: Right: Laver metal1 H ▶ metal1 H ▶ metal2 V ▶ metal2 V ▶ 0.45 0.45 0.45 0.45 Width: 0.45 0.45 Spacing: 0.45 0.45 Update Offset: 🔾 Center in channel 💿 Specify 0.81 0.81 0.81 0.81 **Option Set** 5 dd Ring Option ок Set Mode Apply Defaults Cancel Help

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Figure 4.10 Add power ring

We can also edit the pin placement in our design. Go to "*Edit->Pin Editor*". Group some pins and you can place them on left or right side of the design. If you don't specify *Encounter* will be taking appropriate placement during optimization. Once done click "*OK*"



Figure 4.11 Pin Editor

Watch how your layout is changing while you are setting the parameters in the GUI.



Figure 4.12 The layout view after edit pins

Place the vdd! and gnd! in the design. Go to "Route->Special Route"

Encounter(F	SRoute	× (2)	Net Selection ×
Route Timing Verify Options Generate Routing Guide Trial Route Special Route	Basic Advanced Via Generation Net(s): gndi vddi SRoute ✓ Block Pins P ad Rings ✓ P ad Rings P ad Rings ✓ P ad Rings P ad Rings ✓ P ad Rings P ad Rings ✓ Allow Layer: metalit ✓ Allow Layer: Change	Pissible Nets	Add see
Mgtəl Fill 🕨 🕨	Area X1 Y1 Prewv Y2 Prewv Connect to Target Inside The Area Only Oelete Existing Routes Generate Progress Messages Mode Setup		Cancel Help
	Target Editing Options		

Figure 4.13 Place vdd! and gnd!

1		
ł	↓ gndt	
4		
-	vdal vdal v	idi.
4		
	grid	
•		
4		

Figure 4.14 The layout after place vdd! and gnd!

Now we are all set to place the design. And then we go to "*Place->Place Standard Cell*". Click OK.



Figure 4.15 Place standard cell



Figure 4.16 The result after place standard cell

4.3 Clock tree synthesis

- Download <u>*Clock.ctstch*</u> and place it in working directory.
- Download <u>Clock.tcl</u> and place it in working directory.
- Open *Clock.tcl* using *gedit* and copy the content line by line to the *encounter terminal* and execute it.

Terminal – dengxue.yan@linuxlab009:~/ESE461/DCTutorial				
File Edit View Termina	il Tabs Help			
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Density: 70.455% Routing Overflow: 0.00% H and 0.00% V				
optDesign cpu = 0:00:01, real = 0:00:00, mem = 717.8M, totSessionCpu=0:05: 00 ** * Finished optDesign *** 0 encounter 8> <u>e</u> ncounter 8>				
encounter 8>				

Figure 4.17 Partial of clock tree synthesis commands and results

4.4 NanoRoute

As part of routing go to "*Route->NanoRoute->Route*". And click OK.

Boute Timing Verify Options PVS Tools Flows He	NanoRoute		
Generate Routing Guide Irial Route Snecial Route NanoRoute	Routing Phase Global Route Detail Route Detail Route Start Iteration default End Iteration default Post Route Optimization Optimize Via Optimize Wire		
Metal Fill Route	Concurrent Routing Features		
Via Fill Minalyze Congestion	Version States Fix Antenna Insert Diodes Diode Cell Name		
	Timing Driven Effort 5 Congestion Timing S.M.A.R.T.		
	SI Driven		
	Post Route SI SI Victim File		
	Litho Driven		
	🔤 Post Route Litho Repair		
	Routing Control Selected Nets Only Bottom Layer default ECO Route Select Area and Route Area Route Select Area and Route		
	Job Control		
	Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 Set Multiple CPU		
	OK Apply Attribute Mode Save Load Close Figure 4 18 Nano route	Help	

You will see that your design got placed in the layout and all the interconnections are done.

4.5 Add Filler.

"Place->Physical Cell->Add Filler". Select "filler" cell name and click OK.

Place Optimize Clock	<u>R</u> oute <u>Ti</u> ming Verif <u>y</u>	Add Filler	Select	Filler Cells
Specify Place Jtag Place Standard Cell Place Spare Cell	1 🕅 C O .	Cell Name(s) filler Select Prefix FiLLER Power Domain Select No DRC Mark Elword Select	Selectable Cells List	
Refine Placement ECO Placement Physical Cell Te Hi/Lo Cell Scan Chain	Add Well Tap Add End Cap Add Filler	Mail K Fixed Drawy View Area Fill Area Iix Iiy 5 urx ury 0K Apply Mode Cancel Help		Add
Check_Placement Display Query Density	Delete Filler Add I/O Filler Delete I/O Filler Check Filler			

Figure 4.19 Add Filler

4.6 Verification

Once Place and Route is done:

- Go to "Verify->Verify Geometry". Click OK.
- Go to "Verify->DRC". Click OK
- Go to "Verify-> Connectivity". Click OK

Check the terminal every time for any violations and warnings.



Figure 4.20 Verify Geometry

Cettons PVS Tods Verify Geometry. Verify Office States Verify Office States Verify AC Limit. Verify Directs Antenna. Verify AC Limit. Verify Bis Guide Verify Metal Density Verify Metal Density Verify Pgwer Via	Verify DRC × ******** End: VE asic Advanced Verifacation Area (CPU Time: 0:0) • Entire area • [gew Area > X2 0 > Layer Range: Bottom Layer. MD Det Apply Cott Apply Cancel Heip Verification O Verification O Verify DRC Verify DRC Verification O Verification O	RIFY CONNECTIVITY ******* complete : 0 Viols. 0 Wrngs. 00:00.0 MEM: 0.000M) * Starting Verify DRC (MEM: 785.1) *** Starting Verification Initializing Deleting Existing Violations Creating Sub-Areas Using new threading Sub-Area : 1 of 1 Sub-Area : 1 complete 0 Viols. Complete : 0 Viols.
	*** End Verify	DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.1M) ***
	Figure 4.21 Verif	y DRC
Verify Geometry Verify Geometry Verify Process Antenna Verify Process Antenna Verify AC Limit Verify End Cap Verify Metal Density Verify Metal Density Verify Pgwer Via	Verify Connectivity Net Type All Regular Only Special Only Named: Check Open UnConnected Pin Unrouted Net Connectivity Loop DanglingWire (Antenna) Weakly Connected Pin Connectivity Loop Geometry Loop Geometry Loop Divide Power Net Soft PG Connect Raw Violations Mark Use Virtual Connection TSV Die Abstract File Verify Connectivity Report: Counter.conn.rpt Report Limits Error: 1000 Warning: 50 Set Multiple CPU	<pre>******** Start: VERIFY CONNECTIVITY ******* Start Time: Sun Oct 9 11:00:41 2016 Design Name: Counter Database Units: 1000 Design Boundary: (0.0000, 0.0000) (74.3400, 65.8800) Error Limit = 1000; Warning Limit = 50 Check all nets Begin Summary Found no problems or warnings. End Summary End Time: Sun Oct 9 11:00:41 2016 Time Elapsed: 0:00:00.0 ******** End. VERIFY CONNECTIVITY Verification Complete : 0 Viols. 0 Wrngs. (CPU Time: 0:00:00.0 MEM. 0.000W)</pre>

Figure 4.22 Verify Connectivity

4.7 Timing report

Configure MMMC	Timing Analysis	× timeDes	ign Summary			
Genetat Coperation Table Extract RC Extract RC Cross Human Coperations Grass Back Box Model Write SOF Display Timing Map	Basic Advanced Use Existing Extraction and Timing Data Pre-Place & Pre-CTS Post-CTS Post-Route Sign-Off Analysis Type Setup Hold Include SI Reporting Options Number of Partie: 50 Report file(s) Prefix: Counter_pre-CTS Output Directory: EmingReports EXX	Setup mode WNS (n TNS (n Violating Pan All Pan	all ns): 48.248 ns): 0.000 ths: 0 ths: 5	reg2reg 48.248 0.000 0 5	default 49.017 0.000 0 5	+ +
		DRVs DRVs max_cap max_tran	 Nr nets(ter 0 (0) 0 (0)	Real ms) Wors 0. 0.	t Vio 000 000	Total Nr nets(terms) 0 (0) 0 (0)
		max_fanout max_length bensity: 100.000% Routing Overflow: Reported timing to Total CPU time: 0 Total Real time: 0	0 (0) 0 00% H and 0 0 dir timingRe 16 sec 0 sec 0 882 257812	0.00% V ports	0 0	0 (0) 0 (0)

Figure 4.22 Generating timing report

4.8 Additional Information

Save your design for later use. "*File -> Save*". Give an output file name for each floorplan, Place, Netlist and DEF file so that you can save all the optimization options and can load it later.



Figure 4.23 Save your project

5. Reference

- [1] https://cornell-ece5745.github.io/ece5745-tut5-asic-tools/
- [2] https://cornell-ece5745.github.io/ece5745-tut6-asic-flow/
- [3] http://classes.engineering.wustl.edu/ese566/Tutorial/ese566-linux-tutorial.pdf
- [4] http://classes.engineering.wustl.edu/ese566/Tutorial/ese566-vcs-tutorial.pdf
- [5] http://classes.engineering.wustl.edu/ese566/Tutorial/ese566-dc-tutorial.pdf
- [6] http://www.csl.cornell.edu/courses/ece5745/handouts.html